Abhinav Agarwal

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Areas of Interest

High-level hardware design, FPGA-based rapid prototyping and hardware modeling, Low-power design for wireless applications, Computer Architecture.

Education

Massachusetts Institute of Technology, Cambridge, MA

Ph.D., Electrical Engineering and Computer Science, *Expected:* Summer 2014

- Thesis Topic: *Use of high-level design information to enable automatic power gating*
- Advisor: Prof. Arvind

S.M., Electrical Engineering and Computer Science, Feb 2009

- Thesis Topic: *Comparison of high-level design methodologies for algorithmic IPs*
- Advisor: Prof. Arvind

Indian Institute of Technology, Kanpur, India

B.Tech., GPA: 10.0/10.0, Electrical Engineering, June 2006

Work Experience

Research Internships

Corporate R & D, Qualcomm Incorporated, San Diego, CA
Supervisor: Suhas Pai, Ph.D

- Establishing Quality-Of-Results metrics for evaluating use of different design methodologies for accelerating design processes. **May-Aug 2009**
- Accelerating design testbenches using Dini FPGA platforms and enabling rapid prototyping **May-Aug 2008**
- Development of SCE-MI transactors for generating FPGA-based testbenches for legacy IPs **May-Aug 2007**

Processor Architecture Laboratory, EPFL, Switzerland
Supervisor: Prof. Paolo Ienne

- Profiling and Debugging tools for URLAP Platform. **May-Aug 2005**

Publications

1. **Agarwal, A.**, Hassanieh, H., Abari, O., Hamed, E., Katabi, D., and Arvind. "High-throughput implementation of a million-point Sparse Fourier transform" *Intl. Conf. on Field Programmable Logic and applications*, 2014.
2. **Agarwal, A.** and Arvind. "Leveraging rule-based designs for automatic power domain partitioning" *Intl. Conf. on Computer Aided Design*, 2013.
3. Abari, O., Hamed, E., Hassanieh, H., **Agarwal, A.**, Katabi, D., Chandrakasan, A., and Stojanovic, V. "A 0.75 million-point Fourier transform chip for frequency-sparse signals" *Intl. Solid-State Circuits Conf.*, 2014.
4. King, M., Khan, A., **Agarwal, A.**, Arcas, O., and Arvind. "Generating infrastructure for FPGA-accelerated applications" *Intl. Conf. on Field Programmable Logic and applications*, 2013.
5. **Agarwal, A.**, Ng, M. C., and Arvind. "A comparative evaluation of high-level hardware synthesis using Reed-Solomon decoder" *IEEE Embedded Systems Letters*, 2(3), 2010.
6. **Agarwal A.**, Dave, N., Fleming K., Khan, A., King, M., Ng, M. C., and Vijayaraghavan, M. "Implementing a fast Cartesian-Polar matrix Interpolator" *Intl. Conf. on Formal Methods & Models for Codesign*, 2009.