Anurag Mukkara

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EDUCATION

Massachusetts Institute of Technology Sep 2016 - Jan 2020
Ph.D. in Computer Science - **ABD Status**
Advisor: Prof. Daniel Sanchez

Massachusetts Institute of Technology Sep 2014 - May 2016
S.M. in Computer Science, GPA: 5.0 / 5.0
Advisor: Prof. Daniel Sanchez
Thesis: Techniques to Improve Dynamic Cache Management with Static Data Classification

Indian Institute of Technology Bombay July 2010 - April 2014
Bachelors in Electrical Engineering, GPA: 9.8 / 10.0
Minor in Computer Science and Honors in Electrical Engineering

EXPERIENCE

Graduate Research Assistant Sep 2014 - Jan 2020
Computer Science and Artificial Intelligence Laboratory, MIT, Cambridge, MA
Advisor: Prof. Daniel Sanchez

- Developed techniques to improve memory performance of bandwidth-saturated graph analytics applications.
- Proposed custom hardware support near the core and throughout the memory hierarchy to accelerate important graph operations.
- Implemented software optimizations that improve performance of state-of-the-art graph analytics frameworks by 2× on average.
- Worked on improving performance of multicores with distributed cache hierarchies, by exploiting software hints to dynamically adapt the cache configuration to application behavior.
- Developed a custom memory allocator to convey hints from applications to custom hardware in cache hierarchy.

Ph.D. Intern June 2016 - Aug 2016
Architecture Research Group, Nvidia, Westford, MA
Manager: Steve Keckler

- Worked on analytical modeling methodology for specialized hardware architectures that accelerate deep neural network (DNN) applications.
- Contributed to Timeloop, an open-source tool that finds the best mapping of a DNN kernel on to a hardware architecture while co-optimizing performance, area and energy.

Undergraduate Research Assistant Aug 2013 - Dec 2013
Computer Architecture and Dependable Systems Lab, IIT Bombay
Advisor: Prof. Virendra Singh

- Worked on algorithms to combine fine-grained and coarse-grained DVFS state changes with dynamic core-switching in a heterogeneous processor architecture.
- Used machine-learning techniques to train models that dynamically choose the best core-backend and DVFS state.

Research Intern May 2013 - July 2013
Computer Systems Lab, Cornell University, Ithaca, NY
Advisor: Prof. Rajit Manohar

- Worked on RTL Design and validation of a custom ARM processor intended for Mobile Computing applications.
- Responsible for the design of Memory Management Unit (MMU), cache hierarchy, prototyping the design on a Xilinx Virtex-6 FPGA board and obtaining power, area estimates for a 45nm ASIC implementation.

Research Intern May 2012 - July 2012
ECE Department, University of Toronto, Canada
Advisor: Prof. Farid Najm

- Worked on techniques to reduce dimensionality of feasible space in incremental verification of integrated circuit power grids.

Teaching Assistant Aug 2011 - Apr 2013

Indian Institute of Technology Bombay

- Worked as TA for 3 undergraduate courses - Electricity and Magnetism, Linear Algebra and Differential Equations, over a period of 2 years.
- Placed in charge of more than 50 students, conducted weekly classes and tutorials, responsible for setting examinations and evaluating answer scripts.

TECHNICAL SKILLS

- **Programming Languages** - C/C++, Python, Go. Experienced in parallel programming.
- **Computer Architecture Tools** - Intel Pin, ZSim, McPAT.
- **Software Packages** - Matlab, Altera FPGA Design tools, Synopsys Design Compiler.
- **Miscellaneous** - Comfortable with gcc/make/command-line tools and bash-scripting. Experienced with Linux.

RELEVANT COURSES

- **Graduate:** Computer Architecture, Computer Systems Security, Computer Vision, Computational Cognitive Science, Theory of Computation, Distributed Systems.
- **UG Computer Science:** Machine Learning, Computer Networks, Operating Systems, Data Structures and Algorithms, Discrete Structures.
- **UG Electrical Engineering:** Advanced Topics in Computer Architecture, Processor Design, Foundations of VLSI CAD, Microprocessors, Testing and Verification of VLSI Circuits, Hardware Software Co-design of Embedded Systems.

AWARDS

- OP Jindal Engineering and Management Scholarship - 2011.
- KPMG Foundation Scholarship - 2011-2014.
- Narotam Sekhsaria Scholarship for meritorious undergraduate student in engineering - 2012-13.
- International Research Internship Program Scholar - Cornell University, 2013.
- Undergraduate Research Award - IIT Bombay, 2013
- Institute Academic Prize - IIT Bombay, 2010-11, 2012-13
- Secured rank 2 in All India Engineering Entrance Examination (AIEEE) - 2010
- Secured rank 135 in Indian Institute of Technology Joint Entrance Examination (IITJEE) - 2010

PUBLICATIONS

PHI: Architectural Support for Synchronization and Bandwidth-Efficient Commutative Scatter Updates.
Anurag Mukkara, Nathan Beckmann, Daniel Sanchez.
The 52nd IEEE/ACM International Symposium on Microarchitecture (MICRO-52).

Timeloop: A Systematic Approach to DNN Accelerator Evaluation.
Angshuman Parashar, Priyanka Raina, Yakun Sophia Shao, Yu-Hsin Chen, Victor A. Ying, **Anurag Mukkara**, Rangharajan Venkatesan, Brucek Khailany, Stephen W. Keckler, Joel Emer.
The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS-2019).

Exploiting Locality in Graph Analytics through Hardware-Accelerated Traversal Scheduling.
Anurag Mukkara, Nathan Beckmann, Maleen Abeydeera, Xiaosong Ma, Daniel Sanchez.
The 51st IEEE/ACM International Symposium on Microarchitecture (MICRO-51).

KPart: A Hybrid Cache Partitioning-Sharing Technique for Commodity Multicores.
Nosayba El-Sayed, **Anurag Mukkara**, Po-An Tsai, Harshad Kasture, Xiaosong Ma, Daniel Sanchez.
The 24th IEEE International Symposium on High Performance Computer Architecture (HPCA-24).

SCNN: An Accelerator for Compressed-sparse Convolutional Neural Networks.
Angshuman Parashar, Minsoo Rhu, **Anurag Mukkara**, Antonio Puglielli, Rangharajan Venkatesan, Brucek Khailany, Joel Emer, Stephen W. Keckler, William J. Dally.
The 44th IEEE/ACM International Symposium on Computer Architecture (ISCA-44).

Whirlpool: Improving Dynamic Cache Management with Static Data Classification.
Anurag Mukkara, Nathan Beckmann, Daniel Sanchez.
The 21st ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS-21).

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