Anurag Mukkara

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Education

Sep 2016–Jan 2020 **Ph.D in Computer Science (ABD Status), Massachusetts Institute of Technology**.
Advisor: Prof. Daniel Sanchez, Minor in Brain and Cognitive Sciences

June 2016 **S.M. in Computer Science, Massachusetts Institute of Technology.** GPA:5.0/5.0.
Thesis: Techniques to improve dynamic cache management with static data classification.
Courses: Computer Architecture, Computer Security, Computer Vision, Distributed Systems, Computational Cognitive Science, Theory of Computation.

August 2014 **B.Tech in Electrical Engineering, Indian Institute of Technology Bombay.**GPA:9.8/10.

Experience

Sep 2014–Jan 2020 **Research Assistant**, MIT Computer Science and Artificial Intelligence Lab.

- Developed techniques to improve memory performance of bandwidth-saturated graph analytics applications. Proposed custom hardware support near the core (MICRO-18) and throughout the memory hierarchy (MICRO-19) to accelerate important graph operations. Implemented software optimizations that improve performance of state-of-the-art graph analytics frameworks by 2× on average.
- Worked on improving performance of multicores with distributed cache hierarchies, by exploiting software hints to dynamically adapt the cache configuration to application behavior (ASPLOS-16). Developed a custom memory allocator to convey hints from applications to custom hardware in cache hierarchy.

June–Aug 2016 **Ph.D. Intern**, NVIDIA Research.

- Worked on analytical modeling methodology for specialized hardware architectures that accelerate deep neural network (DNN) applications.
- Contributed to Timeloop, an open-source tool that finds the best mapping of a DNN kernel on to a hardware architecture while co-optimizing performance, area and energy.

May–July 2013 **Undergraduate Intern**, Cornell University.

- Worked on RTL design and validation of a custom ARM processor for mobile computing.
- Responsible for design of memory management unit (MMU) and cache hierarchy, FPGA prototyping and obtaining power, area estimates for 45nm ASIC.

First Author Publications

MICRO 2019 Architectural Support for Synchronization & Bandwidth-Efficient Commutative Scatter Updates
MICRO 2018 Exploiting Locality in Graph Analytics through Hardware-Accelerated Traversal Scheduling
ASPLOS 2016 Whirlpool: Improving Dynamic Cache Management with Static Data Classification

Skills

Summary 4 years experience in parallel programming and performance engineering in C++.
5 years experience in performance analysis on server systems and through C++ simulators.
5 years experience in data analysis and presentation using numpy and matplotlib.

Languages C, C++, Python, Go, CUDA, Verilog

Tools Git, Bash, Intel Pin, Zsim, Matlab

Awards

- Secured rank 2 in AIEEE 2010
- OP Jindal Engineering and Management Scholarship 2011
- IIT Bombay Institute Academic Prize 2010-11, 2012-13
- Secured rank 135 in IITJEE 2010
- KPMG Foundation Scholarship 2011-2014
- Narotam Sekhsaria Scholarship 2012-13