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CSE 291: Operating Systems in Datacenters

Amy Ousterhout

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Agenda for Today

- Processor pipelines
- Warehouse-Scale Computer discussion
- AccelNet discussion

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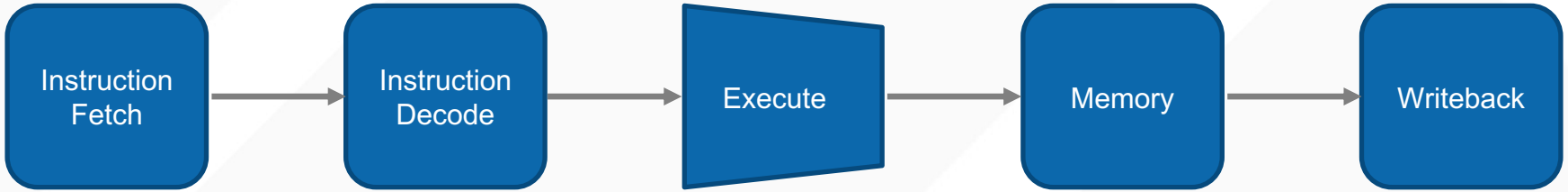
Processor Pipelines

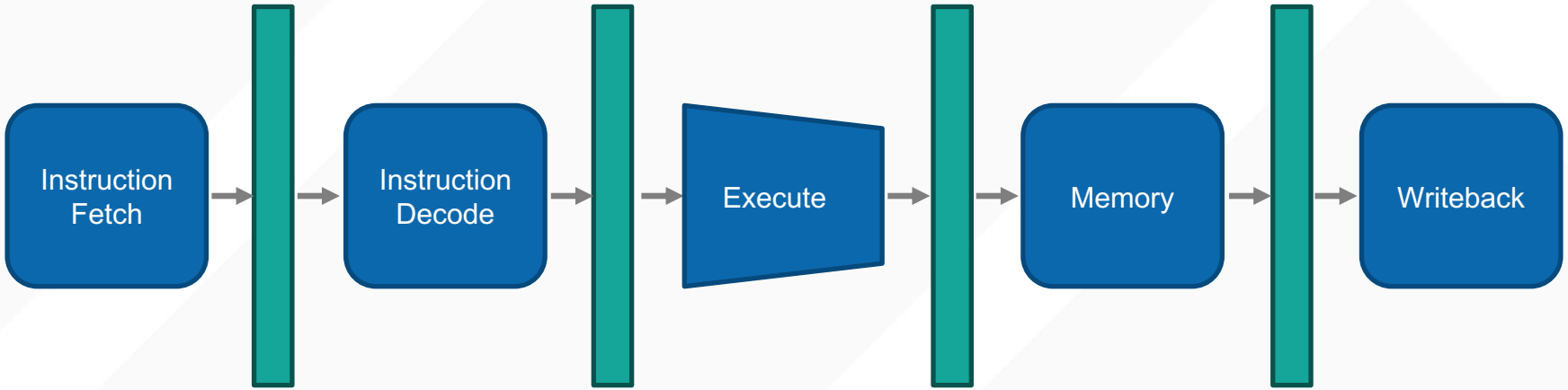
Single-cycle Processor

- In each clock cycle:
  - Fetch one instruction from memory
  - Decode instruction, read from registers
  - Execute (ALU operations, compute branch targets)
  - Read or write to memory
  - Write results to register file



Pipelined Processor

- Break instructions into multiple clock cycles
- Add registers to store state between stages
- Five-stage RISC architecture
- Benefits:
  - Shorter clock cycle, more efficient use of resources

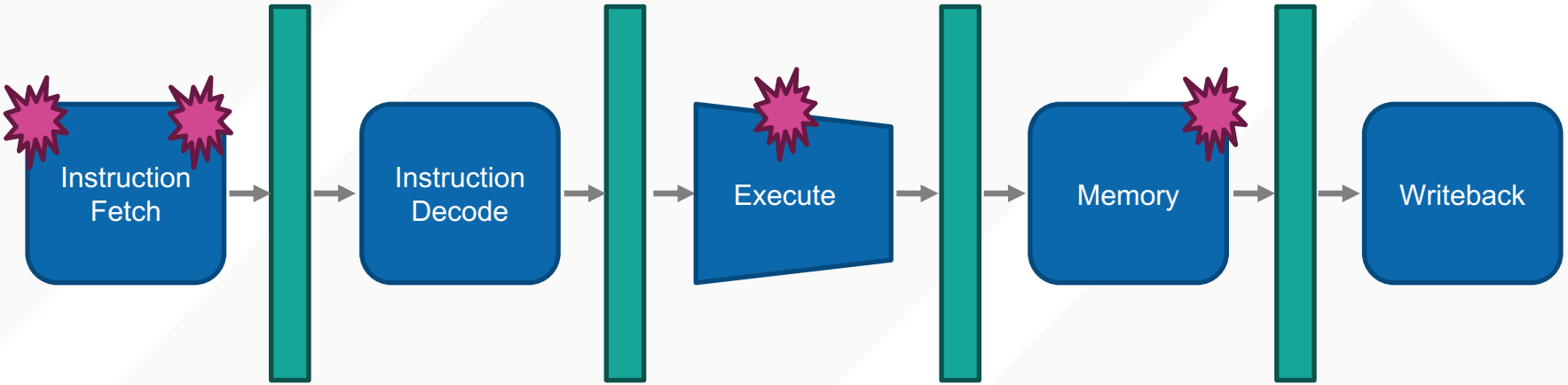


Modern Processors

- Modern processors are much more complex!
  - Execute instructions out of order
  - Speculative execution
  - Multiple instructions in each stage at once
  - Each instruction is translated into multiple micro-operations (uops)
  - Simultaneous multithreading (hyperthreads)

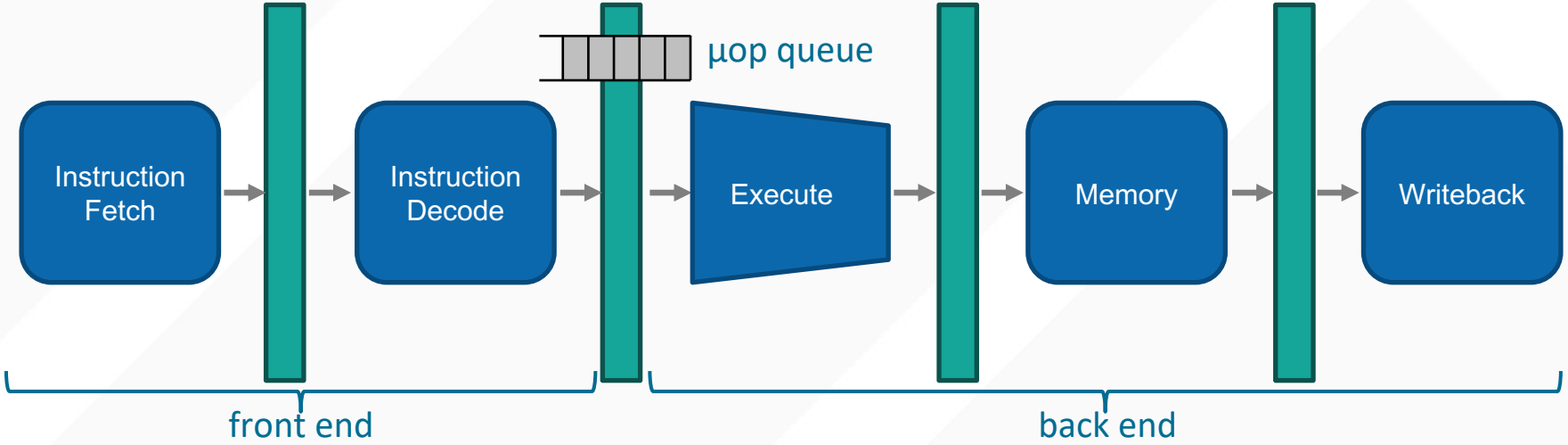
What Can Go Wrong?

- Ideally, the processor completes N instruction every clock cycle
- What can cause this to not happen?
  - Instruction cache miss, data cache miss
  - Branch mispredict
  - Not enough execution units



How Can We Diagnose What Went Wrong?

- Challenging because multiple issues may occur simultaneously
- Top-Down: analyze the problem hierarchically
  - Divide the processor in two by the µop queue
  - First: front end or back end?
  - Next: dig deeper into the specific problem



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Warehouse-Scale Computer Discussion
AccelNet Discussion