WPM 2.5: An Object Position and Orientation IC with Embedded Imager*

David L. Standley, Berthold K. P. Horn
Department of Electrical Engineering, Massachusetts Institute of Technology, Cambridge, MA

An analog VLSI chip that determines the position and orientation of an object against a dark background implements an algorithm based on finding the first and second moments of the spatial intensity distribution of the object.[1] These moments allow the centroid (an indicator of position) and the axis of least inertia (an indicator of orientation) to be computed. (Figure 1) The chip has a self-contained array of phototransistors, which are available in CMOS, so that the input is acquired by focussing the scene directly onto the chip surface.[2] Using a scheme proposed by Horn, the moments are computed by using a uniform grid of linear resistors.[3] Only eight measurements are required. Resistive sheets have been used in earlier systems to determine the position of objects, e.g. a small, bright spot.[3] Also, the analog VLSI chip by DeWeerth et al. finds the centroid of an object, though using a different method.[4] Neither performs the orientation task, which is the primary emphasis of the design presented here.

Figures 2 and 3 show the chip architecture. The resistor grid and photo receptor cell array occupies most of the active chip area. The grid is a 30-by-30 array of 3kΩ polysilicon resistors, which is associated with a 29-by-29 array of photoreceptor cells. Each photoreceptor cell contains a phototransistor together with other circuitry to produce an output current roughly proportional to the incident light intensity. This current is injectetd into the grid at each location. Because of this gray-level feature, subpixel resolution can be achieved, provided the image is slightly blurred. If the background is not sufficiently dark to be negligible, as is typically the case, the cells can completely remove the background by subtracting an adjustable threshold from the light intensity signal and clamping negative values to zero. Around the perimeter of the grid are the current buffers, which hold each perimeter node at a common dc voltage and convey the currents flowing out of the grid into uniform and quadratic resistor lines at the periphery, as shown in Figure 3. The buffer outputs can be simultaneously steered to either the uniform or quadratic lines, and the corresponding sets of output currents, $i_1 - i_4$ and $i_5 - i_8$ respectively, are measured. The lines implement spatially-weighted sums of the currents out of the grid. In particular, each quadratic line weights the currents out of a side of the grid according to the square of the normalized distance along the line, where the origins are at the left and the bottom for the horizontally and vertically oriented lines, respectively. The resistors in the lines are polysilicon, and each resistor in each quadratic line is made by connecting certain other resistors selected from a set of "primitives" in series. The ends of the lines are held at a virtual ground by external op-amps (not shown) that convert the currents flowing out of the chip into voltages. The eight output quantities are enough to find the object position and orientation with simple formulas.

Figure 4 shows the schematic of a photoreceptor cell, together with bias sources on global busses, which are realized by diode-connected pFETs driven by external current sources. All sizes are in micrometers. Transistors M1 - M3 form the thresholding current source i_{th} which subtracts from the photocurrent i_p, of Q1. The gate of output transistor M4 is held at about 3.0V above ground. The drain of M4 is the cell output, which is connected to the resistor grid. In normal operaton, the grid voltage is at most 3.0V, and thus M4, which is either cut off or in saturation, acts like a diode in addition to a cascode transistor which gives a higher output resistance than if M4 were simply diode-connected. If the incident light level is below the threshold, i.e. if $i_p < i_{th}$ the output current $i_o = 0$. If the light level is above the threshold, i.e. $i_p > i_{th}$ then $i_o = i_p - i_{th}$. The result is a continuous, piecewise-linear dc response curve. Diode-connected pFET M5 is connected to a bus normally held high, so it is cut off.

Grounding this toggle bus forces i_o to zero for all the cells. By measuring the final outputs with all cells "shut off", the net effects of offset errors in the system are measured and thus cancellable. This is done in all experiments. Typical operating currents are $i_p = 0.1$ to $1.0\mu A$ and $i_{th} = 0.2\mu A$. Reference 5 discusses the current buffers.

Working chips have been fabricated in a 2μm p-well process. Total chip dimensions are 7.2x9.2mm., and the light-sensitive cell array occupies 5.5x5.5mm. Power is nominally 30mW, which is shared between the 841 photoreceptor cells and the 116 current buffers.[5] Performance is dependent on object size and shape, but changes in orientation can typically be measured to within ±2° for elongated and moderately-sized objects, e.g. a rectangle of dimensions 30 by 60 on a 100 by 100 image field. The position of a 25 by 25 square is determined to within ±0.3% of the range for which the object remains completely in the image field, when referenced to a linear least-squares fit line. Measurements of the response to light pulses show that the chip operates at about 5000 images per second. Though the system operates in continuous time, speed can be characterized for images that remain constant over a certain period. This is analogous to the settling performance of operational amplifiers. The speed is limited by the photoreceptor cells.

Acknowledgments:

The authors thank H-S. Lee, C. Sodini, and J. Wyatt for comments.

References

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*This work was supported by the National Science Foundation and the Defense Advanced Research Projects Agency under Contract MIP-8814612, and DuPont Corp.

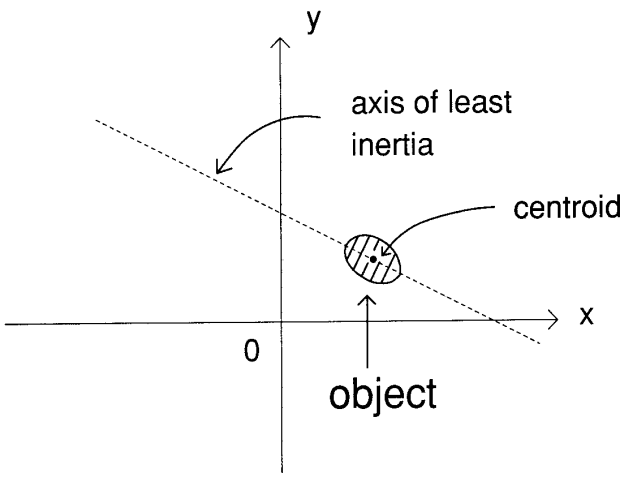

Figure 1: Example of object centroid and axis of least inertia.

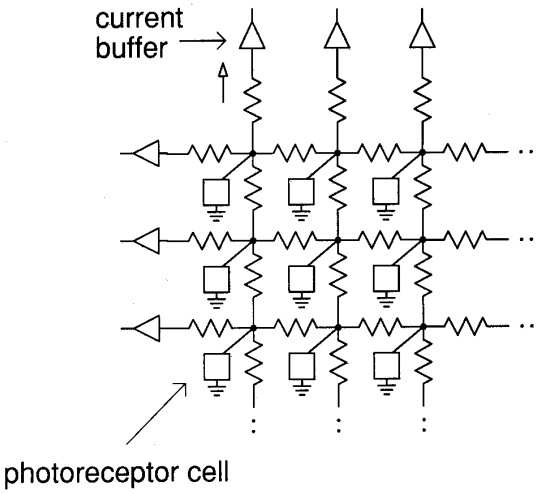

Figure 2: Resistor grid and photoreceptor cell array.

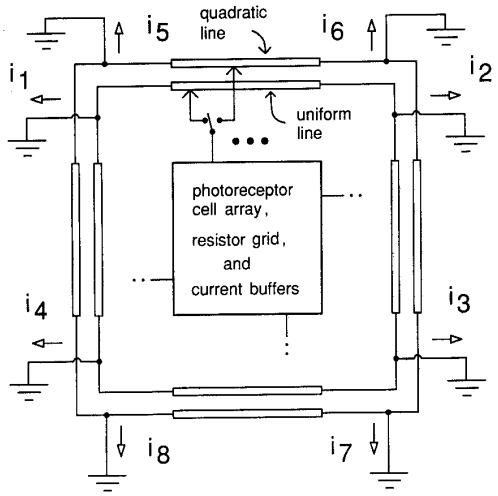

Figure 3: Main chip architecture.

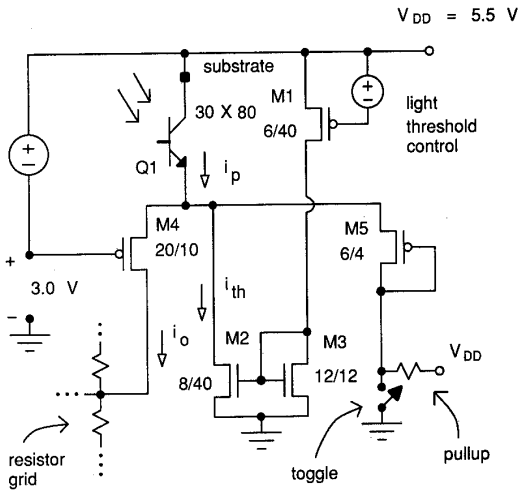

Figure 4: Circuit for photoreceptor cell. Voltage sources and the toggle are on global busses.