MEMORANDUM

To: ASD                          April 25, 1990
From: Rick Jordan
Re: Features of new machine for patent consideration

The following are the concepts and features in the new machine that are currently being considered for patenting. Please let me know if there are any other concepts or features that should be considered. In addition, please let me know of any prior art for any concept or feature, as we will use that information in determining whether to pursue patent protection therefor, as well as in determining the scope of protection we can reasonably expect.

Please review this carefully. We will file only on the items that are identified to me (those listed here and others that you identify in the next few weeks), at least during a first round. Accordingly, if anything not listed here is a likely candidate, please let me know.

I. Architecture

1. Massively Parallel Processor in which processing elements communicate over two (generally separate, asynchronous) networks: data net and control net, of considerably different structure.

Data net is a "fat tree" design and control net is a standard tree design.

2. Subsidiary ideas:

(a) addition of diagnostic network (standard tree) to handle diagnostic functions.

(b) Scalar control processors and input/output processors as nodes, similar to processing elements.

(c) Clock Tree to guarantee synchronicity of edges of clock signal at all chips in large system.

II. Other (possibly) independent ideas:

1. Method and apparatus for controlling transfer of messages through fat tree network. Data network messages identify target height and fixed path down; data network router directs messages up along random path until reach target height, then along fixed path identified in message to target. This provides fault tolerance and reduces likelihood of bottlenecks.

2. Method and apparatus ("Kirchoff counter") for determining when data network is empty. Counter values monitored periodically over control network.
3. Method and apparatus for mapping messages for physical processors, using address map in interface, to facilitate partitioning of data network. In addition, control of control network in view of processor mapping.

4. Method and apparatus for aligning operation of processors, in control network. (This may be covered, in part, in a pending patent application directed to alignment. We may want to update that application to add embodiment for new machine.)

5. Method and apparatus, in control network for effecting combining of messages; identification of conflicts or errors and broadcasting of error messages over control network. How scalar processors and input/output processor notify control network chips that they are not to participate in combining operations, so that the chips do not wait for messages from them before combining.

6. Two issues for task switching, particularly re message transmission over data network:

   (a) Method and apparatus for inhibiting PE's from transmitting messages over data network. First-in first-out buffer arrangement at each PE network interface. At context switch, each PE transmits flush packet up data (?) network.

   (b) "All fall down" technique in data network. In response to context switch, the control network transmits command to data network (chips) to go into "all fall down" mode. In that mode, the data network transmits messages down to closest PE for storage before context switch. When switch back to the particular context, the PE's all transmit messages received during "all fall down" mode.

7. In diagnostic network: Ability of the diagnostic network to address and test a section of the PE's in parallel, and quickly identify a faulty chip.

8. In control network: use of bits in messages otherwise for transmission to or from the PE's to control the control network.

9. Features for testing diagnostic network, such as loop backs, perhaps others.

10. In scanning (during diagnosis) tracking errors and notifying other processors not to transmit or receive from a faulty PE.

11. Digital phase-locked loop circuit to control delay of clock edge using a micro-sequencer. (This has been filed.)

12. ECC in memory controller using by-4 memory chips, can detect 3 or 4 bit errors if they have certain chip relationships. (This may already be covered by a previously-filed patent application).

13. Differential pad circuit (a) optimized for common mode signal rejection and (b) that detects when one wire is stuck high or low.

14. Synchronizer circuit which enables PE's and router to run off different clocks.

16. In data router chips, circuitry for matching between slow logic on the chip that controls the cross-bar switch and the fast logic that controls transfer of the message flits.

17. In data router chips, circuitry for performing "lookahead" in two-dimensional priority mechanism for assigning output lines in crossbar.

18. In data router system, message format for ensuring that messages are properly transmitted, using checksum. Each chip checks checksum and, if error, generates complement.

19. In data router/network interface for PE's, use and control of first-in first-out buffers for injecting messages into data router, selection of one or the other buffer for particular sides of the fat tree.

20. Performance monitor.

21. On-board clock oscillator, controlled by receipt of clock from external source.

22. Management of power distribution by processors.

23. Design patent on cabinetry.

III. Non-implemented ideas to be covered:

1. Other methods/apparatus for detecting when router is clear (other than Kirchoff counter):
   (a) sweep mechanism
   (b) acknowledgement protocol
   (c) polling mechanism

2. Circuit for interfacing between two synchronous systems, using set/reset flip-flop.

3. In data router, circuit for implementing a fast-response first-in first-out buffer using slow components (multiple first-in first-out buffers and multiplexers interconnected to form a single first-in first-out buffer.)

4. Processor alternatives