Session I

Program Overview

Welcome, Introductions,
Historical Background

H.T. Kung
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Session I

Program Overview

iWarp Development Program

Les Furnanz

Intel Corporation

Completing the iWarp Technology Vision

- **iWarp: an application–enabling technology**
- **Building blocks for most efficient parallel computing**
- **A successful collaboration of government, university, and industry**

iWarp Forum Information

- **Progress report on iWarp program VLSI and systems technology development**
- **Not a product announcement**

Program Contributions

DARPA with Navy SPAWAR

- **Program direction and monitoring**
- **Funding**
- **Vision of application futures**

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- **Architectural concept, evolution, and validation**
- **Technology feasibility and applications (Warp)**
- **Software models, tools, and prototyping**
- **Detailed technical review**
- **Approximately 150 man years (1984 – 1990)**

Program Contributions

Intel

- **VLSI architecture and implementation**
- **Hardware and software systems**
- **Software development environment**
- **System production and support**
- **Approximately 200 man years (1986 – 1990)**
- **Funding**

Running an Effective Program

- **Solid contracted quarterly payable milestones**
- **Flexibility to reflect project needs and opportunities**
- **Dedicated on–site Intel interface at CMU**
- **Constant design collaboration and review**
- **Separation of project responsibilities**
  - CMU: SW prototyping, applications, and performance evaluation
  - Intel: VLSI and systems implementation

Running an Effective Program

- **CMU development of previous Warp system** (solid concept and experience)
- **Intel development and investment beyond contract**
- **Trust built up over long–term**
- **Periodic program status reviews**
  - Monthly between Intel and CMU
  - Semi–annually with DARPA and SPAWAR

Major Program Accomplishments

- **Macro–architecture specification and simulator**
- **Architecture validation and evaluation**
- **Micro–architecture simulator and cross–validation**
- **VLSI design and mask database**
- **HW and SW systems prototypes** (awaiting first silicon)

Remaining Program Milestones

- **10–cell prototype: Q4/89**
- **64–cell prototype: Q2/90**
- **64–cell final versions: Q4/90**
- **Additional systems modules and development software**

Major iWarp Improvements from Contract Specification

- **2–D torus topology**
- **Increased modularity and configurability**
- **Large–grained and fine–grained computing integration**
- **Multiple logical connections**
- **Clock speed–up**
- **Standard languages: C, FORTRAN**
- **VME–bus interface and Unix remote I/O interface**
- **Simplified external interfacing**

Strong collaboration between Intel and CMU resulting in powerful, flexible parallel building blocks

Realizing the iWarp Applications Potential

Opportunities for collaboration and partnership

- **Tools development**
- **Applications development**
- **Systems and interface development**
- **Integration and application services**

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Program Overview

iWarp System

Developments

George Cox

Intel Corporation

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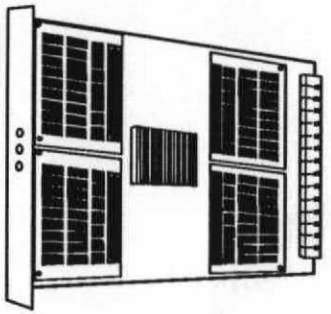
iWarp System Developments

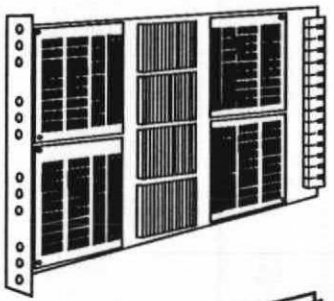
George Cox
Intel Corporation

iWarp System Building Blocks

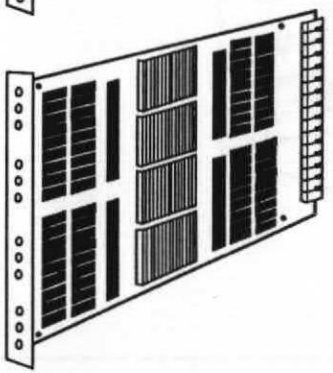
Single Cell Board
6MB/Cell



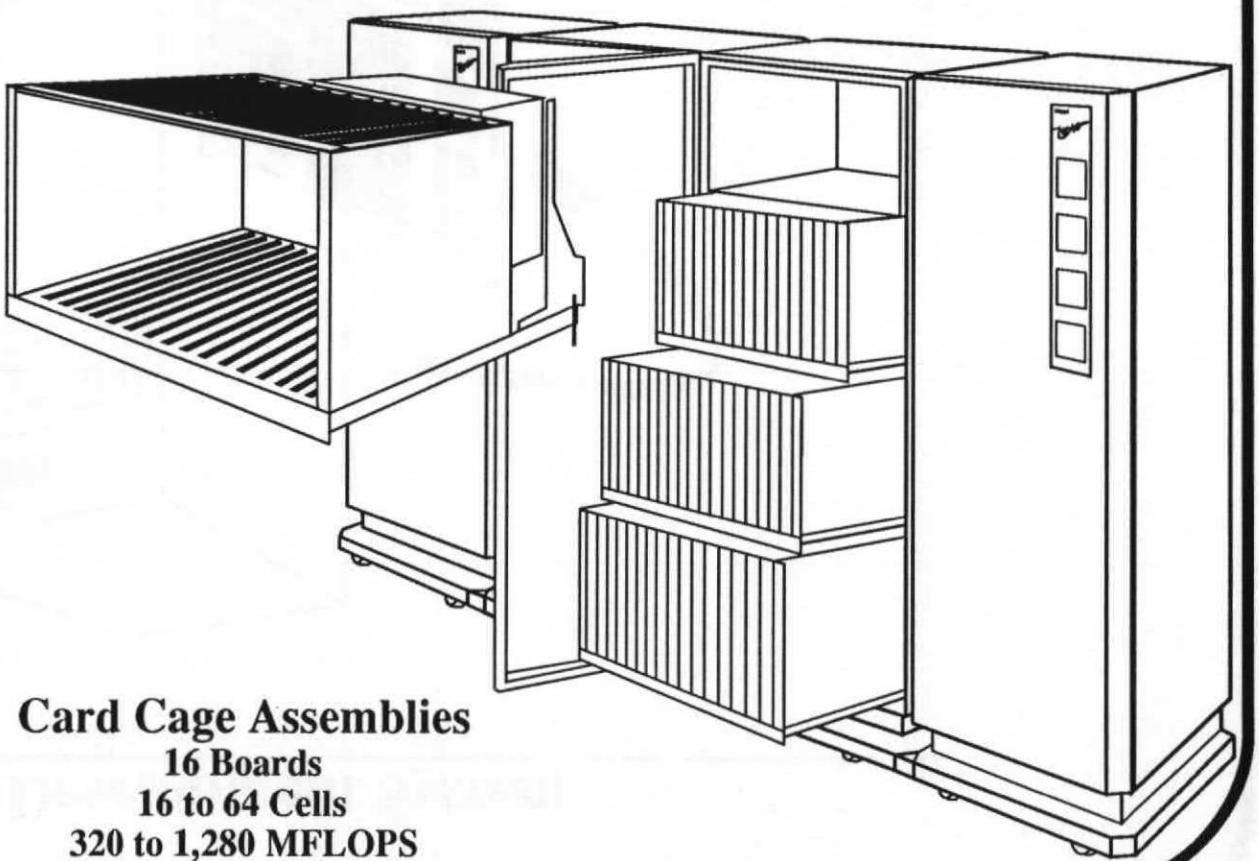
Quad Cell Board
1.5 MB/Cell



Quad Cell Board
.5 MB/Cell

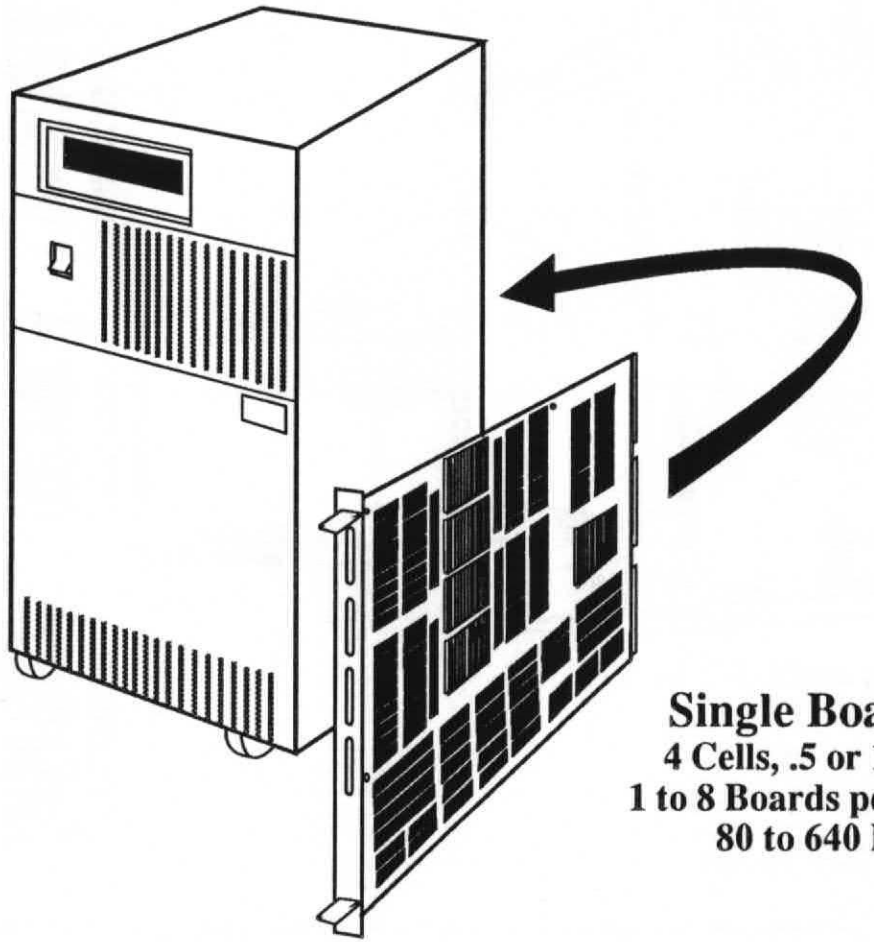


Fully Configured Systems
1 to 4 Card Cage Asm. per Cabinet
1 to 4 Cabinets per System
64 to 1024 Cells
1,280 to 20,480 MFLOPS



Card Cage Assemblies
16 Boards
16 to 64 Cells
320 to 1,280 MFLOPS

Development System



Single Board Array
4 Cells, .5 or 1.0 MB / Cell
1 to 8 Boards per Workstation
80 to 640 MFLOPS

Summary of iWarp Array Features

- **System expansion capacity**
  - Up to 256 iWarp Cells connected in a 2-dimensional array per container
  - Expandable to 4 containers (1024 Cells)
  - Multiple interface ports per array are supported
- **Memory performance and capacity per Cell**
  - 160 MBytes/sec access rate
  - 512K-1.5MBytes SRAM per Quad Cell Board
  - 1.5M-6MBytes of SRAM per Single Cell Board
- **Computation performance per Cell**
  - 20 MIPS (20-100 MOPS)
  - 20 MFLOPS (32-bit)
  - 10 MFLOPS (64-bit)
- **Communication data rates**
  - 320MBytes/sec per Cell (8 pathways/cell)
  - 40 MBytes/sec per I/O interface

iWarp Program Development Environment

Supported on SUN

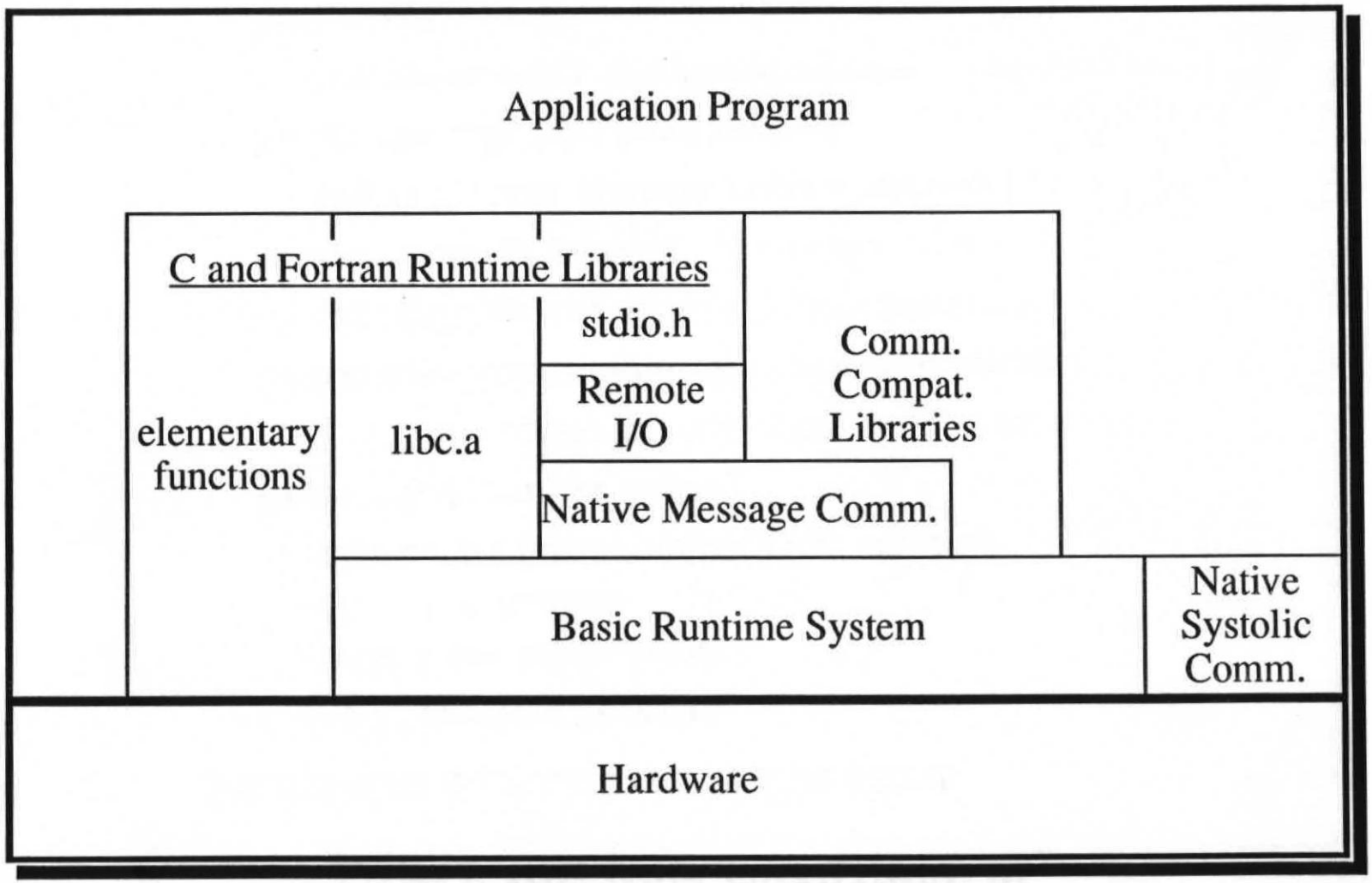
- **Compilers:** C and F77
- **Assembler**
- **Linker:** Cell and Array
- **Loader**
- **Debugger**
- **Diagnostics:** system level

iWarp Runtime Environment

Supported on Each Cell, Host & File Server

- **C & F77 runtime libraries**
  - stdio.h (eg. fopen, fclose)
  - libc.a (eg. malloc)
  - elementary function library (eg. sin, cos)
- **Remote I/O runtime library**
  - UNIX I/O equivalent (eg. open, close, read, write)
- **Communication compatibiltiy protocol support**
  - (eg. iPSC model, sockets model equivalent)
- **Native "message passing" protocol support**
  - (eg. datagrams, streams, request/response)
- **Native "systolic" protocol support**
  - (eg. gatebinding, spooling/streaming, word-level sync)
- **Basic runtime system support**
  - (eg. multi-threaded scheduling, low latency mailbox-based buffering/scheduling, low level memory mgt, timer mgt and event mgt)

Cell Kernel Structure



Apply—Application Specific Development Tool

- **Local operator computation model for 2-dimensional problems**
- **Programmer declares the size of the array(s)**
- **Programmer defines the local operator to be "applied"**
- **User is isolated from detailed data movement**
  - Operates on contiguous segments of the data array
  - Compiler coordinates data movements and distributes computational processes
  - Typical application is picture to picture processing
- **Primary program development tool for Autonomous Land Vehicle (ALV) program**

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High-Performance Computing at DARPA

Stephen Squires
Defense Advanced Research
Projects Agency

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Summary Comments

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