Session III

Component Architecture and Technology

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iWarp Forum '89 - Session III

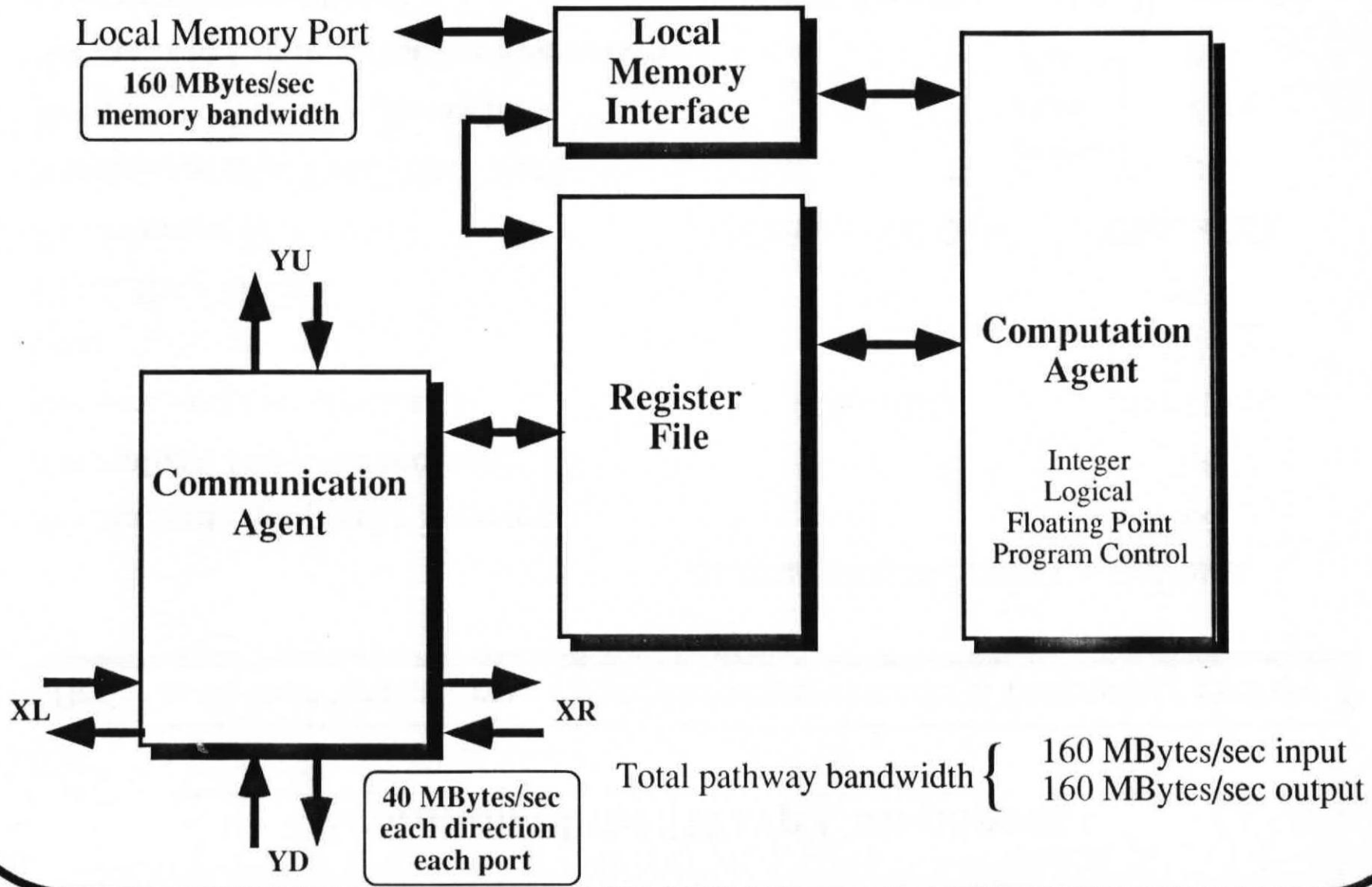
- Evolution of iWarp Component
- iWarp Component Overview
- Instruction Set
- Microarchitecture & Features
- Technology Update

Evolution of the iWarp Component

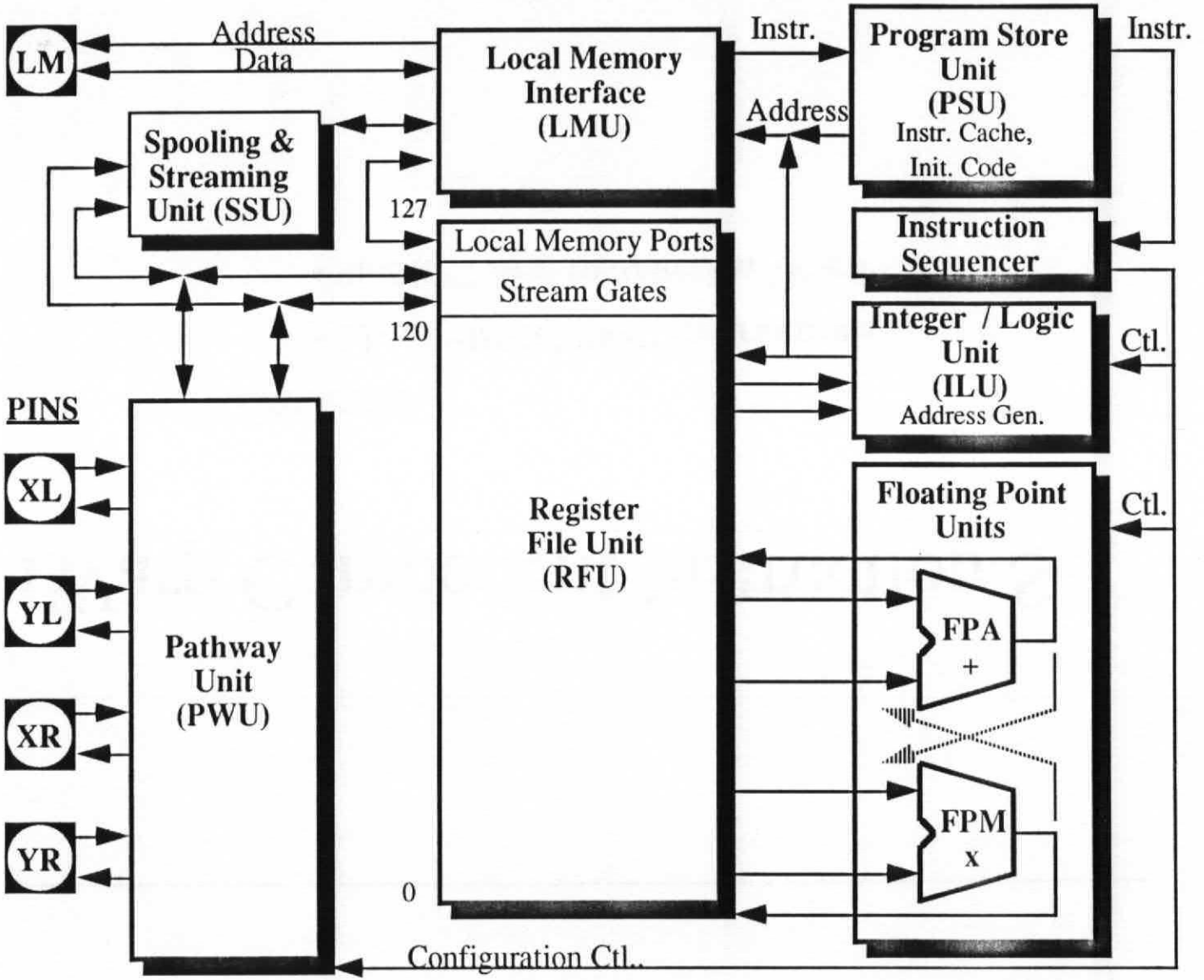
Desire for the Best System drove Consistent Improvements as Technology Evolved.

	At Beginning of Project		Today
Normalized Complexity Increase	1		3.6
Normalized Die Area Increase	1		1.8
Die Size mils sq. (mm sq.)	408 (10.4)		551 (14.0)
Pins	208		271
Clock Rate (Mhz)	16		20 +
Environmental	Commercial Only		Com. + Mil.
Normalized Dbl. Prec. Math Perf.	1	Same Clock Rate	2
Normalized Memory Bandwidth	1		2
Normalized Communication Bandwidth	1		2
Communication Models	1 D, Systolic		1D, 2D, Systolic, Msg, +

iWarp Component Overview



iWarp Chip Block Diagram



iWarp Component Instruction Set

Two Types

- **32-bit "RISC-like" Instructions**
- **96-bit "Long Instruction Word"**

General Purpose "*RISC-like*" Instruction Summary

32-bit Instruction Format

Integer/Logical Operations	**Logical ops, Arithmetic ops, Bit ops, Shift & Rotate, Find MSB**
Floating-point Operations	**Add, Sub, Compare, Max, Min, Logb,Scale Mult, Div, Sq Root, Remainder**
Data Conversion Operations	**Integer to Floating-point, Floating-point to Integer**
Memory Access Operations	**Byte, Half-word, Word, Double-word**
Flow Control	**Call, Return, Branch, Push, Pop, Break, Enter loop (Implicit Loops), Stack control**
Extended Flow Control	**Absolute call/branch, Indirect call/branch**
Literal Loads	**Load literal**
Communication Support	**Pathway control, Spool control**
General Control	**Event control, Timer op, Pointer cntrl**

Compute and Access "*Long*" Instruction

96-bit Instruction Format

Word-1

31	30—29	28—(4)—25	24—(4)—21	20——(7)——14	13——(7)——07	06——(7)——00
J	1 1	Data Mode	FADD	B operand Reg	A operand Reg	K operand Reg

Word-2

31——————(9)——————23	22—21	20——(7)——14	13——(7)——07	06——(7)——00
Memory Control	FMUL	M operand Reg	N operand Reg	R operand Reg

Word-3

31 30	29——(7)——23	22——(7)——16	15 14	13——(7)——07	06——(7)——00
OP 1	Offset 1	Base 1	OP 2	Offset 2	Base 2

Operand for 1st Read Access **Operand for 2nd Read / Write Access**

—OR—

Word-3

31——————————————(32)——————————————00
Full ILU (Integer Logical Unit) Instruction or general Branch operation

Compute & Access Instruction Parallelism

- **20 MFLOPS Nonpipelined Single Precision**
  - + 20 MIPS Integer or Address Computation
  - + 20 Mega Word / Double Word Local Memory Accesses / Sec
  - + 20 Mega Word Transfers / Sec of input via Systolic Gates
  - + 20 Mega Word Transfers / Sec of output via Systolic Gates

  100 MOPs @ 20 Mhz

  + Implicit Loop-decrement, Test, and Branch

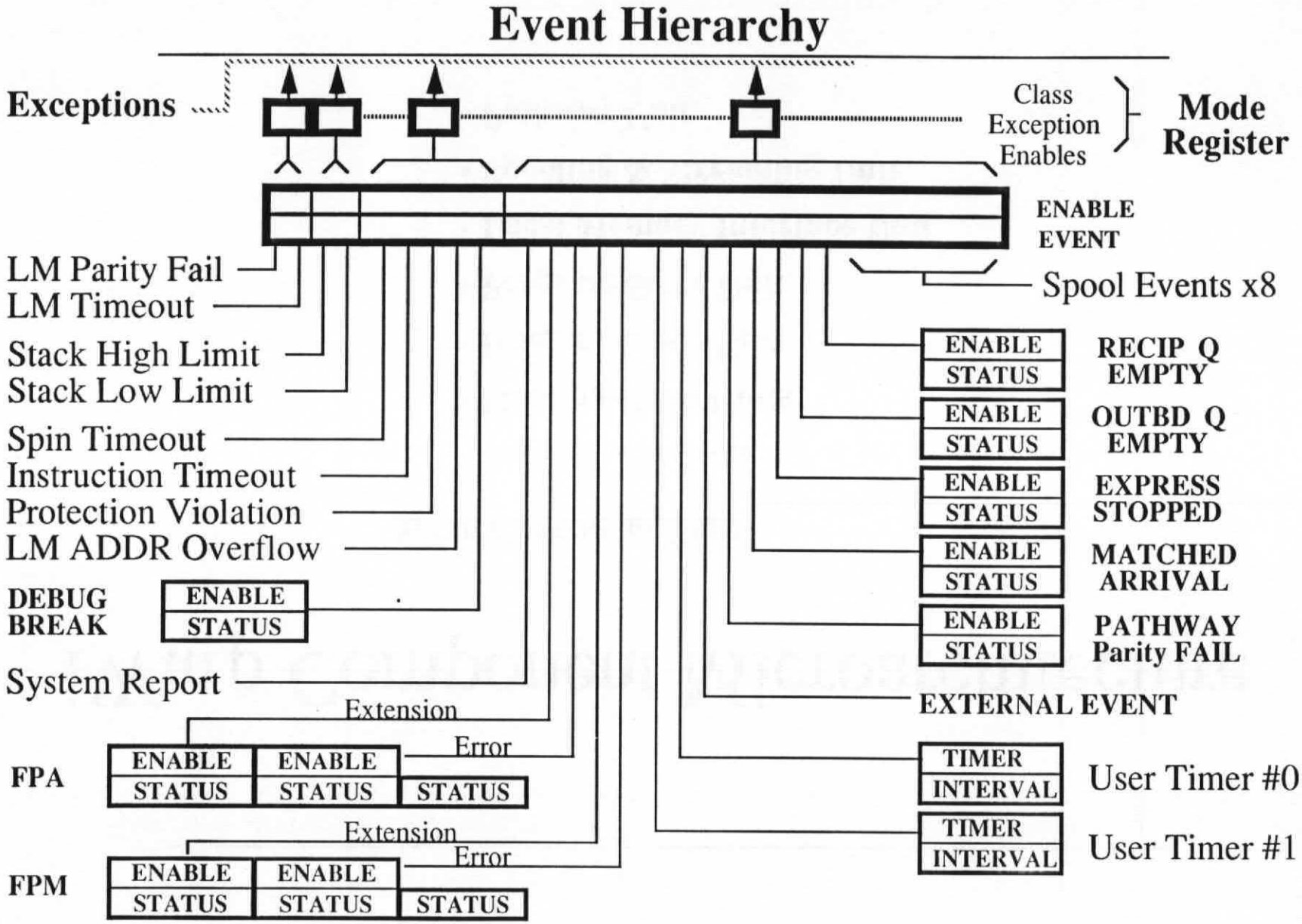
- **Nonpipelined Double Precision**

  50 MOPs @ 20 Mhz

Event Support

- **Explicit Operation via a Full Set of Condition Codes**
  - 139 Condition Codes: Event Reg, Mode Reg, State Reg, ILU Flags, FPA Flags, FPM Flags, Gate Status, Stream Tags
- **Implicit Operation via Events**
  - **Vectored Response**
  - **Synchronous** *example* **:** Stack Limit Exceeded
  - **Asynchronous** *example* **:** Matched Message Arrival

Event Hierarchy

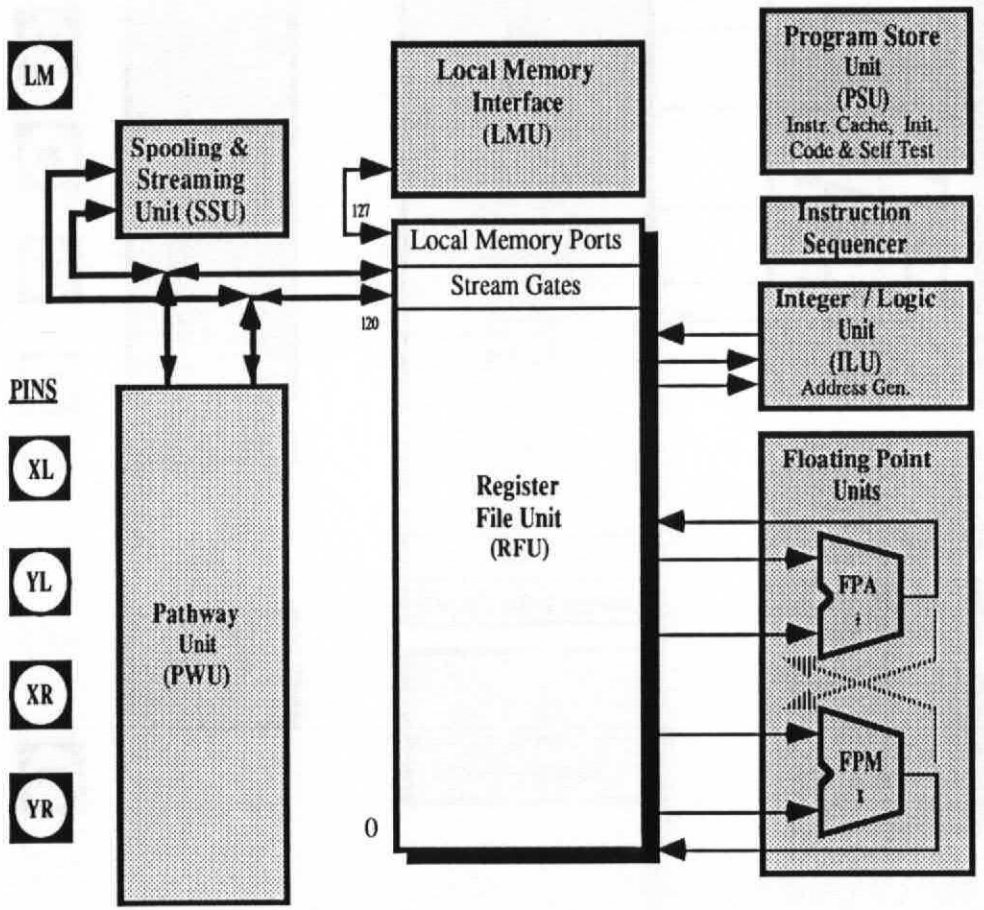


iWarp Component Microarchitecture

Seven Functional Units

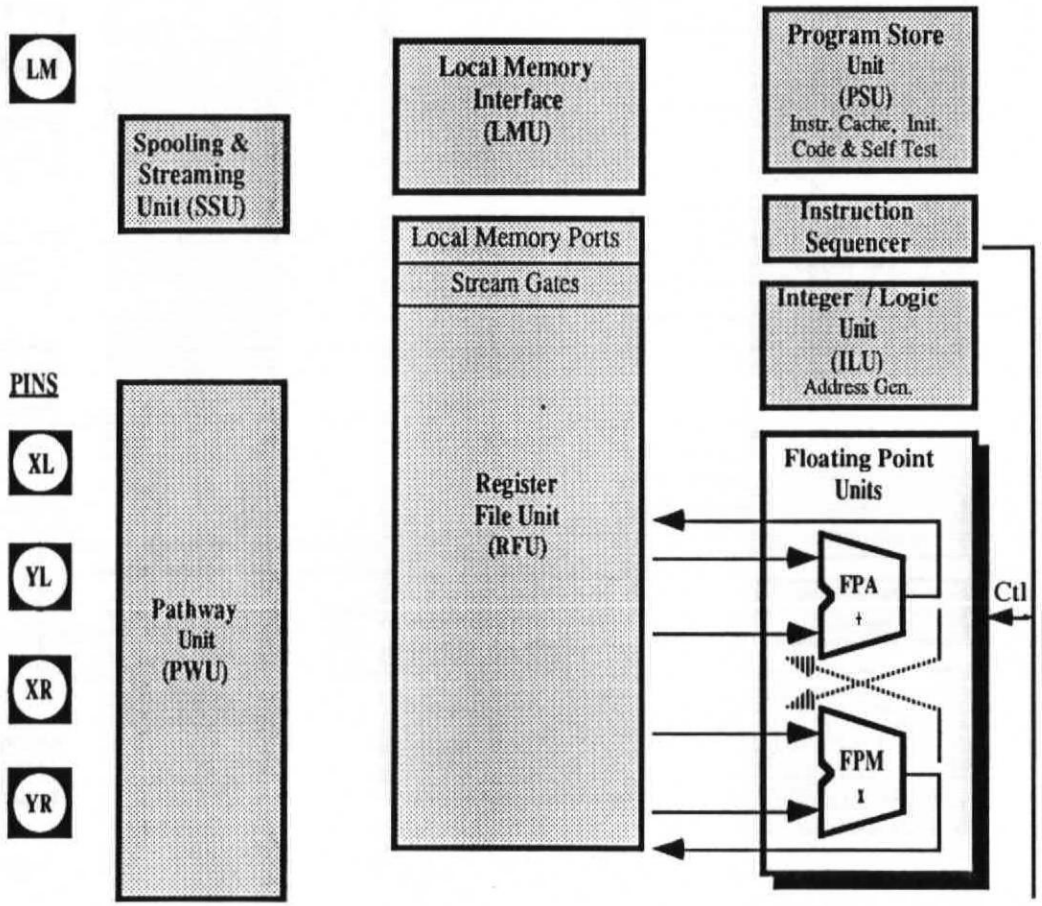
- **Register File Unit**
- **Floating-Point Units**
- **Integer / Logic Unit**
- **Program Store Unit**
- **Local Memory Interface Unit**
- **Spooling & Streaming Unit**
- **Pathway Unit**

Register File Unit (RFU)



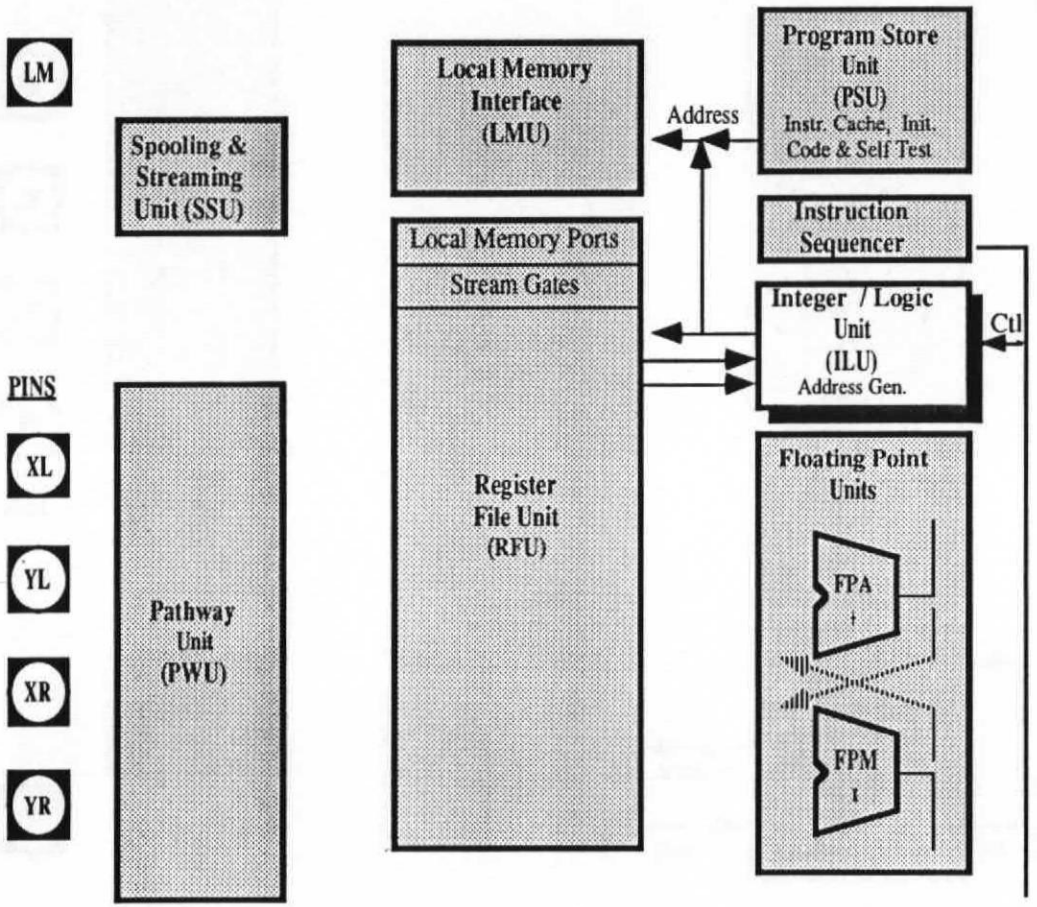
- 128 Word Register file
- 9 Read Ports, 6 Write Ports
- 800 MBytes / Sec Bandwidth
- Programmers Systolic Ports

Floating Point Units (FPA & FPM)



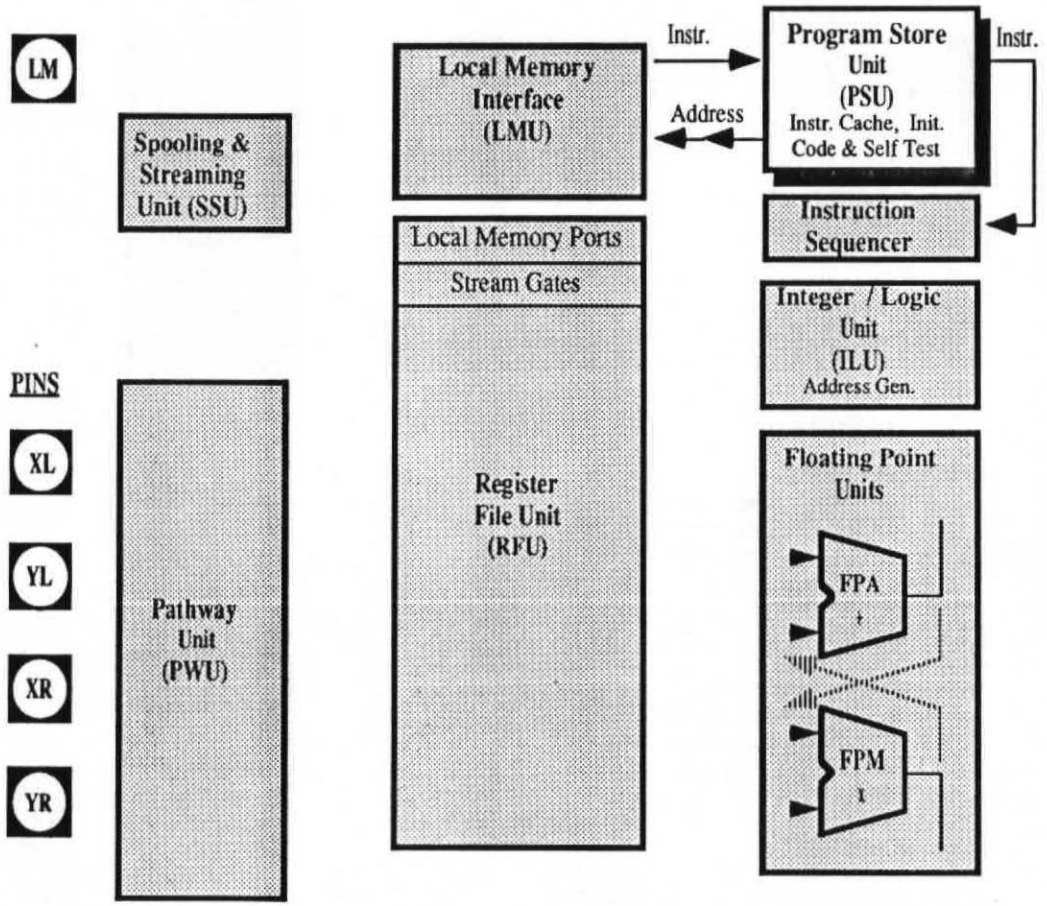
- IEEE 754 Floating Point
- Nonpipelined
- 10 Mflops FPM Single Precision
- 10 Mflops FPA Single Precision
- 5 Mflops FPM Double Precision
- 5 Mflops FPA Double Precision
- Denormalized numbers, NANs
- IEEE Exception Handling
- All Rounding Modes
- Hardware DIV, REM, SQRT

Integer / Logic Unit (ILU)



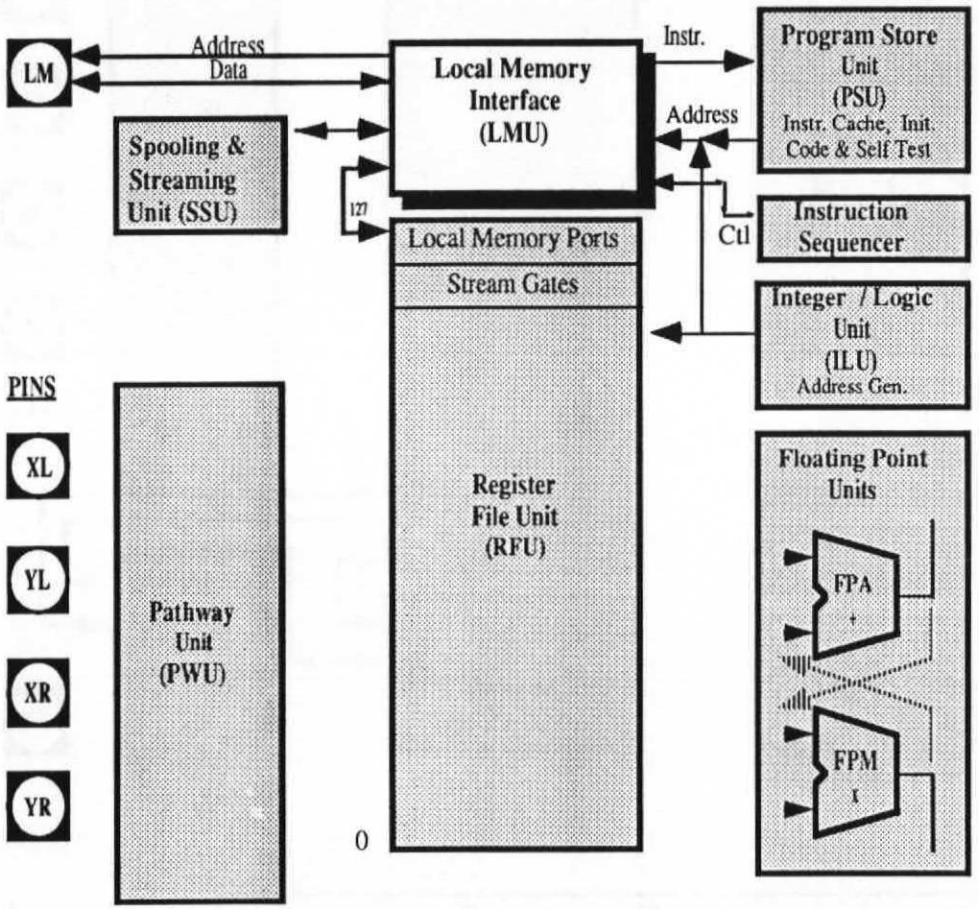
- Integers, Ordinals
- Word, Halfword, Byte
- Arith OPS, Logical OPS, Bit OPS, Shift/Rotate, Find MSB
- Address Computation
- Instruction Pointer
- Stack Pointer & Limits
- Events
- Debug Breaks

Program Store Unit (PSU)



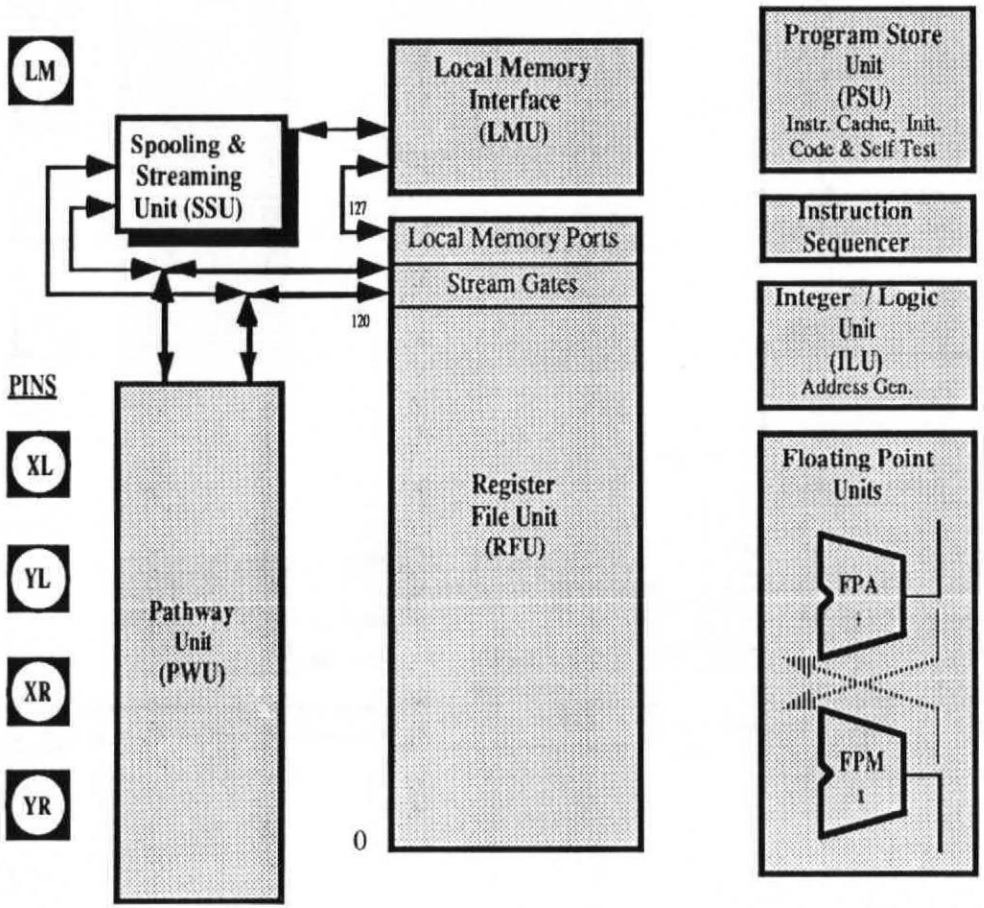
- ROM 2K words (8KByte)
  - Initialization
  - Self Test
  - LM Parity or Timeout
- Instruction Cache (1KByte)
  - 4 sectors of 4 blocks of 16 words
  - Prefetch
  - Fetch Across Blocks
  - Memory Interleaving

Local Memory Interface Unit (LMU)



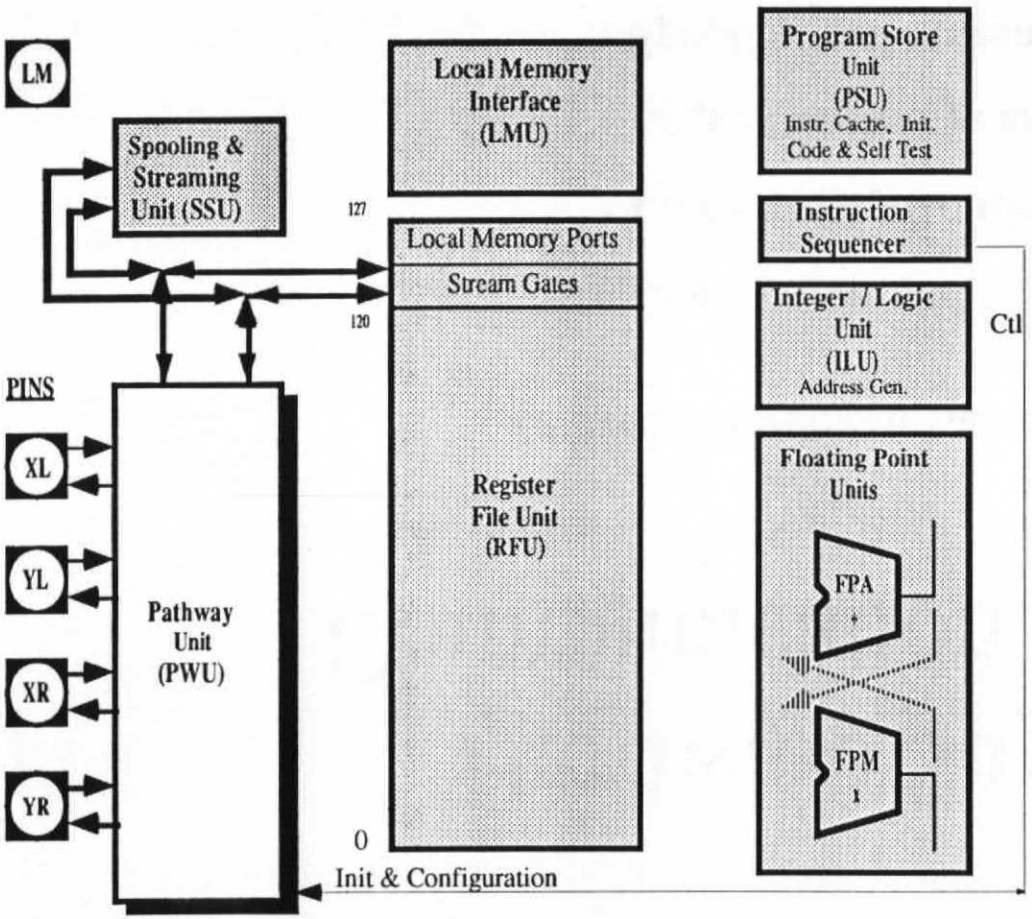
- **160 MByte/sec**
- **64 bit Data Bus**
- **64 MBytes Addressing**
- **Word, Double-word** (Direct)
- **Byte, Half-word** (Read-modify-write)
- **4 bit parity**
- **Interrupt**
- **Data, Instruction & Spooling**
- **LM Limit Checks**
- **Both Byte Ordering Stds.**
  - Big-endian (IBM, DEC-10, 68000
  - Little-endian (PDP-11, VAX, 386)

Spooling & Streaming Unit (SSU)



- 8 Spool Channels
- 4 Stream channels
- DMA from / to Logical Pathway (via cycle stealing)
- 160 MByte/sec

Pathway Unit (PWU)



- **320 MBytes/sec External Communication**
- **160 MBytes/sec to Comp. Agent**
- **1D or 2D Torus**
- **Simultaneously Supports**
  - Systolic Communication
  - Message Passing Comm.
- **System Hdw Features**
  - Compensated Pin Drivers
  - Near / Far: Cable Data Piping
  - Adjustable Input Thresholds

Hardware Supported Communication Primitives

Integrated Communications

- **Connections and Messages**
- **Low Latency Routing**
- **Logical Pathways and Buffers**
- **Spooling and Streaming**

Connections & Messages

- **A *Connection Header* reserves unidirectional routing resources from one cell to some other cell in the array – "like dialing the telephone".**
  - Contains Routing & Destination Addresses.
  - Reserves a *Logical* point-to-point communication path.
  - Guaranteed Order of Arrival.
  - Hardware allocates routing resources as it makes the connection.

- ***Messages* are like sentences that are spoken over the open line.**
  - Also has a Header and Tail.
  - The Header may contain an address used during "Party Line" operation.

- **A *Connection Tail* frees the routing resources and terminates the connection - "like hanging the telephone up".**

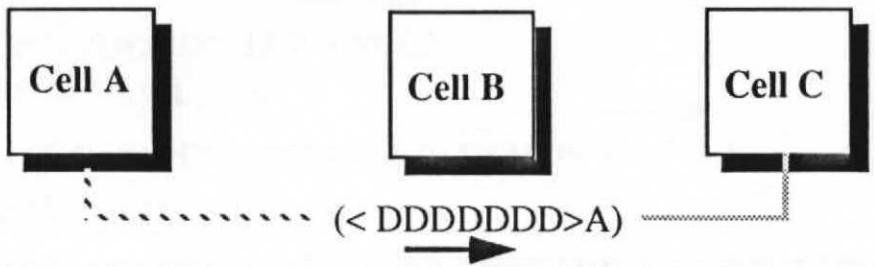
Semantics for Connection and Message Examples

(<DDDDDDD>A) →

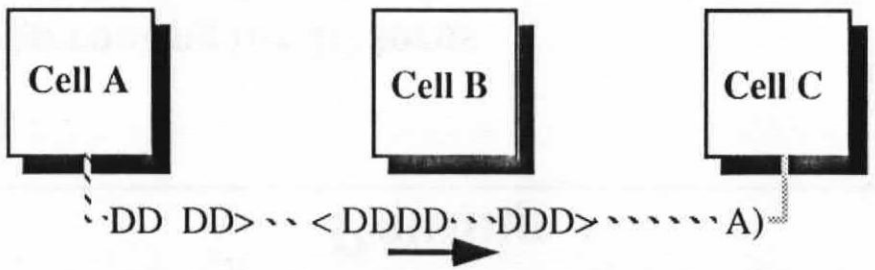
A)	Connection Header w/ Destination Address
>	Message Header
D	Data Word
<	Message Tail
(	Connection Tail

Examples using Connections & Messages

- **Message Passing** **moves a message from one cell's memory into another cell's memory — "like one person sending E-Mail to another person's in–basket".**
  - Coincident Connection & Message Header, Coincident Tails



- **Systolic** **moves data one word at a time from one cell's program to another cell's program — messages are like sentences that are spoken over the open line.**
  - The receiver listens and makes meaning of each and every word as it's spoken.
  - The connection reserves resources along the route and carries 1 or more msgs.



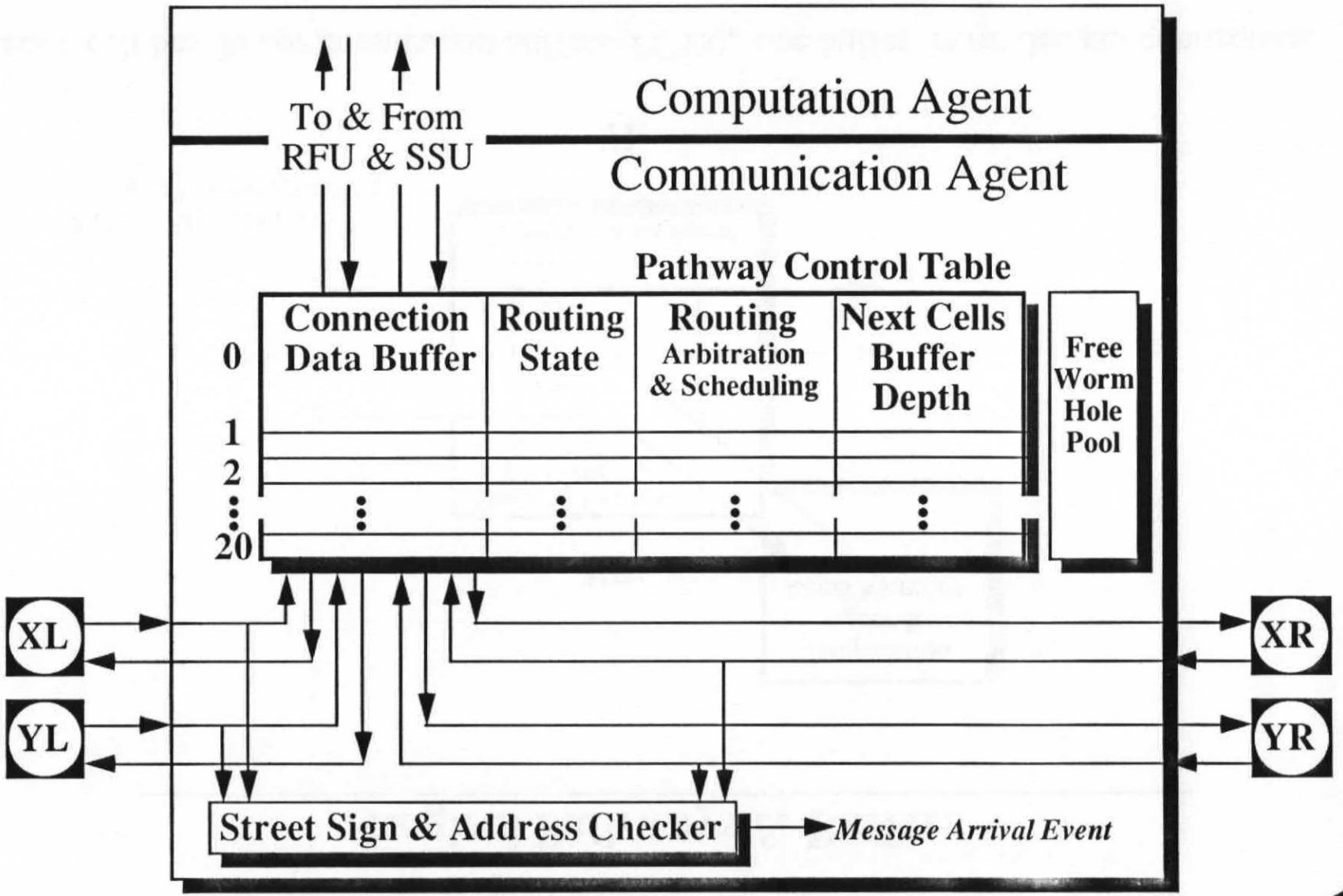
Routing

- **Streetsign routing for 2D torus**
  - "Go to Forbes, Turn Left"
    "Go to Broadway, Stop", etc.
  - One pair of "street name" and "action" in the message header for each routing step.

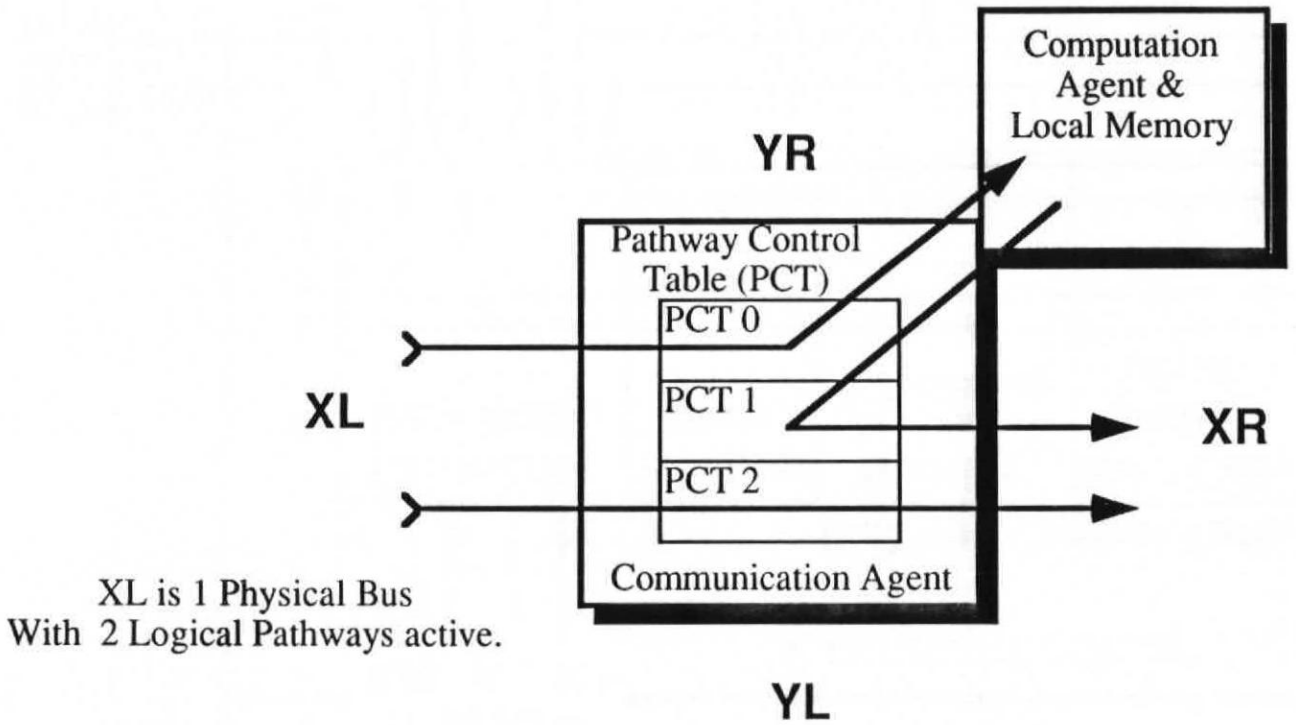
- **Turning a corner strips the route connection header**
  - Message Before Turn :
    (<DDDDDD>"Broadway")"Left on Forbes") →
  - Message After Turn :
    (<DDDDDD>"Broadway") →

- **Timing**
  - 200 nsec. to pass through a cell (250 nsec. if corner turning).
  - A Word is pipelined every 100 nsec.

Pathway Unit – Microarchitecture



Logical Pathways & Buffers

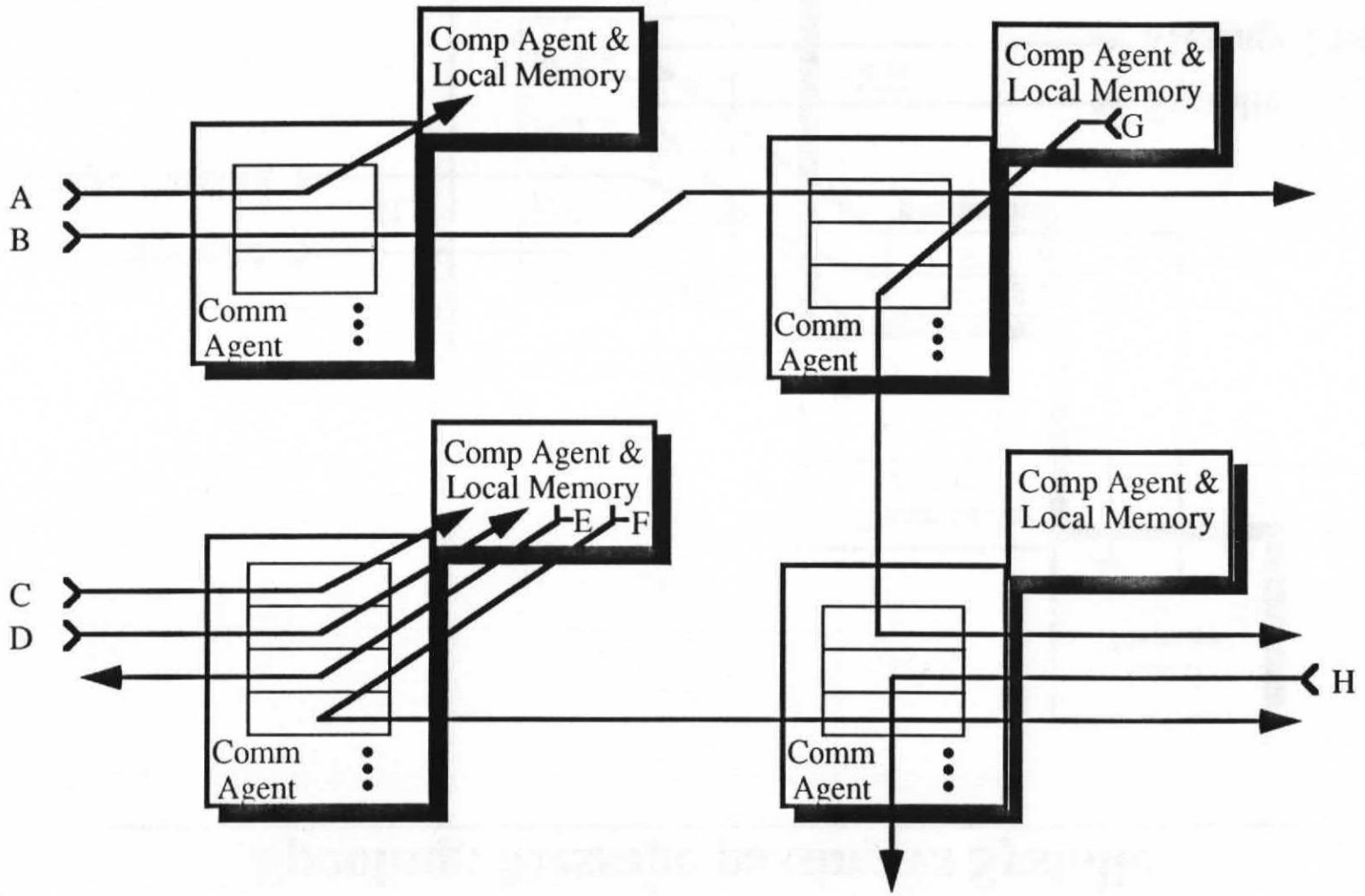


XL is 1 Physical Bus
With 2 Logical Pathways active.

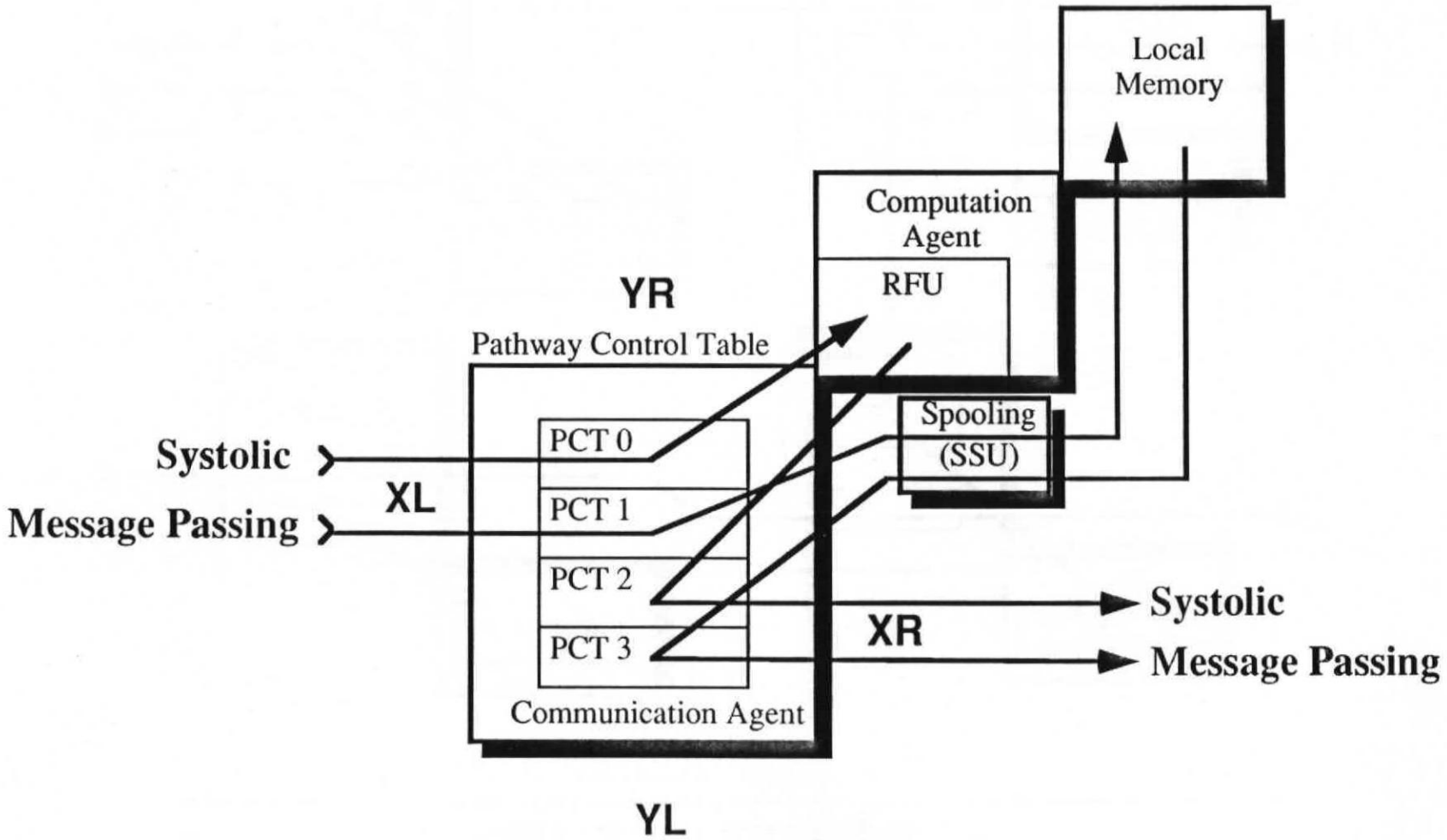
Each cell has 20 communication buffers (PCTs), one buffer is needed per connection.

Up to 20 simultaneous connections supported in each cell – 20 PCT Buffers

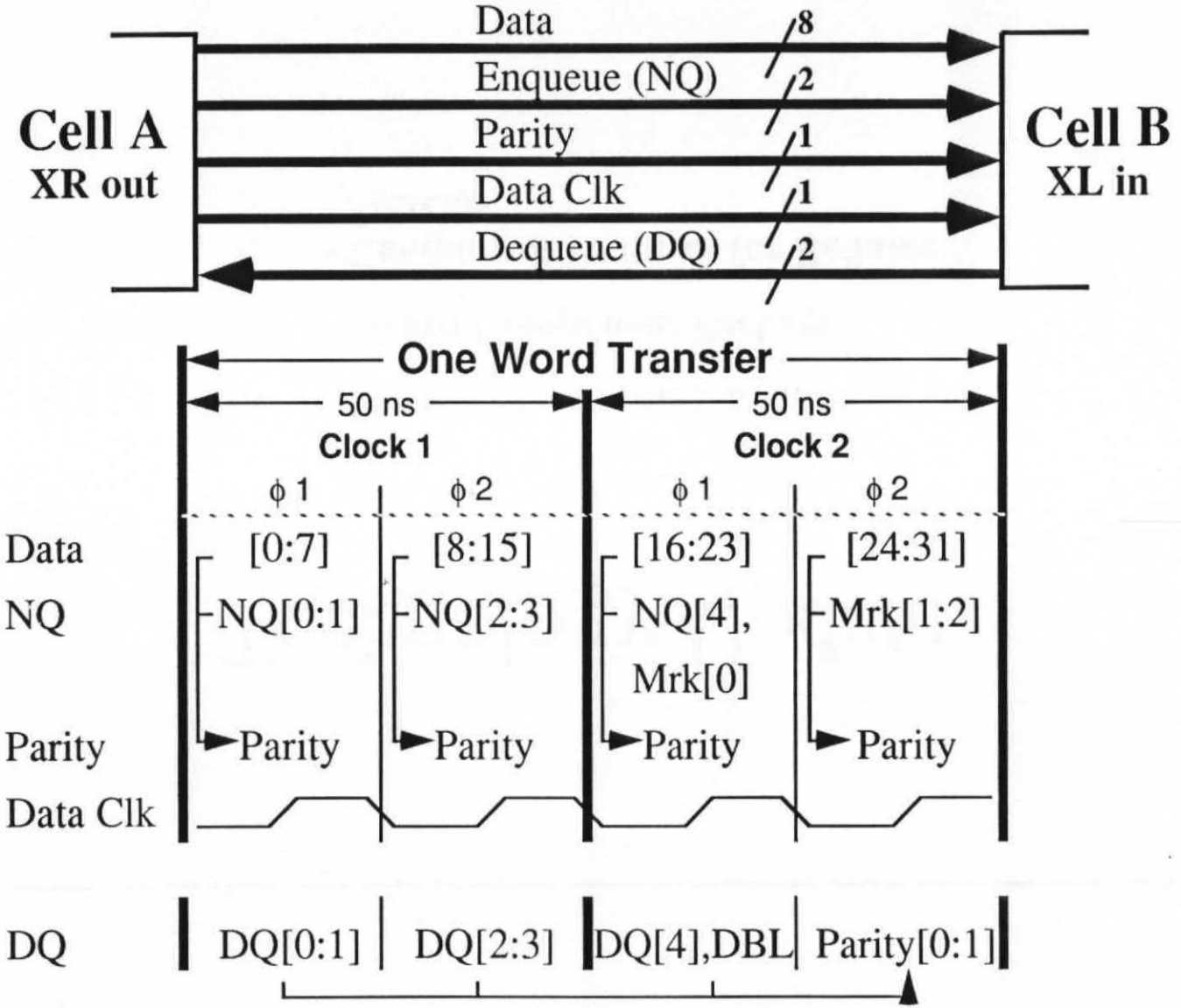
2D 2 x 2 Example



Spooling: Message passing vs Systolic



External Pathway Pins and Handshake



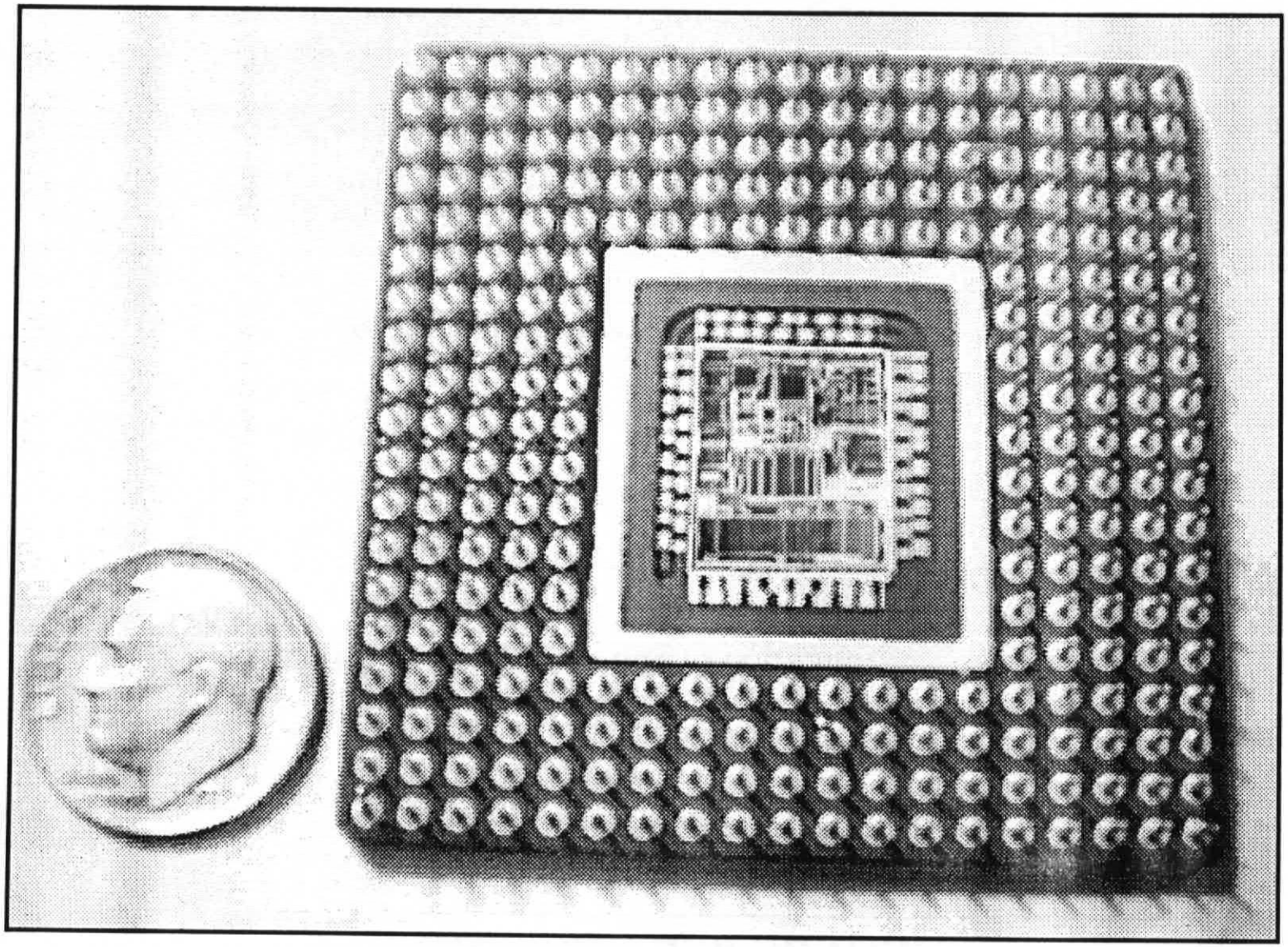
Technology Update

- **Process Status and Statistics**
- **iWarp Component Package**
- **Component Features for Reliable Systems**

Process Status and Statistics

- **< 1μ CMOS Technology**
- **Volume Production on 80486 & 80386.**
- **Environmental**
  - Commercial
  - Military 883C
  - RAD
    - iWarp not tested yet.
    - 386 on same process & similar design style.
      - Total Dose : 20 – 24 KRad
      - Approved for Space Station

iWarp Component Package



Component Features for Reliable Systems

Basic Features

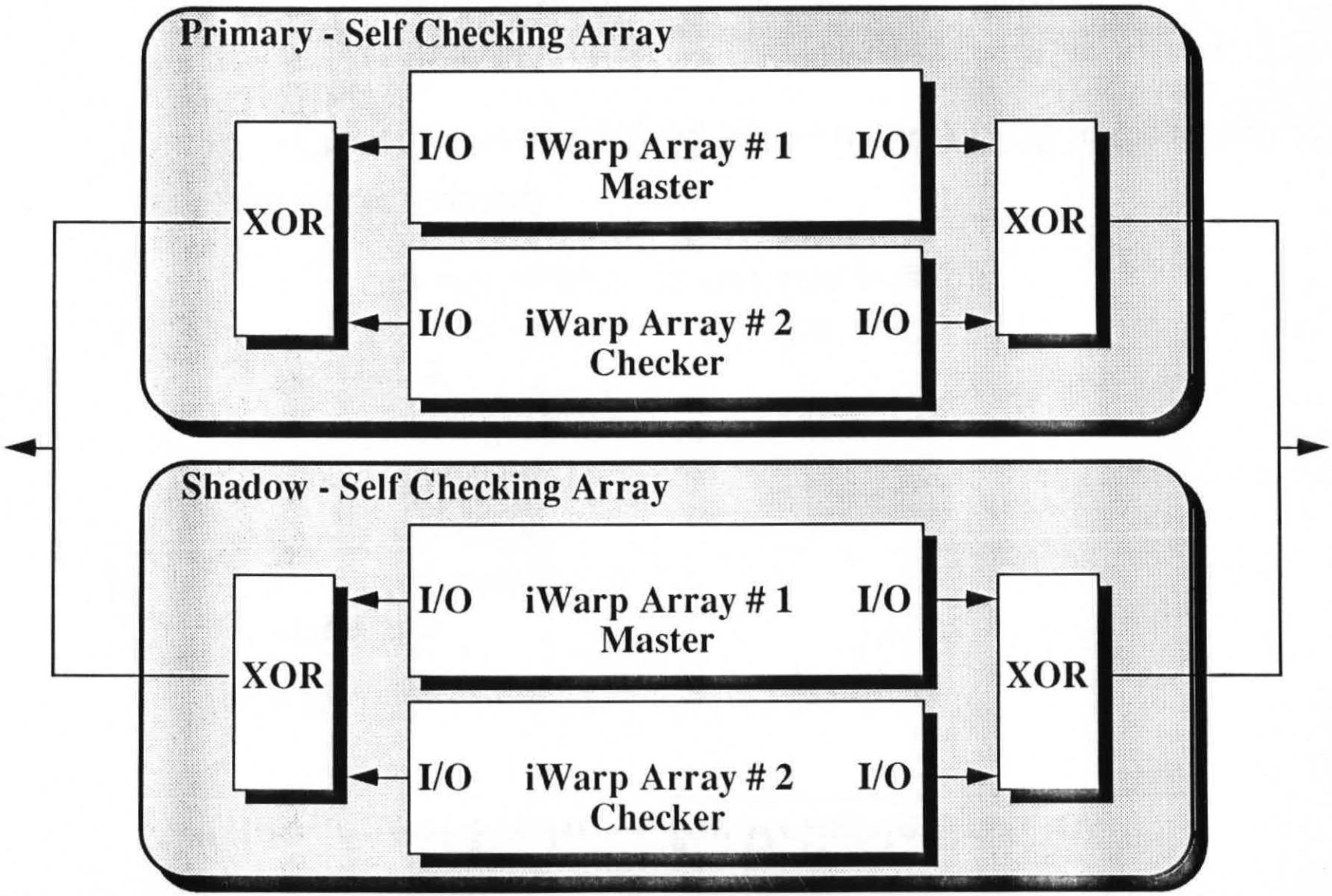
- **Detection**
  - LM Parity
  - Pathway Parity
- **Error Reporting**
  - System Reporting Unit
- **Recovery**
  - Source Routed Communication
  - Graceful Degradation via Remapping Routes

Advance Applications

- **Clock Synchronous Array makes for easy QMR at the array level.**
  - Detection : via Functional Redundancy Checking + Parity.
  - Recovery : via Array Replication & Hot Stand by

(QMR : Quad Modular Redundancy)

Array Level QMR



Component Summary

- **Significantly Exceeded Design Objectives**
- **Conventional "*RISC-like*" Instruction Set**
  + Powerful "*Long Word*" Instructions
- **Register File Based**
- **High Performance Delivered by High Degree of Parallelism Inside Component**
- **Powerful Integrated 1D or 2D Mesh Communications Unit**