Session V

System Hardware Technology

Dick Hofsheier
Intel Corporation

iWarp Hardware Session V

- **Hardware System Configurations**
- **Interfacing to iWarp**
- **Design Aspects**

Dick Hofsheier

Intel Corporation

Hardware System Configurations

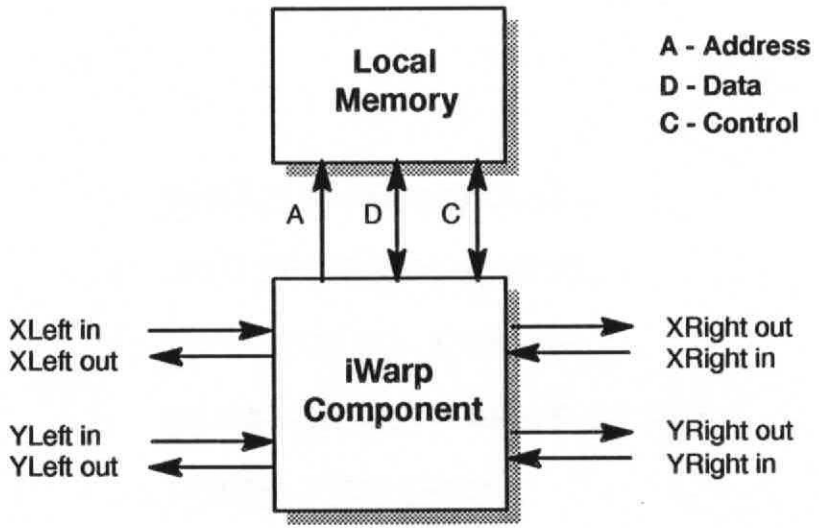
System Features

- **2–d Extensible Array**
- **Multiple Entry Levels**
  - **Components**
  - **Boards**
  - **Cardcage Assembly**
  - **System**
- **Flexible I/O Structure**
- **40MHz System Clock**

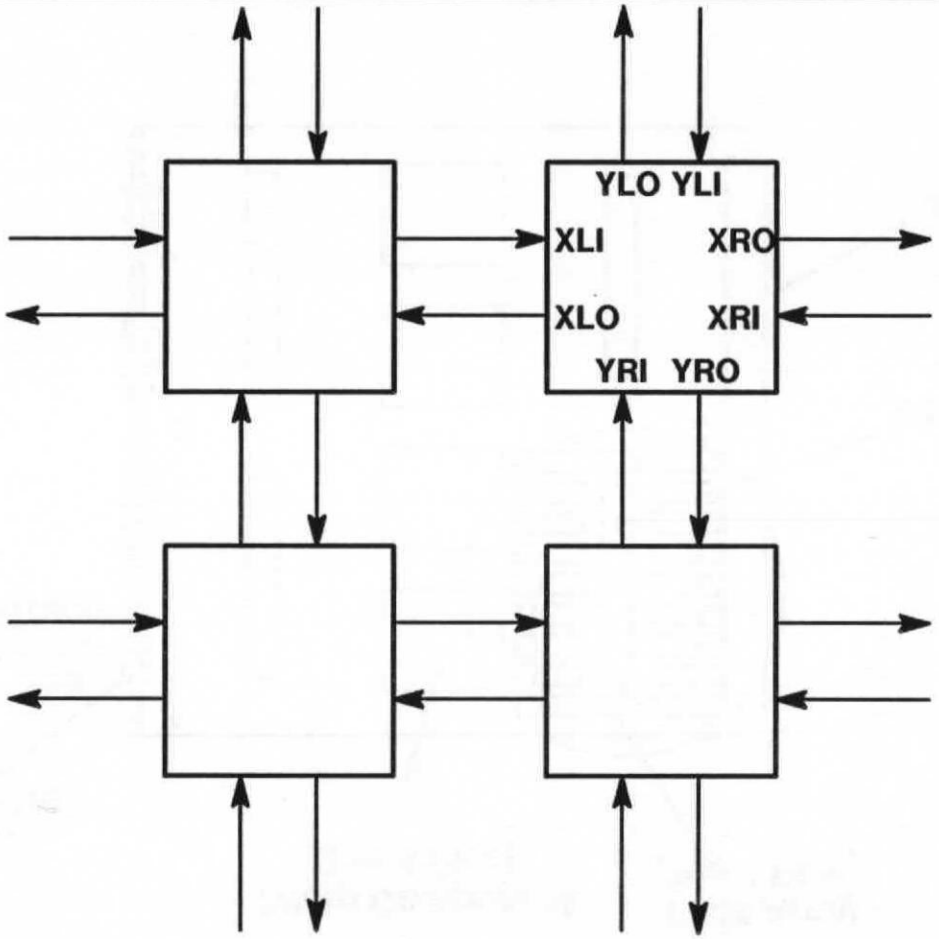
Board Building Blocks

- Quad Cell Board
- Single Cell Board
- Memory Expansion Module
- External I/F Boards
- Sun Interface Board
- Single Board Array

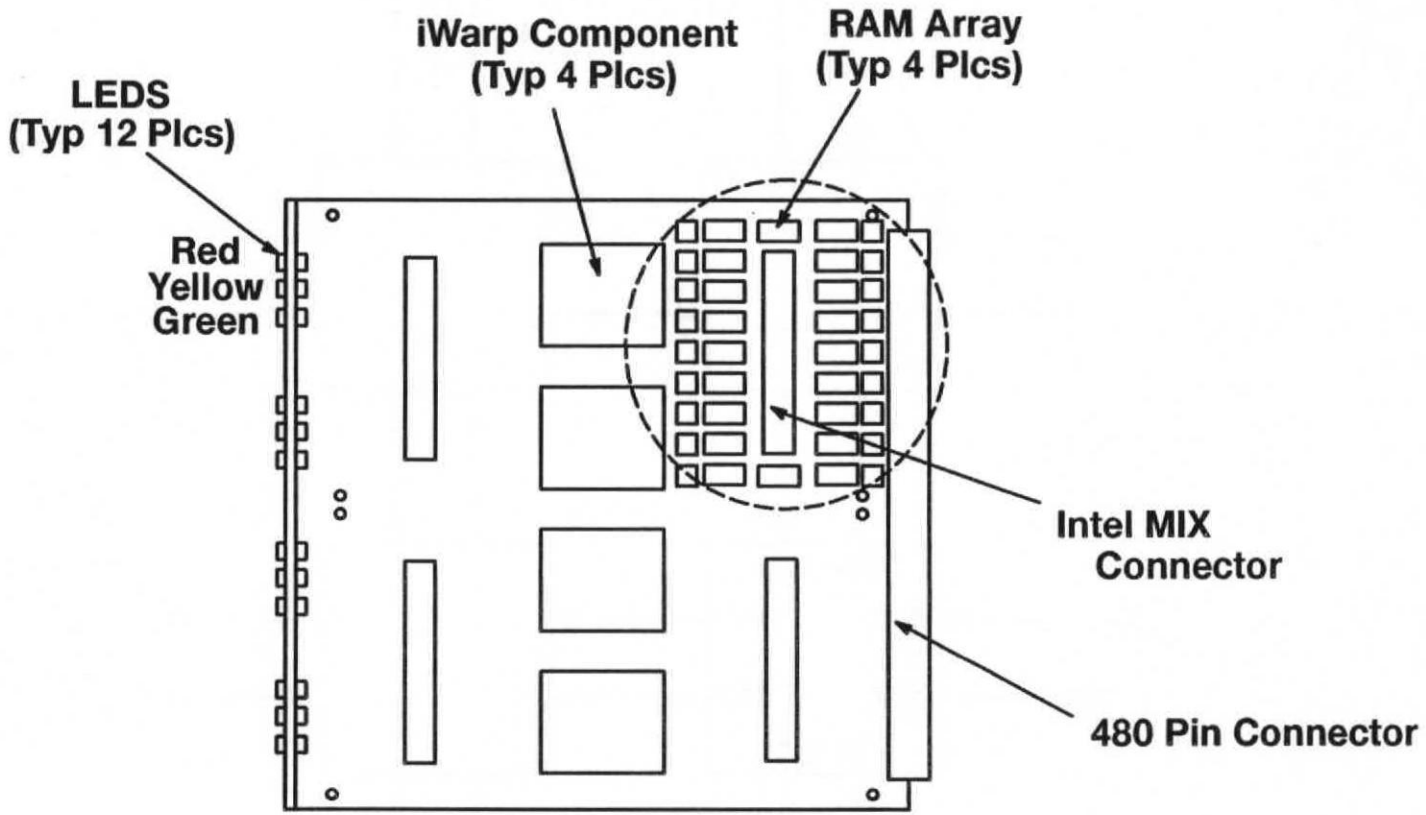
iWarp Cell


Local Memory
A - Address
D - Data
C - Control
A
D
C
XLeft in
XLeft out
YLeft in
YLeft out
iWarp Component
XRight out
XRight in
YRight out
YRight in

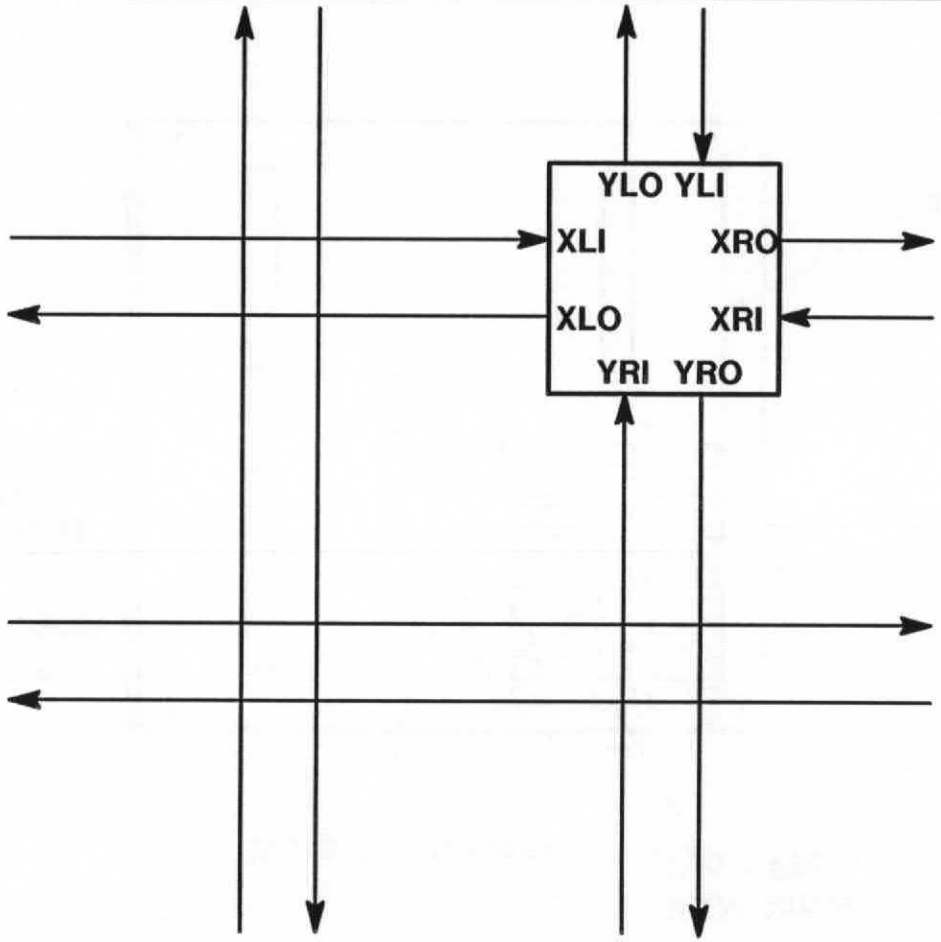
Quad Cell Configuration



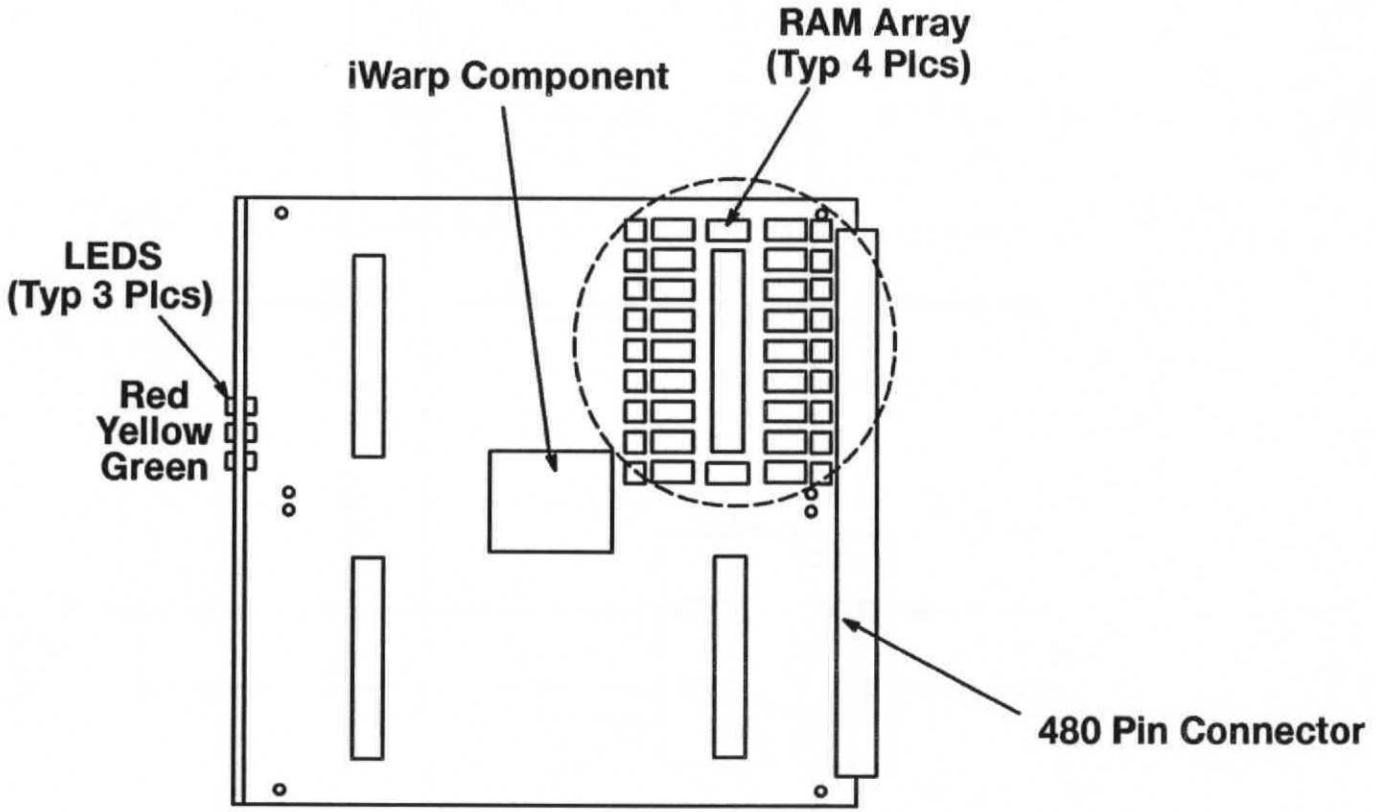
Quad Cell Board



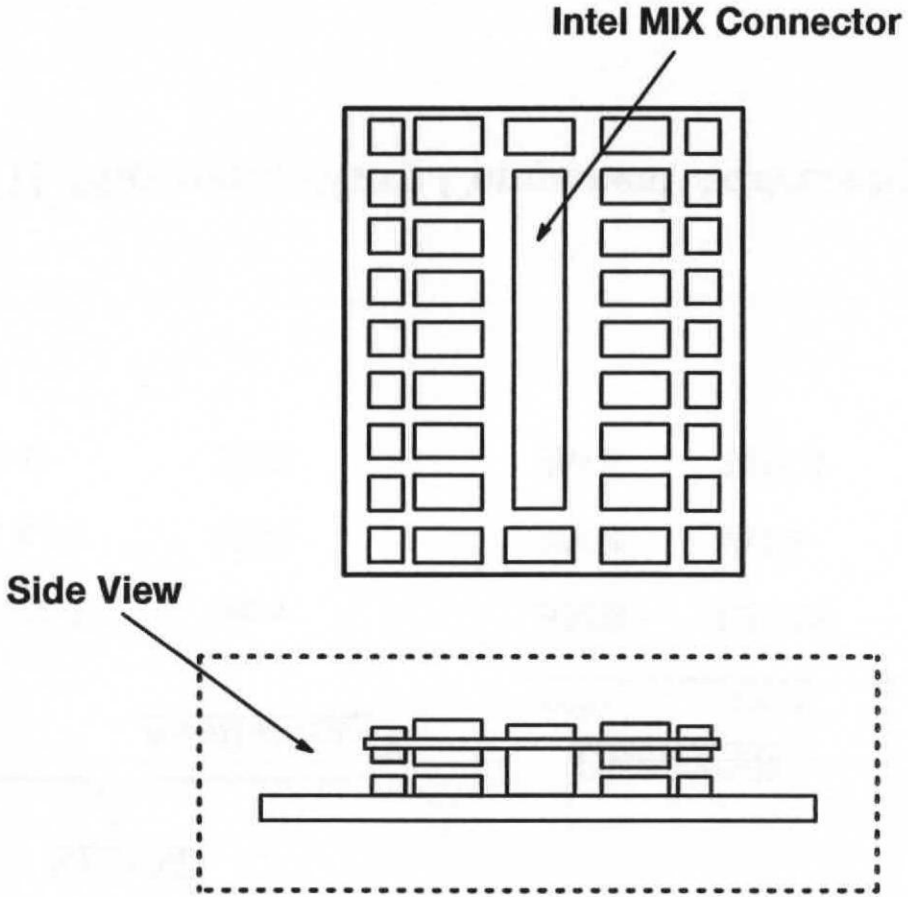
Single Cell Configuration



Single Cell Board



Memory Expansion Module

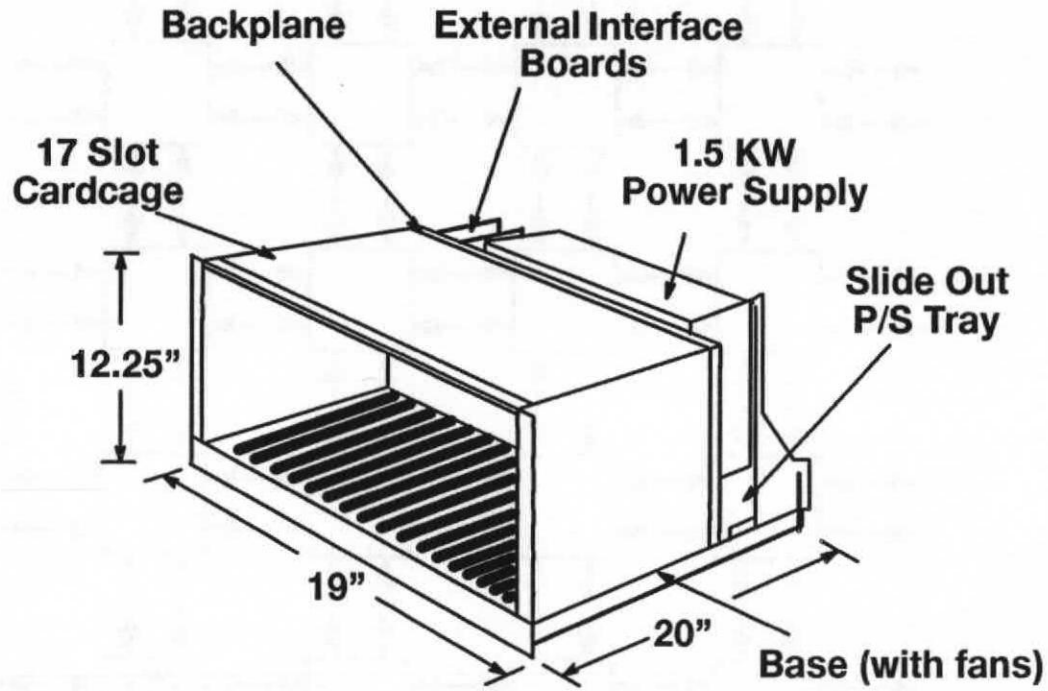


Cell Board Memory Size

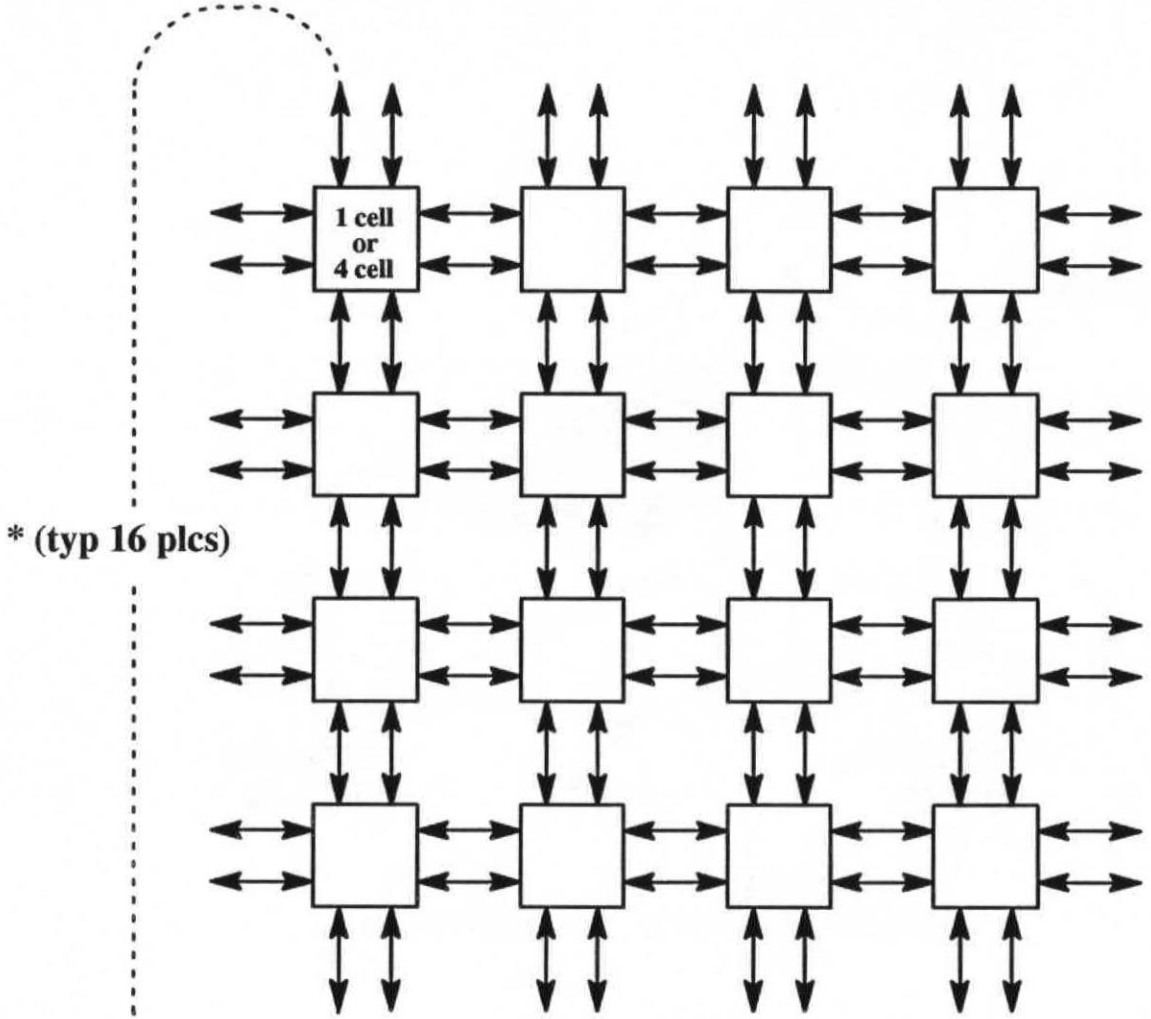
SRAM		Quad Cell		Single Cell	
Density	Availability	min	max	min	max
256K (64K x 4)	Now	.5MB	1.5MB	2MB	6MB
1M (256K x 4)	1990	2MB	6MB	8MB	24MB
4M (1M x 4)	1992	8MB	24MB	32MB	64MB[1]

Notes: [1] Maximum iWarp Component Address Space

Cardcage Assembly



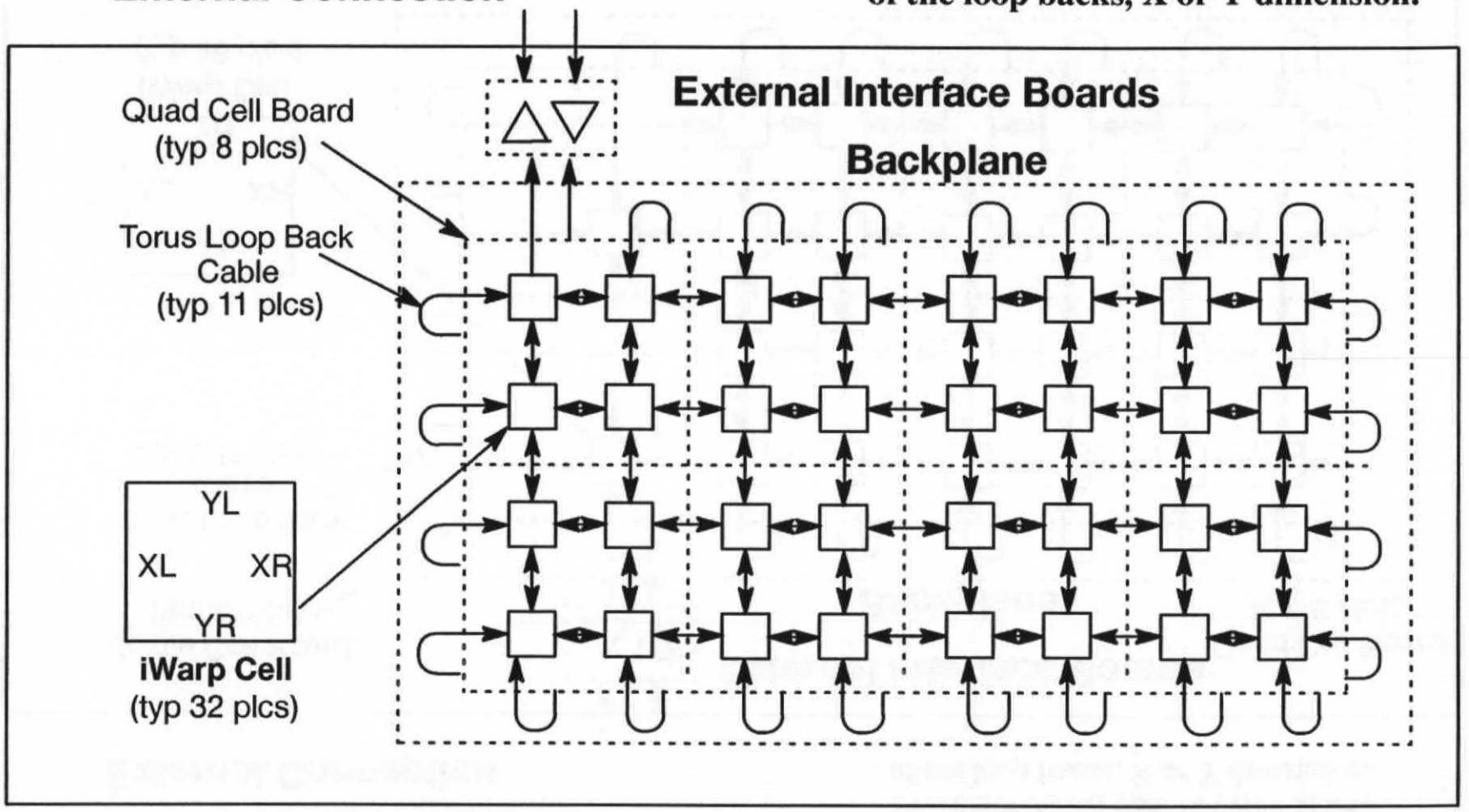
2–d Backplane Configuration



*** I/O Connections via External I/F Board or Torus Loopback**
8 x 8 Quad Cell Array (1.28GFLOPS)
4 x 4 Single Cell Array (320MFLOPS)

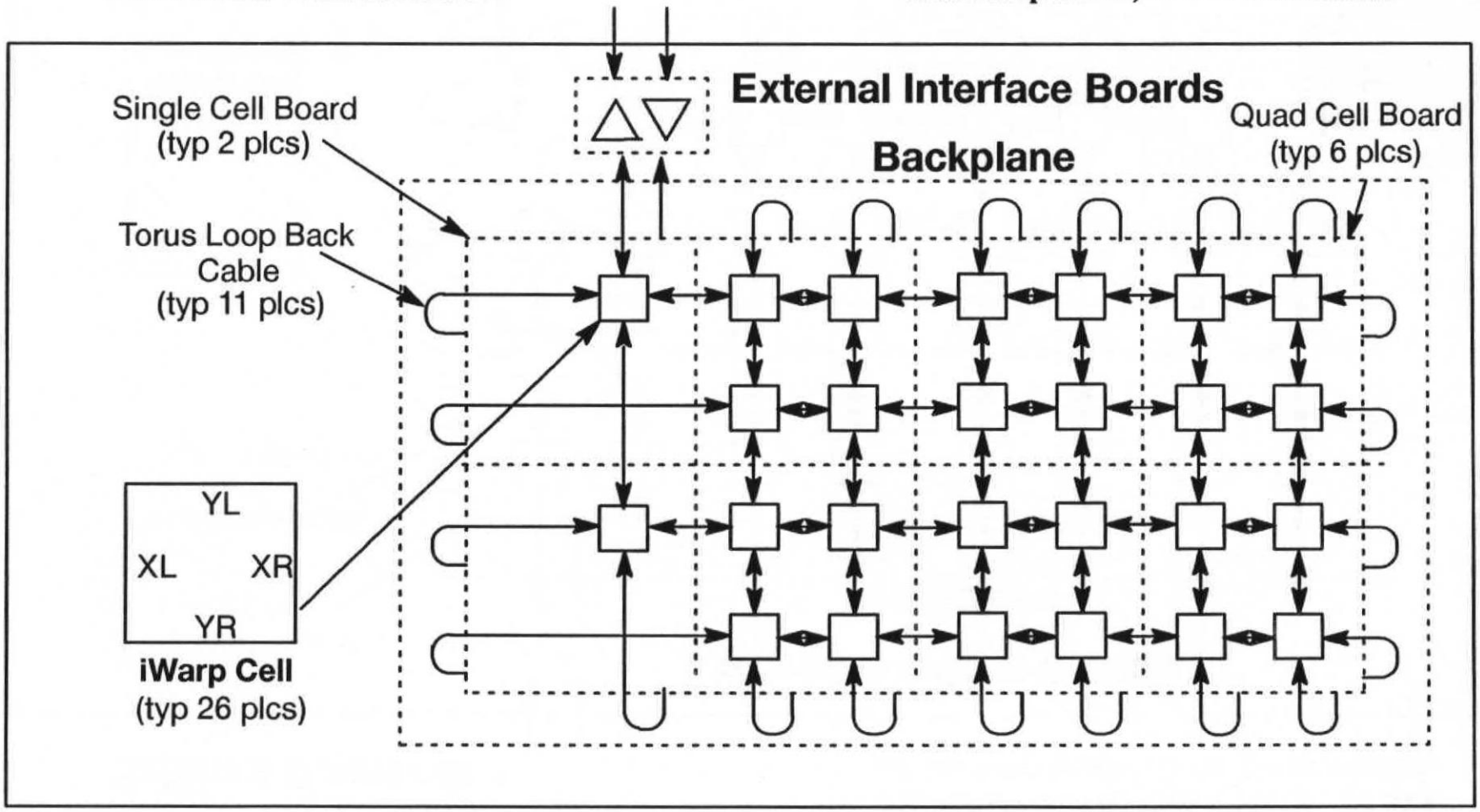
Quad Cell 8 x 4 Array

NOTE: The external connection to the iWarp Processor Array can be made at any of the loop backs, X or Y dimension.

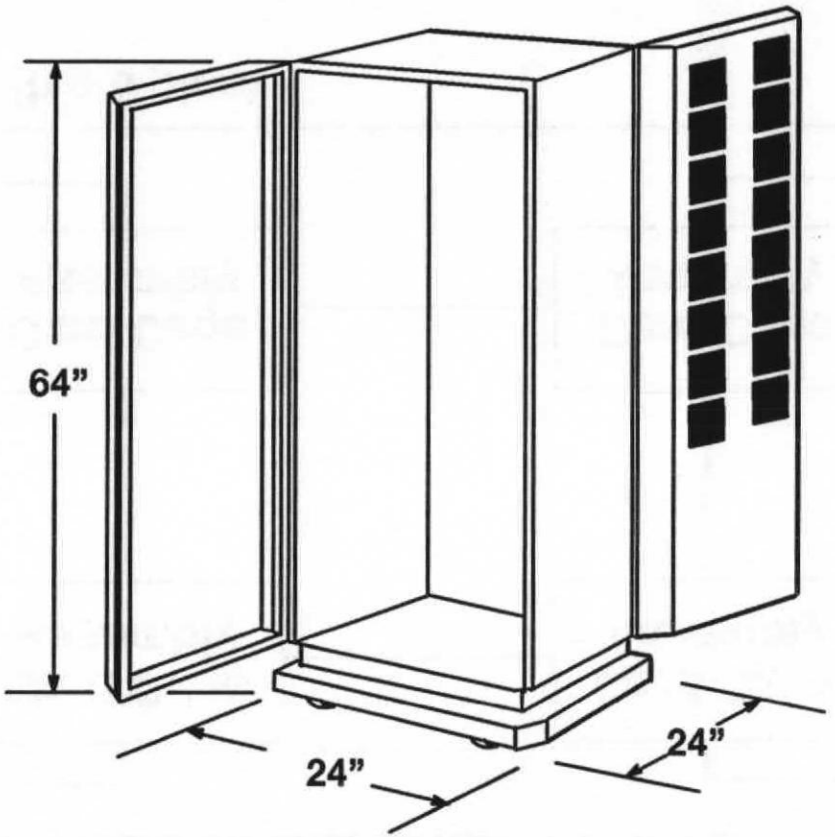


Combination Quad & Single Cell Array

NOTE: The external connection to the iWarp Processor Array can be made at any of the loop backs, X or Y dimension.

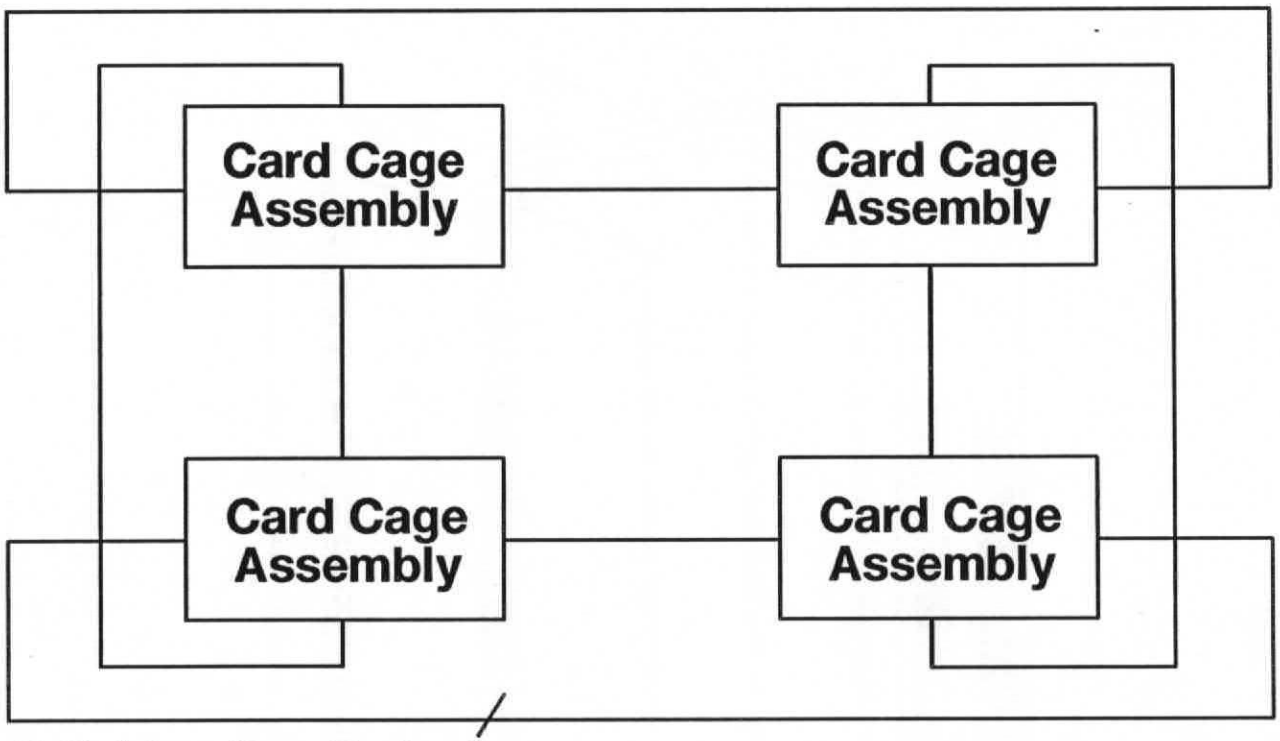


19" Container



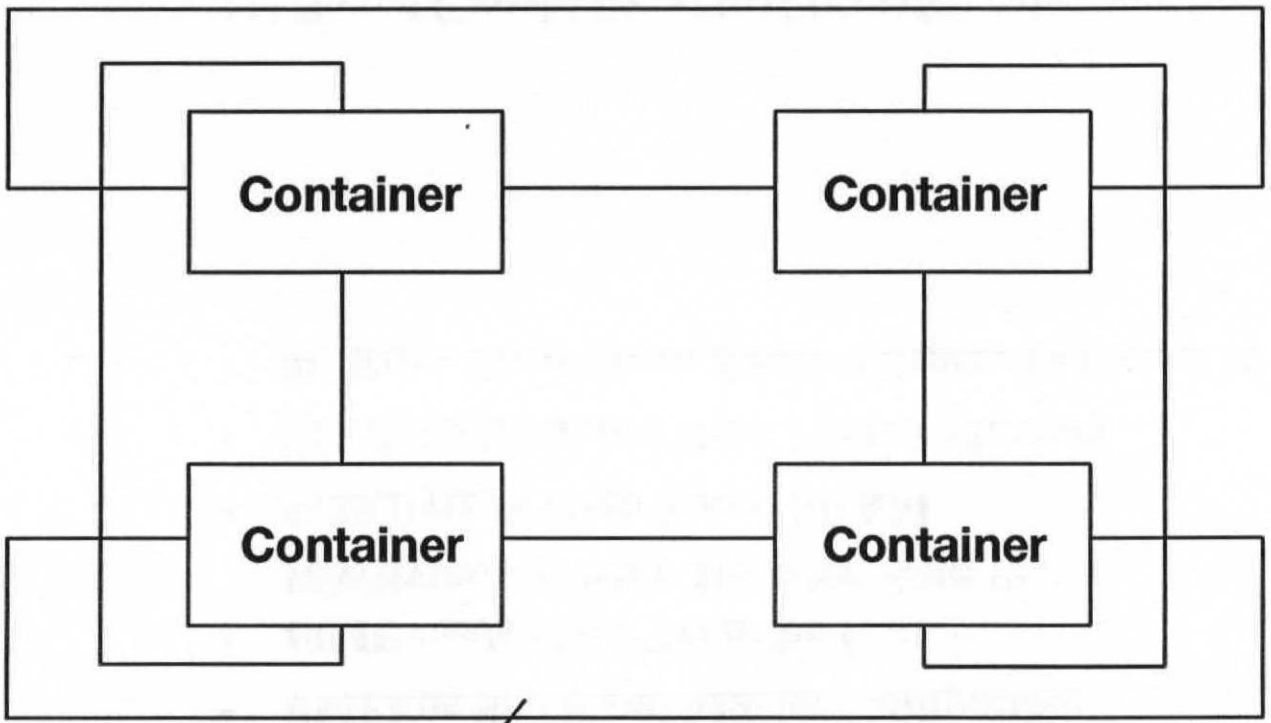
29 Rack Units (1 Rack Unit = 1.75")
5K WATTS

Max Single Container Array



16 x 16 Quad Cell Array (5.12GFlops)
8 x 8 Single Cell Array (1.28GFlops)

Max 2–d Configuration



16 Cables (typ 8 plcs)

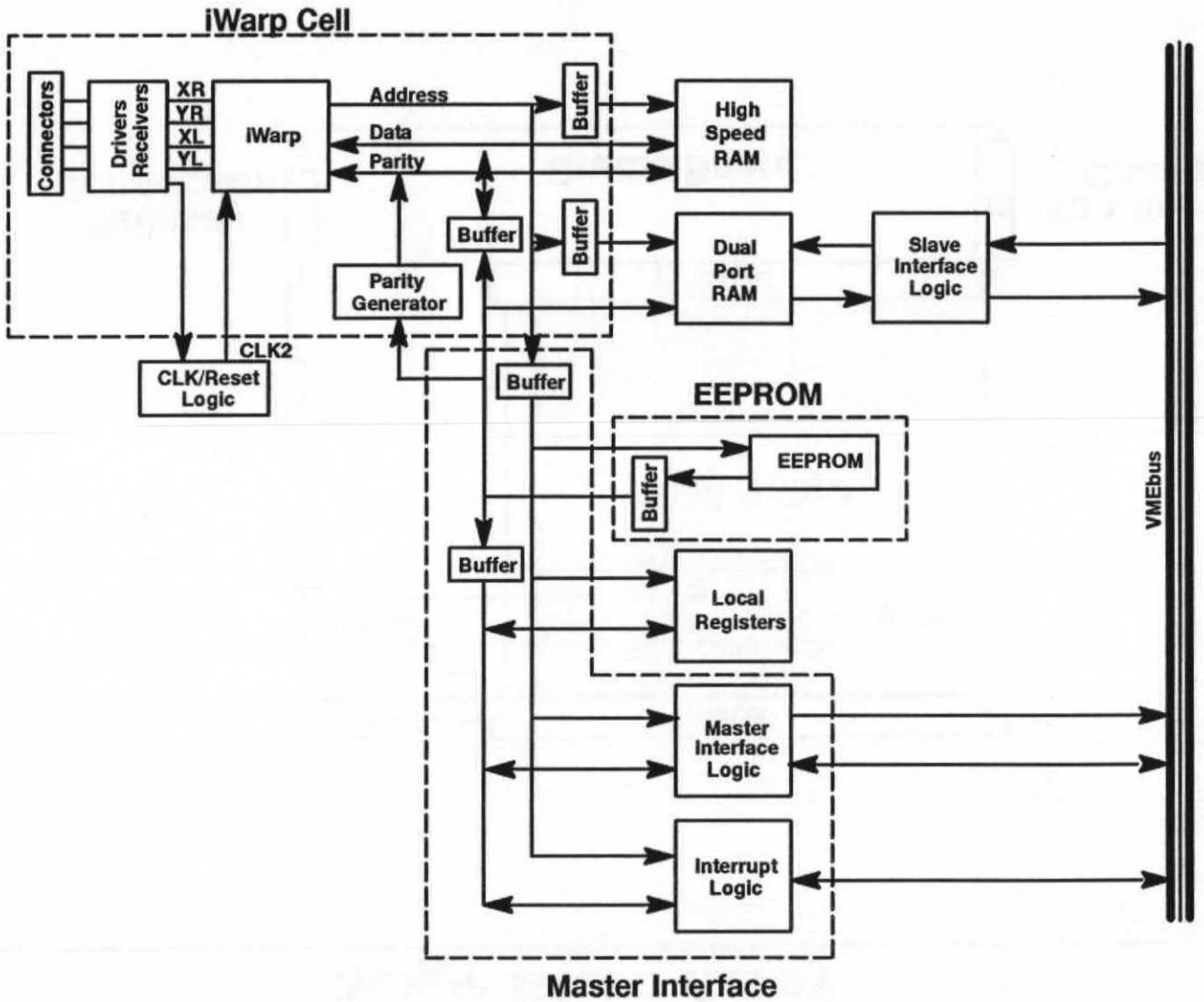
32 x 32 Quad Cell Array (20.48GFlops)
16 x 16 Single Cell Array (5.12GFlops)

Sun Interface Board

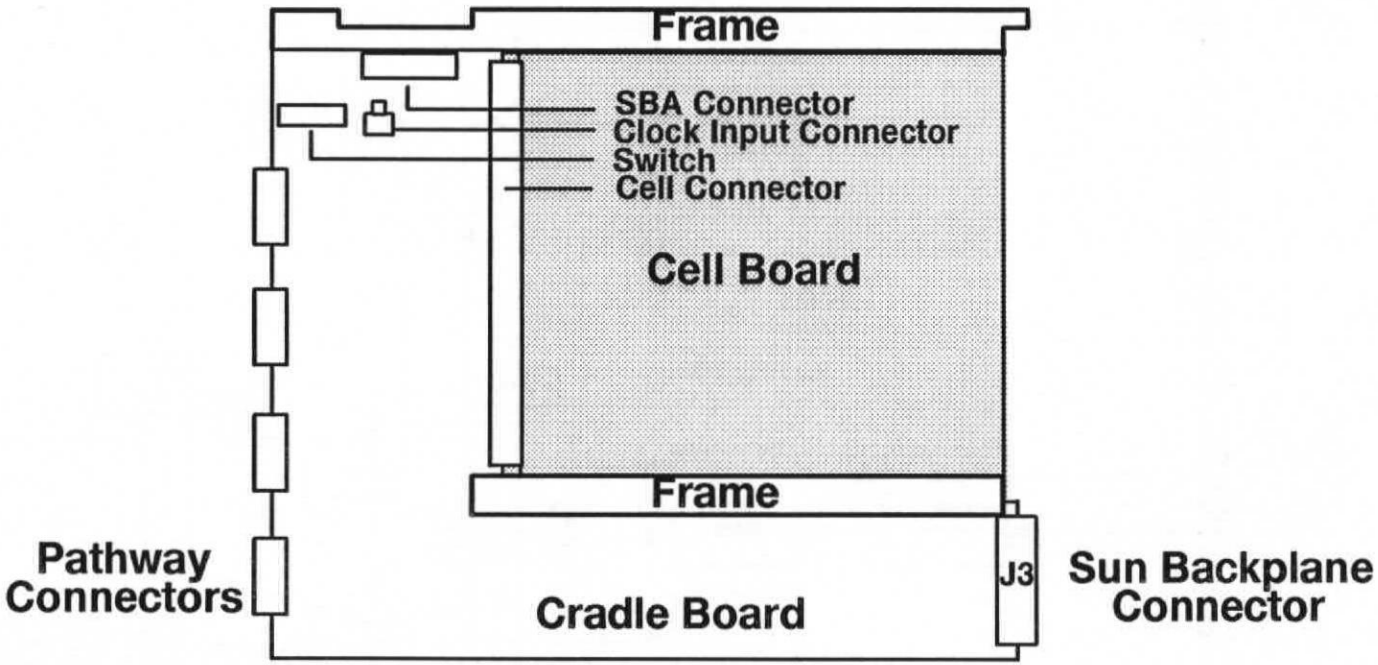
- **VMEbus Slave and Master Compatible**
- **40MBytes/s Slave Transfer Rate [1]**
  18MBytes/s Master Transfer Rate [1]
- **512KBytes/s High Speed SRAM**
- **64KBytes/s Shared Dual Ported Memory**
- **9U Euro Card Form Factor (appro. 14 inch x 15 inch)**

[1] Board Capability, actual transfer rate depends on system capability

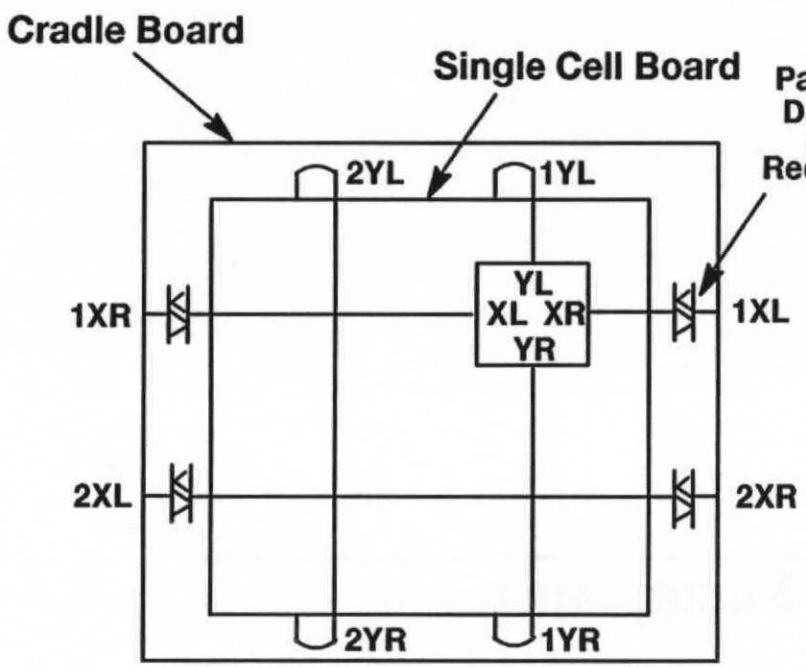
Sun Interface Board Block Diagram



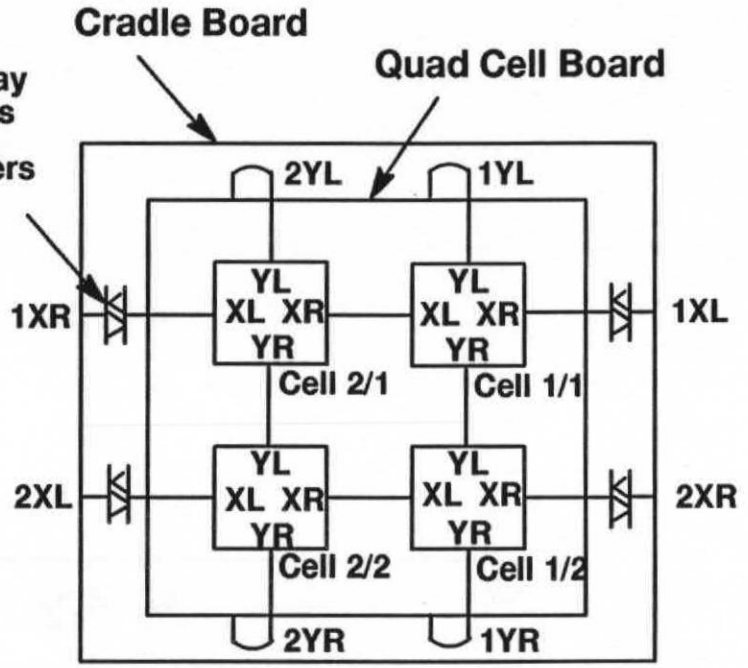
Single Board Array



Single Board Array Block Diagram



SBA With Single Cell Board



SBA With Quad Cell Board

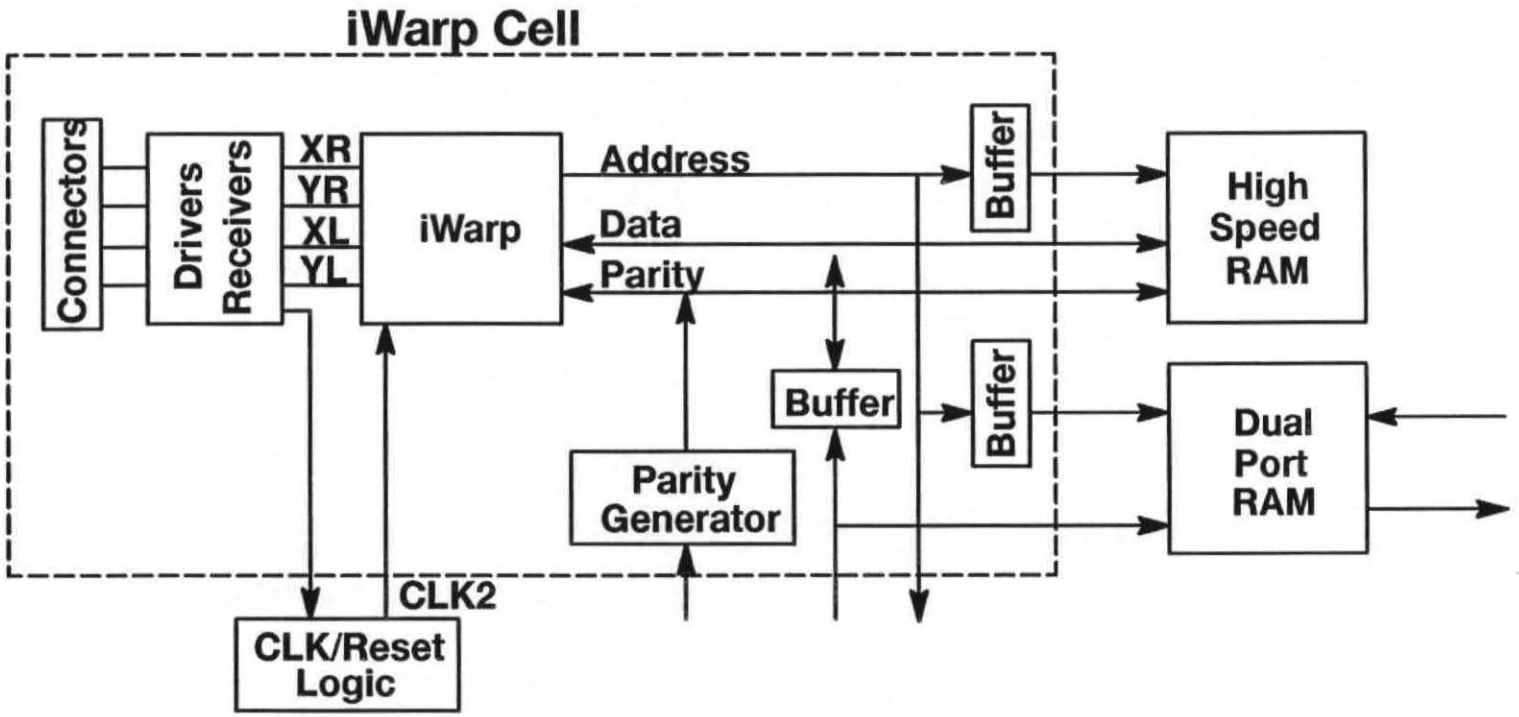
- Up to Nine Single Board Array and Sun Interface Boards may be Configured Together.
- Expandable in the "X" Dimension Only, "Y" Dimension Fixed.
- At Least One Sun Interface Board Required.

Interfacing to iWarp

iWarp Local Memory Interface

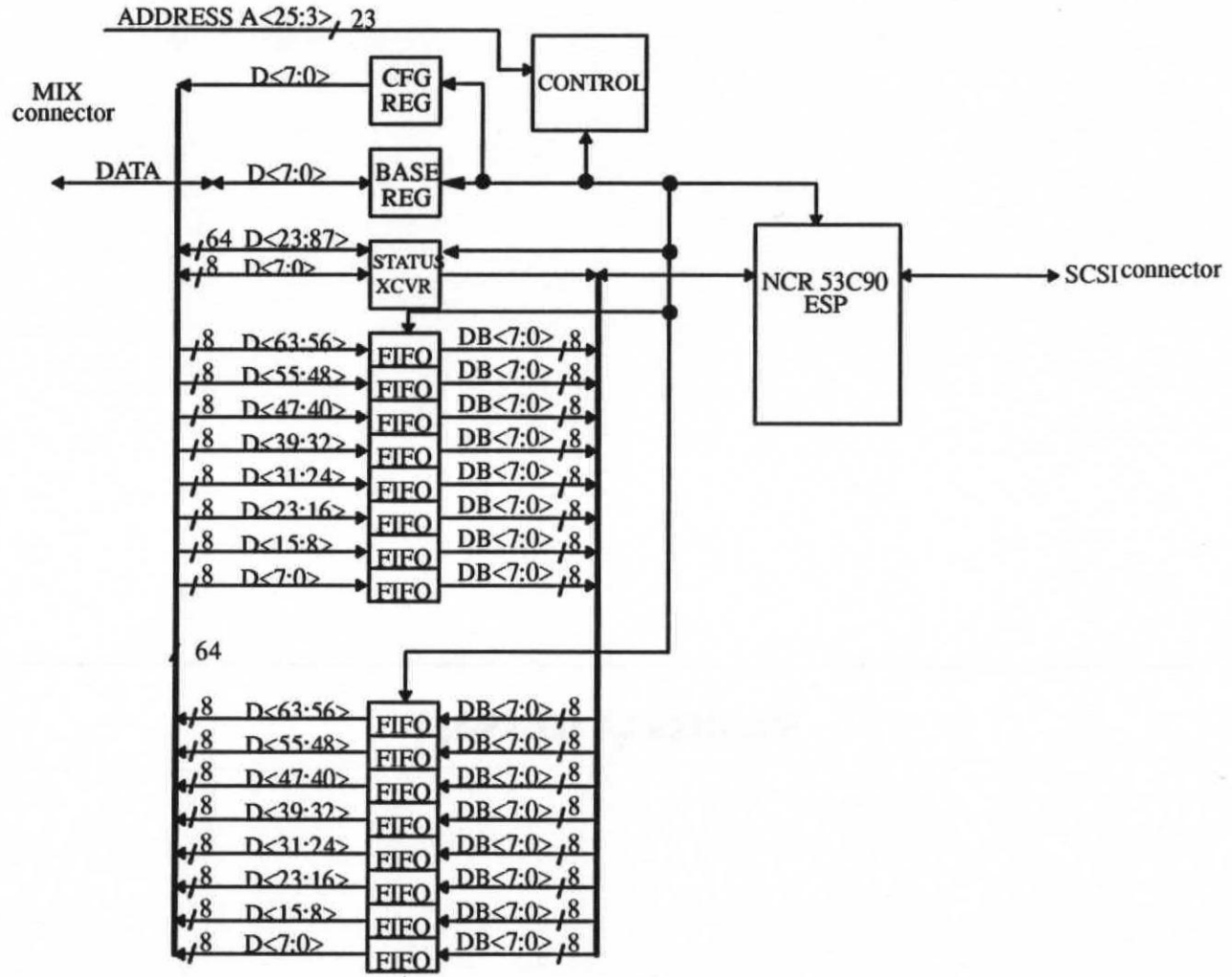
- **Straightforward Read/Write Address/Data Bus, with Ready**
- **Cell Boards provide (via an Intel MIX Connector)**
  All Local Memory Signals; plus Reset, Clock, and Event,
  As Well as Power and Ground.
- **Up to 160MBytes/s Transfer Rate**
- **Two Interface Approaches:**
  - **Shared Dual Ported Memory**
  - **Memory Mapped**

Shared Dual Ported Memory Approach



- Supplies High Performance 40MBytes/s Transfer Rate
- Asynchronous

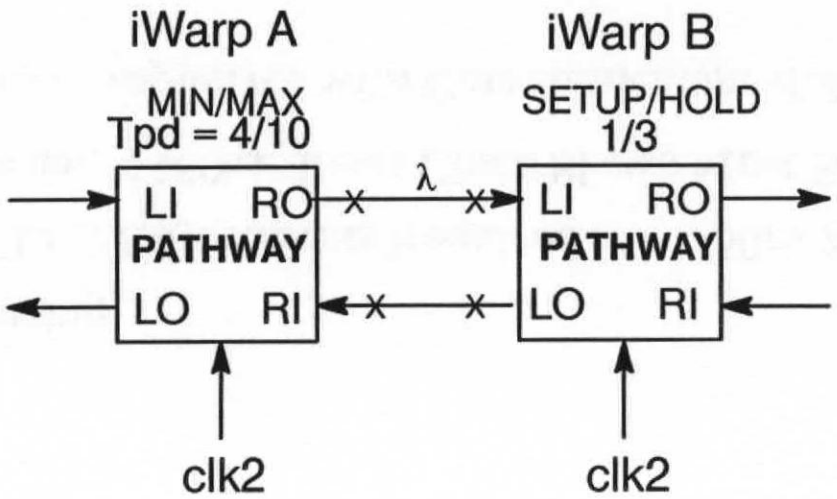
Memory Mapped I/O



Design Aspects

Synchronization

- Near Neighbor



$$\text{Setup}_B \leq \frac{1}{\text{FREQ}_{clk2}} - (\text{SKEW}_{clk2B/A} + \text{Tpd}_{MAXA} + \lambda_{MAX})$$

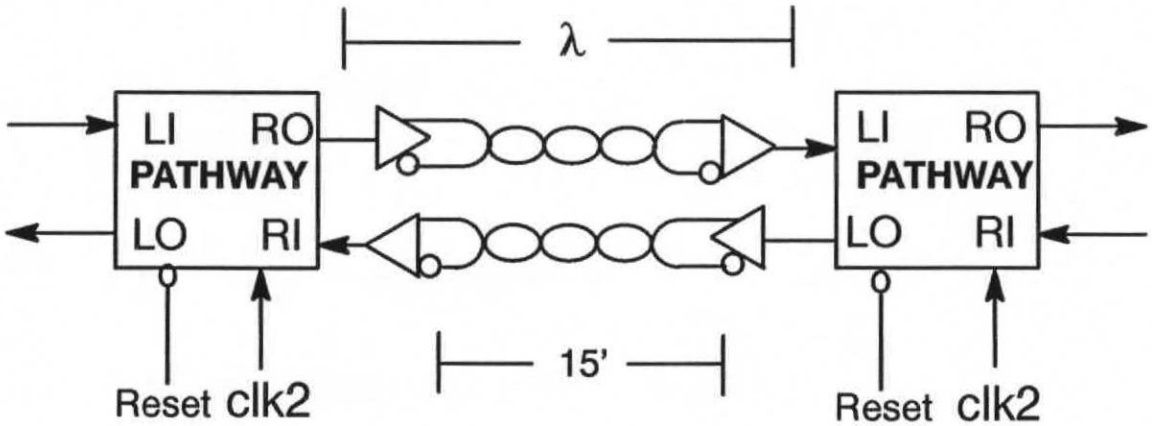
$$\text{Hold}_B \leq (\text{Tpd}_{Min} + \lambda_{Min}) - (\text{SKEW}_{clk2B/A})$$

	Setup	Hold
iWarp Examples:	$3 \leq 25 - (3 + 10 + 5)$	$1 \leq (4 + 0) - 3$
	$3 \leq 7$	$1 \leq 1$

*Assumes Reset Occurs at Both chips on the Same CLK2, All Times Shown are in Nanoseconds (NS)

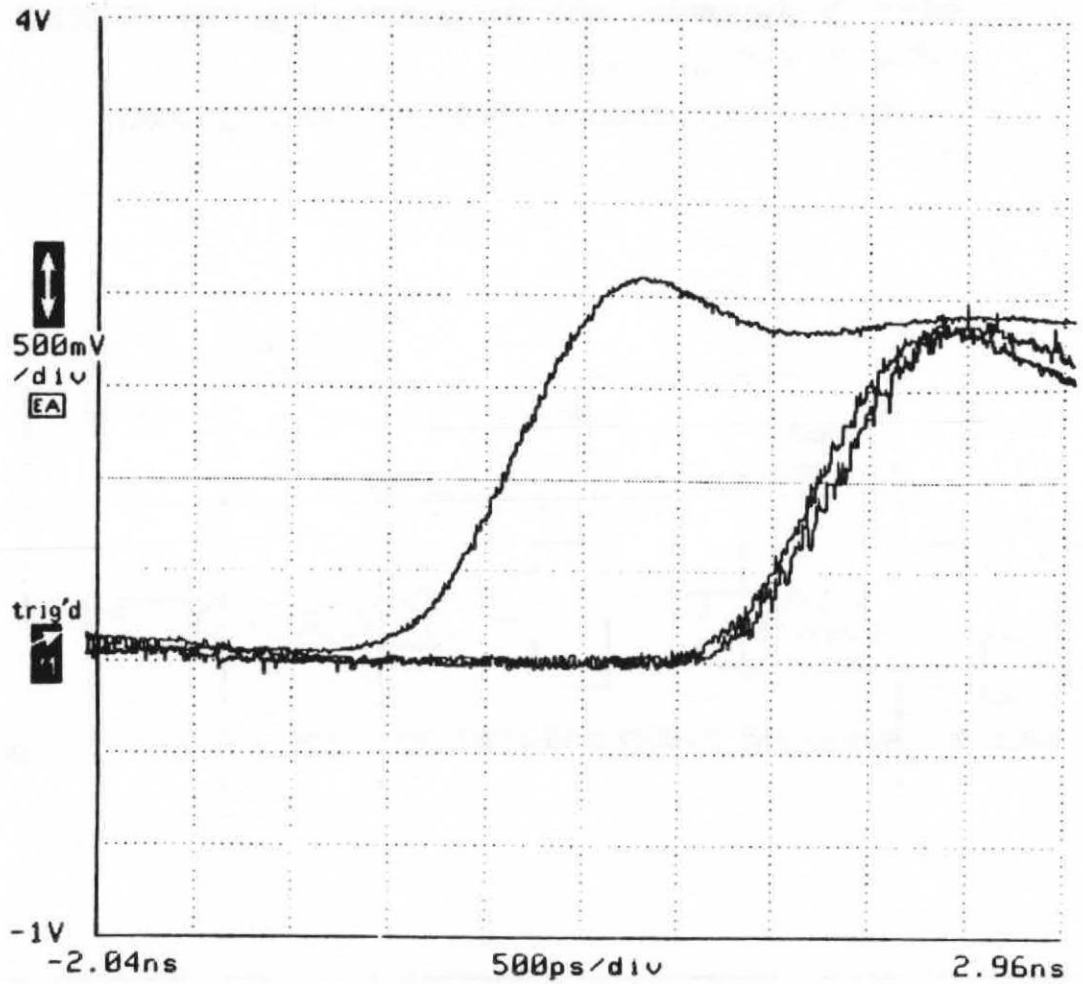
Synchronization (continued)

- Far Neighbor

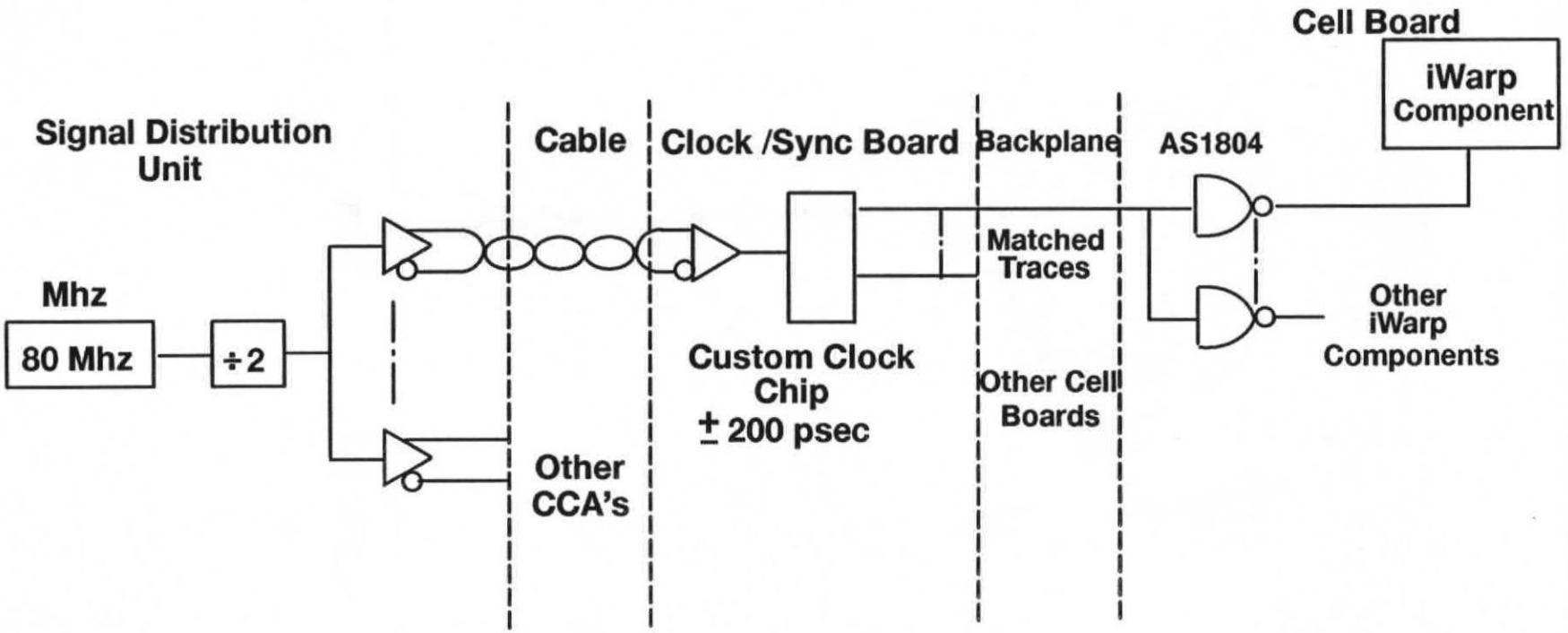


- **Self Synchronizing**
- **No Reset or CLK2 Adjustments Required if** $\lambda < 50ns$ @ 40Mhz
- **For** $\lambda >$ 50ns and < 100ns **Reset Clock Skews Must Be More Closely Aligned**
- **Greater Distance Supported with Communication Holes (Reduced B/W)**

Clock System Performance



System Clock Distribution



iWarp Component to Component Clock Skew

Same Board < 2ns'
Different Boards, Same Cardcage Assembly < 4.4ns'
Different Cardcage Assemblies < 28.4ns'

Threshold Controlled Input Buffers