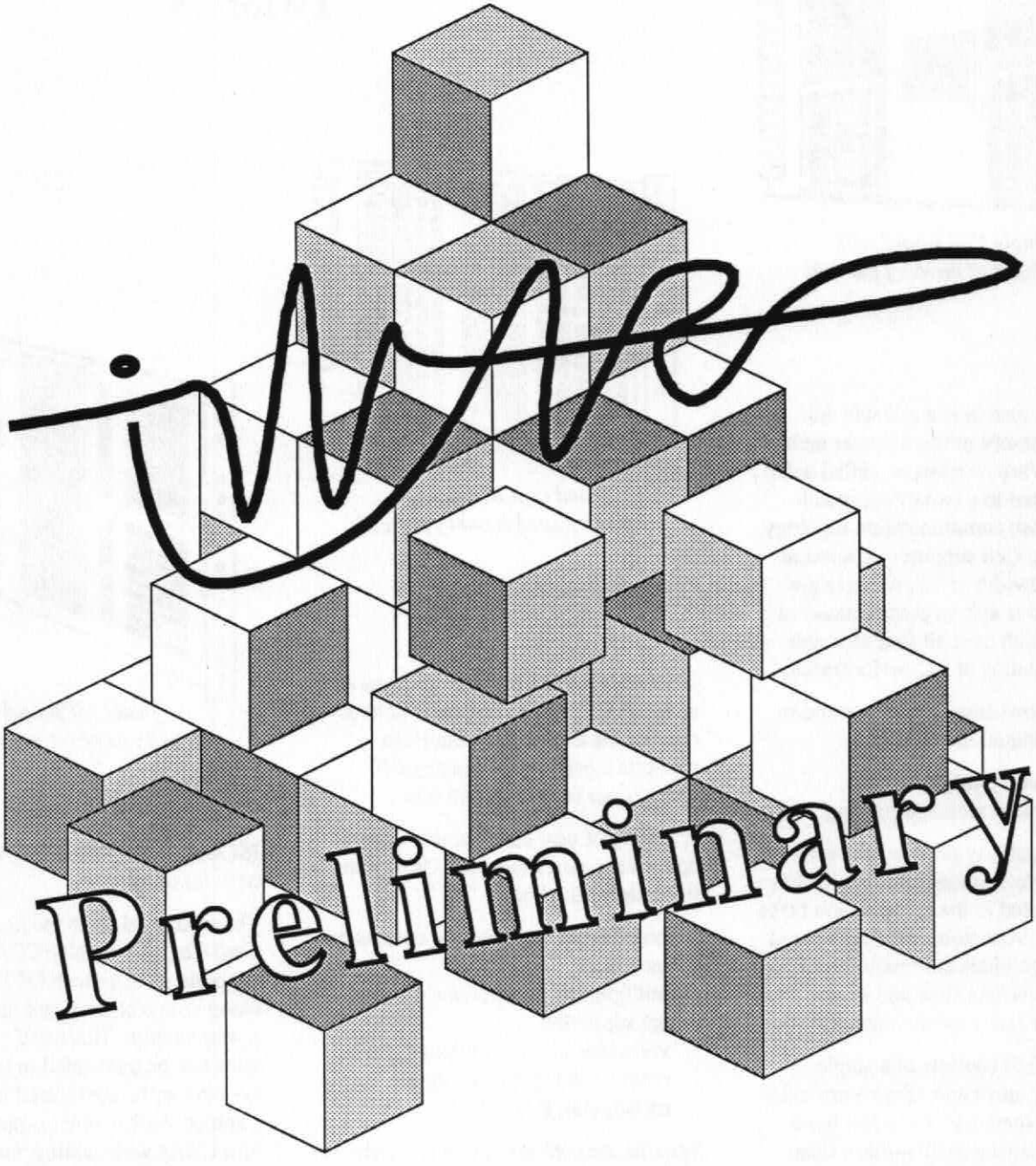
May 26, 1989

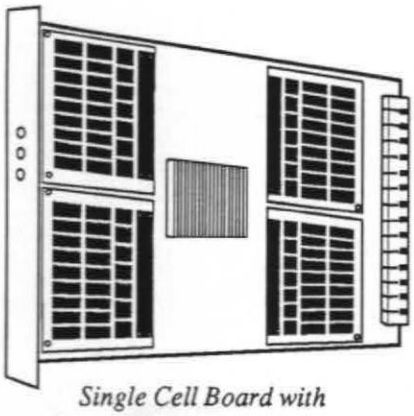
iWarp System Configurations and Options Summary



intel

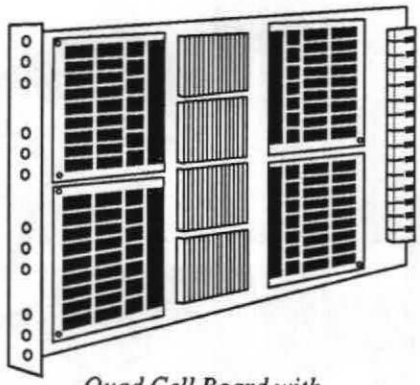
The iWarp* System:

Building blocks for high performance signal and image processing—

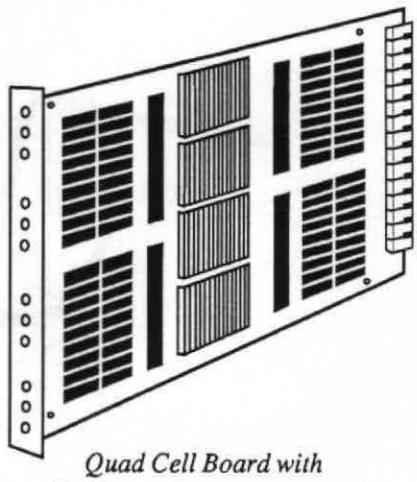


Single Cell Board with
6 MBytes of memory per cell

Boards



Quad Cell Board with
1.5 MBytes of memory per cell



Quad Cell Board with
.5 MBytes of memory per cell

The iWarp system is a scalable distributed memory multicomputer architecture. iWarp processors, called cells, are connected in a two dimensional toroidal mesh communication topology. Each iWarp Cell supports a communication bandwidth of 320 MBytes per second, and is able to communicate at full bandwidth over all four channels while computing at full performance.

iWarp systems support two communication-computation models:

- fine-grain systolic
- coarse-grain message-passing.

Systolic capability provides the efficiency of synchronous communication tightly coupled to the computation tasks of selected processors. Message-based capability provides the flexibility of asynchronous data flow and control required for real-time interaction.

An iWarp Cell consists of a single iWarp component and 18 memory chips per bank of memory. Each cell has a peak performance of 20 million floating-point operations per second (MFLOPS) single precision (32-bits) and 10 MFLOPS double precision (64-bits). iWarp systems are configurable to 1,024 cells for a peak performance of 20,480 MFLOPS.

I/O interfaces and host connections are attached to cells on the border connections of the array. Each interface supports a peak performance of 40 MBytes per second, full duplex.

A variety of user configurable system options are also available. Using configuration guidelines:

- board types and memory options can be mixed,
- multiple I/O connections per array are supported,
- variations in array topology can be configured (eg. linear, square, rectangular, etc).

Systems are comprised of a hierarchy of boards, card cages and cabinets. There are two types of iWarp cell boards. The Quad Cell Board (QCB) has four iWarp cells with memory of .5 MBytes/cell, and an option for expansion to 1.5 MBytes/cell. The Single Cell Board (SCB) has one iWarp cell with 6.0 MBytes of memory.

The next level up in the hierarchy is the Card Cage Assembly (CCA) that supports up to sixteen QCBs or SCBs along with a clock board and integral power supply. These self contained units can be embedded in larger systems, or be configured in a System Cabinet. Each cabinet supports up to four CCAs with cabling, and up to four System Cabinets can be configured to form a single multi-cell array system.

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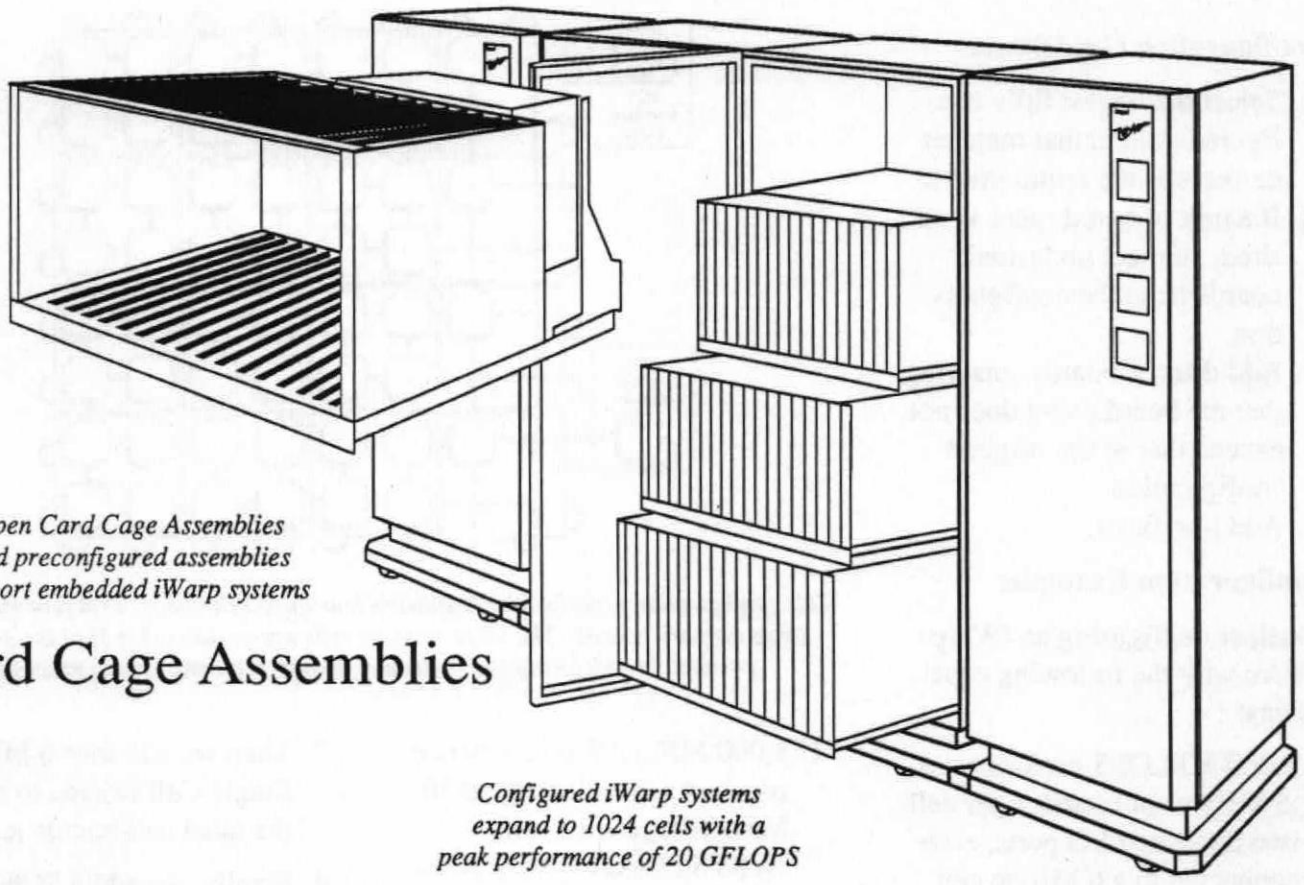


Open Card Cage Assemblies and preconfigured assemblies support embedded iWarp systems

Card Cage Assemblies

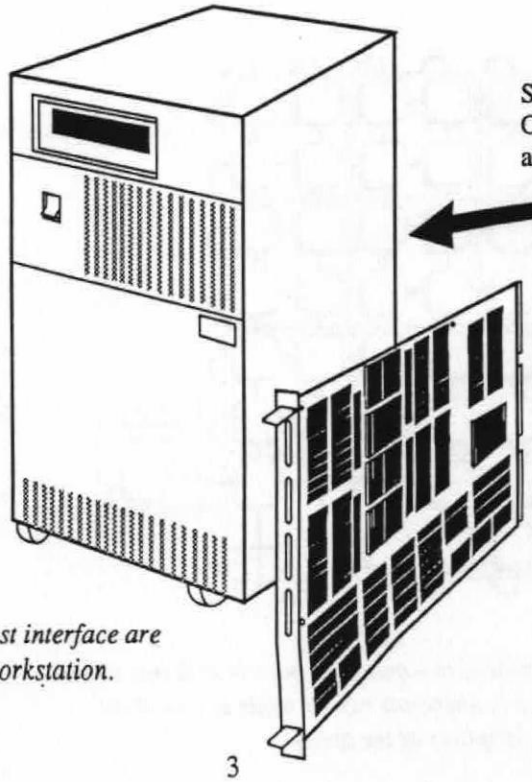
Configured iWarp systems expand to 1024 cells with a peak performance of 20 GFLOPS

Configured Systems

Single Board Arrays support efficient application development

The iWarp Single Board Array (SBA) is a complete iWarp array on a SUN circuit board. Combined with the SUN Interface Board, a complete iWarp system of 1 to 32 cells is supported in a single workstation enclosure.

SBA systems can be configured similar to larger iWarp arrays with one or four cells per board. Memory options include .5 or 1.0 MBytes for a quad cell SBA, and 4.0 MBytes for a single cell version. A single workstation can support up to eight SBAs with 640 MFLOPS in a 2x16 array.



iWarp arrays of 1-32 cells plus host interface are supported in a single SUN workstation.

SBA systems also support the same I/O configuration options of larger iWarp arrays. Thus, the SBA is an ideal environment for developing both applications software and special interfaces for larger systems.

SBA systems provide a small, inexpensive, dedicated environment that can be proliferated throughout a system development team, and provide the power required to meet the demanding needs of real-time applications.

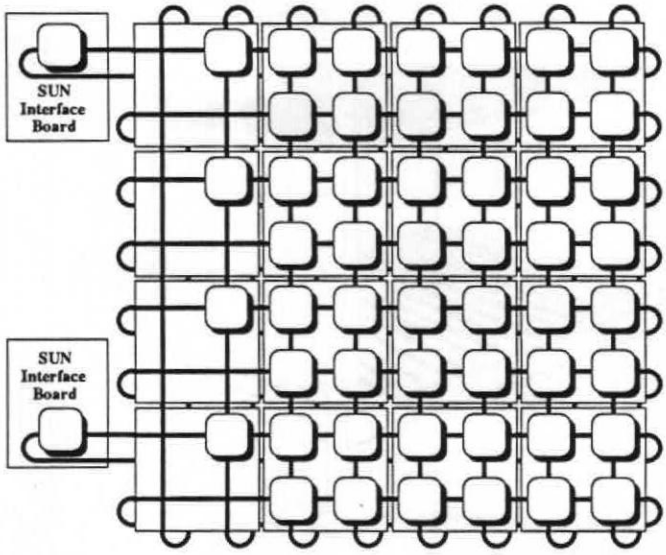
Configuration Guidelines:

1. Select the largest fully configured system that matches or exceeds the requirement.
2. If a mix of board types is desired, subtract undesired boards from the configuration.
3. Add desired boards, ensuring that the board count does not exceed that of the original configuration.
4. Add interfaces.

Configuration Example:

Consider configuring an iWarp system with the following capabilities:

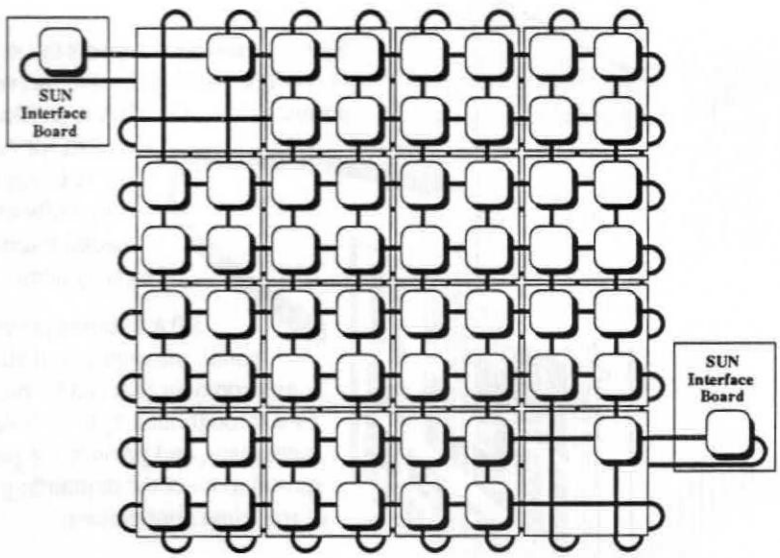
- 1,000 MFLOPS performance,
- .5 MBytes of memory per cell,
- two dedicated I/O ports, each connected to a 6 MByte cell for staging data to the array,
- a SUN host connection,
- a SUN file server connection,
- with the entire configuration supported in a dedicated rack.



This configuration is derived by displacing four quad cell boards with four single cell, large memory boards. The large memory cells are positioned to feed the array in parallel, broadcasting and collecting data as the computation proceeds.

1. 1,000 MFLOPS performance requires a 50 cell array at 20 MFLOPS per cell. An iWSYS 064 Q1 system is selected as the base configuration with 64 quad cell boards with .5 MBytes per cell.
2. Next we subtract four Quad Cell Boards from the array.
3. Then we add four 6 MByte Single Cell Boards to replace the quad cell boards removed.
4. Finally, we add a SUN interface board for the host interface and a second SUN interface for the file server interface.

This configuration contains 52 cells: 48 computation cells on Quad Cell Boards (.5 MByte each), two additional computation cells on Single Cell Boards (6 MBytes each) and two interface cells on Single Cell Boards (6 MBytes each).



The alternate configuration simply displaces two quad cell boards with two single cell large memory boards. Interface connections can be made at any of the loopbacks on the periphery of the array.

Alternate Configuration:
Instead of deleting four Quad boards, you could delete only two and still be able to add the two Single Cell Boards. This configuration contains 58 cells: 56 cells on Quad boards dedicated to the computation task, and two Single Cell Boards dedicated to I/O staging. This configuration has greater performance, but contains somewhat less memory.

iWarp Nomenclature

System Code Numbers—

iW www xxxx y zz

www Indicates the style of the system or the highest level in the hierarchy

- SYS Configured Systems including enclosure
- CCA Card Cage Assembly systems
- SBA Single Board Array based systems

xxxx Defines the number of cells in the system

- 64 64 cells
- 256 256 cells
- 1024 1024 cells

y Identifies the board style used to configure system

- Q Quad Cell Board contains four cells+mem.
- S Single Cell Board contains one cell + mem.

zz Shows memory size per cell in .5MB increments

- 1 500 KBytes
- 2 1 MByte
- 3 1.5 MBytes
- 8 4.0 MBytes
- 12 6.0 MBytes

Upgrade Code Numbers—

iW www xxxxUxxxx y zz

xxxxUxxxx Indicates the number of cells in the base configuration and the number of cells in the final upgraded configuration.

- 0256U0512 Upgrades a 256 cell system to 512
- 0064U0128 Upgrades a 64 cell system to 128

Upgrade configurations are determined by the difference between the existing system configuration and the final desired configuration. If the upgrade requires an additional cabinet, then the SYS upgrades are used. For upgrades within an existing cabinet, a CCA upgrade is required.

For example, upgrading an iWSYS 256 Q to an iWSYS 512 Q requires an additional iWSYS 256 Q system. Likewise, the same upgrade satisfies the requirements of a 512 to 768 upgrade and a 768 to 1,024 upgrade. Similar guidelines apply to systems configured from Single Cell Boards.

Upgrades within a cabinet are configured relative to the cabinet being upgraded. Thus, the upgrade required to expand a 128 Quad cell system to 192 cells is identical to that required to upgrade a 384 Quad cell system to 448 cells. Both require a 64 cell to 128 cell Card Cage Assembly upgrade (384 = full cabinet + 64). To attach the additional 64 cells in the 448 cell configuration into the adjacent 256 cell cabinet, additional external interface boards and cables must be added.

Physical and Environmental

Configured Systems—

Quad Cell Config.	WxDxH	Watts	BTUs
iWSYS256-Q	21"x 21"x 66"	6,000	20,000
iWSYS512-Q	45"x 21"x 66"	12,000	41,000
iWSYS768-Q	69"x 21"x 66"	18,000	61,000
iWSYS1024-Q	90"x 21"x 66"	24,000	82,000

Single Cell Config.	WxDxH	Watts	BTUs
iWSYS64-S	21"x 21"x 66"	4,000	14,000
iWSYS128-S	45"x 21"x 66"	8,000	27,000
iWSYS192-S	69"x 21"x 66"	12,000	42,000
iWSYS256-S	90"x 21"x 66"	16,000	56,000

Card Cage Assemblies—

Configuration	WxDxH	Watts	BTUs
iWCCA64-Q	19"x 21"x 12.3"	1,500	5,000
iWCCA16-S	19"x 21"x 12.3"	1,000	3,400

Boards—

Configuration	WxDxH	Watts	BTUs
iWQCB-1	1"x 11"x 9.2"	50	170
iWQCB-2	1"x 11"x 9.2"	52	180
iWQCB-3	1"x 11"x 9.2"	55	190
iWSCB-8	1"x 11"x 9.2"	38	130
iWSCB-12	1"x 11"x 9.2"	40	140
iWSBA-Q1	.8"x 16.5"x 14.5"	60	200
iWSBA-Q2	.8"x 16.5"x 14.5"	65	220
iWSBA-S8	.8"x 16.5"x 14.5"	45	160
iWSIB-1	.8"x 16.5"x 14.5"	75	260

iWarp Systems and Constituent Elements

Configured Systems—

.5MB/cell Systems		Cells	MBytes	MFLOPS
iWSYS 64	-Q1	64	32	1,280
iWSYS 128	-Q1	128	64	2,560
iWSYS 192	-Q1	192	96	3,840
iWSYS 256	-Q1	256	128	5,120
iWSYS 512	-Q1	512	256	10,240
iWSYS 768	-Q1	768	384	15,360
iWSYS 1024	-Q1	1,024	512	20,480

1.5MB/cell Systems		Cells	MBytes	MFLOPS
iWSYS 64	-Q3	64	96	1,280
iWSYS 128	-Q3	128	192	2,560
iWSYS 192	-Q3	192	288	3,840
iWSYS 256	-Q3	256	384	5,120
iWSYS 512	-Q3	512	768	10,240
iWSYS 768	-Q3	768	1,152	15,360
iWSYS 1024	-Q3	1,024	1,536	20,480

6MB/cell Systems		Cells	MBytes	MFLOPS
iWSYS 16	-S12	16	96	320
iWSYS 32	-S12	32	192	640
iWSYS 48	-S12	48	288	960
iWSYS 64	-S12	64	384	1,280
iWSYS 128	-S12	128	768	2,560
iWSYS192	-S12	192	1,152	3,840
iWSYS256	-S12	256	1,536	5,120

System Upgrades— *See note*

.5MB/cell Upgrades		Cells	MBytes	MFLOPS
iWSYS 256U384	-Q1	128	64	2,560
iWSYS 384U512	-Q1	128	64	2,560
iWSYS 256U512	-Q1	256	128	5,120
iWSYS 512U768	-Q1	256	128	5,120
iWSYS 768U1024	-Q1	256	128	5,120

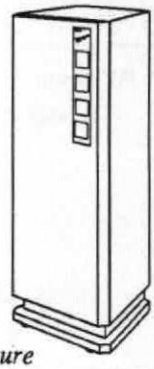
1.5MB/cell Upgrades		Cells	MBytes	MFLOPS
iWSYS 256U384	-Q3	128	192	2,560
iWSYS 384U512	-Q3	128	192	2,560
iWSYS 256U512	-Q3	256	384	5,120
iWSYS 512U768	-Q3	256	384	5,120
IWSYS 768U1024	-Q3	256	384	5,120

6MB/cell Upgrades		Cells	MBytes	MFLOPS
iWSYS 64U96	-S12	32	192	640
iWSYS 96U128	-S12	32	192	640
iWSYS 64U128	-S12	64	384	1,280
iWSYS 128U192	-S12	64	384	1,280
iWSYS 192U256	-S12	64	384	1,280

Note: For upgrades within a single cabinet, see "Card Cage Assemblies and Upgrades", page 7

Systems

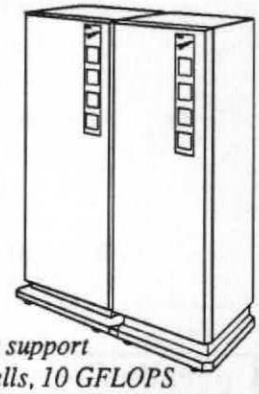
Quad Cell	Single Cell
iWSYS 64	iWSYS 16
iWSYS 128	iWSYS 32
iWSYS 192	iWSYS 48
iWSYS 256	iWSYS 64



16 to 256 iWarp cells can be configured in a single system enclosure

Systems

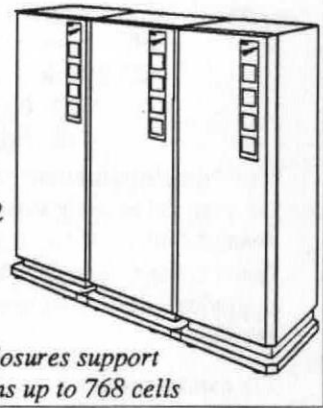
Quad Cell	Single Cell
iWSYS 512	iWSYS 128



Two system enclosures support iWarp configurations to 512 cells, 10 GFLOPS

Systems

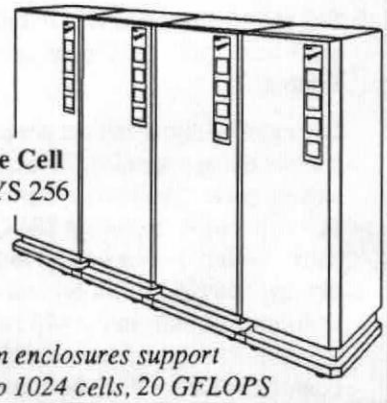
Quad Cell	Single Cell
iWSYS 768	iWSYS 192



Three system enclosures support iWarp configurations up to 768 cells

Systems

Quad Cell	Single Cell
iWSYS 1024	iWSYS 256



Four system enclosures support configurations to 1024 cells, 20 GFLOPS

Cabinet Upgrades & Assemblies

Card Cage Assemblies & Upgrades—

Base Card Cage Assemblies		Cells	MBytes	MFLOPS
iWCCA	——	——	——	——
iWCCA 64	-Q1	64	32	1,280
iWCCA 64	-Q3	64	96	1,280
iWCCA 16	-S12	16	96	320

.5MB/cell CCA Upgrades		Cells	MBytes	MFLOPS
iWCCA 64U128	-Q1	64	32	1,280
iWCCA 128U192	-Q1	64	32	1,280
iWCCA 192U256	-Q1	64	32	1,280

1.5MB/cell CCA Upgrades		Cells	MBytes	MFLOPS
iWCCA 64U128	-Q3	64	96	1,280
iWCCA 128U192	-Q3	64	96	1,280
iWCCA 192U256	-Q3	64	96	1,280

6MB/cell CCA Upgrades		Cells	MBytes	MFLOPS
iWCCA 16U32	-S12	16	96	320
iWCCA 32U48	-S12	16	96	320
iWCCA 48U64	-S12	16	96	320

Boards—

.5MB/cell Quad Cell		Cells	MBytes	MFLOPS
iWQCB-1	——	4	2.0	80
iWSBA-Q1		4	2.0	80

Ext. Mem. Quad Cell		Cells	MBytes	MFLOPS
iWQCB-3	——	4	6.0	80
iWSBA-Q2	——	4	4.0	80

Single Cell Boards		Cells	MBytes	MFLOPS
iWSCB-12	——	1	6.0	20
iWSBA-S8	——	1	4.0	20

Miscellaneous boards

iWCLB	Clock Board
iWEIB	External interface Board
iWMEM-1	.5 MByte Memory board
iWMEM-2	1.0 MByteMemory board
iWSIB-1	SUN Interface Board (contains one iWarp cell and .5 MBytes of memory

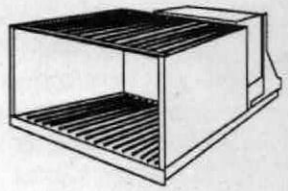
Cables—

Miscellaneous cables

iWLCA	Local-chassis Cable Assembly
iWICA	Inter-chassis Cable Assembly
iWECA	External Cabinet Cable Assem.

Card Cage Assembly (CCA)

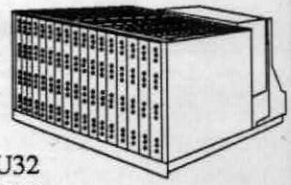
iWCCA



iWarp Card Cage Assemblies are self contained, including power supply and cooling

Card Cage Systems

Quad Cell	Single Cell
iWCCA 64	iWCCA 16



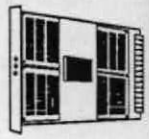
Card Cage Upgrades

iWCCA 64U128	iWCCA 16U32
iWCCA 128U192	iWCCA 32U48
iWCCA 192U256	iWCCA 48U64

Each CCA supports 16 iWarp boards with mixed configurations

Single Cell Board (SCB)

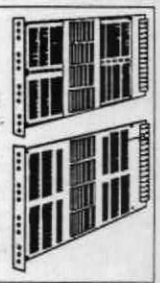
iWSCB-12 6 MBytes/cell



16 SCBs can be configured in a CCA to support 16 iWarp cells

Quad Cell Boards (QCB)

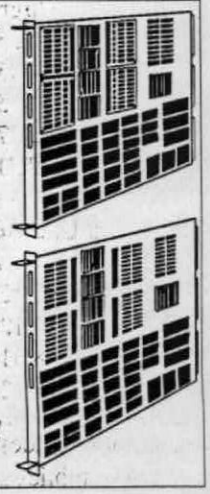
iWQCB-1	.5 MBytes/cell
iWQCB-3	1.5 MBytes/cell



16 QCBs can be configured in a CCA to support 64 iWarp cells

Single Board Arrays (SBA)

iWSBA-Q1	.5 MBytes/cell
iWSBA-Q2	1.0 MBytes/cell
iWSBA-S8	4.0 MBytes/cell



SUN workstations support one to eight SBAs, plus required Sun Interface Board, (SIB)

Software, Services and Manuals

System Software— *See note*

System Support Software

- C optimizing compiler
- Program Development Environ. Assembler, Linker, Loader Multi-cell Debugger
- Cell Runtime Kernel
- Host Runtime System

Optional Software

- FORTRAN compiler (optimized)
- APPLY application development tool and WEBlib image library

Consulting Services—

System and Application Consulting

- Contracted software/hardware development and consulting services for special requirements.

Note: A single System Support Software package is included with each iWSYS or iWSBA array system

Support Services—

Warranty Service

- 90 days covered in purchase

Service Support Contract

- Service Support Contracts supported by Intel's world-wide Customer Service organization provide hardware and software support for a variety of customer needs and response times.

Time and Materials Service

- Time and Materials Service meets the special needs of iWarp OEMs, Value Added Resellers and certain customers who must maintain their own equipment.

Manuals—

Hardware

- Site Preparation Manual
- System Installation Manual
- System Configuration Guide

Software

- Programmer's Guide
- Language Extensions Manuals
- System Debugger Manual
- Operating System Manual
- Applications Libraries

Service and Support

- System Diagnostics Manual
- System Administrator's Manual

Intel, Carnegie Mellon, DARPA, SPAWAR and iWarp

Founded in 1968, Intel Corporation has long been recognized as an innovative leader in VLSI component technology. In recent years, Intel has extended this leadership role to parallel systems. iWarp is the result of a joint collaboration between Carnegie Mellon University and Intel in a development program sponsored by the Defense Advanced Research Projects Agency (DARPA), and administered through Department of the Navy, Space and Naval Warfare Systems Command. Intel's expertise in systems and VLSI component technology has been joined with a decade of research at Carnegie Mellon to produce the first supercomputer to meet the performance and I/O needs of signal and image processing applications.

For further information on the iWarp system, write or call:

Intel Corporation
iWarp Marketing, MS JF1-60
5200 Elam Young Parkway
Hillsboro, Oregon 97124

Phone: (503) 696-4746

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