Massachusetts Institute of Technology
School of Engineering Faculty Personnel Record

Date: April 11, 2013
Full Name: Charles E. Leiserson
Department: Electrical Engineering and Computer Science

1. Date of Birth

November 10, 1953

2. Citizenship

U.S.A.

3. Education

School	Degree	Date
Yale University	B.S. (*cum laude*)	May 1975
Carnegie Mellon University	Ph.D.	Dec. 1981

4. Title of Thesis for Most Advanced Degree

Area-Efficient VLSI Computation

5. Principal Fields of Interest

Analysis of algorithms
Parallel algorithms, architectures, and languages
Digital hardware and computing machinery
Multicore computing
Parallel and distributed computing
Caching
Theoretical computer science
Supercomputing
Computer network architecture
Scalable computing systems
Distance education and interaction
Computer chess
Leadership skills for engineering and science faculty

6. Name and Rank of Other Department Faculty in the Same Field

Scott Aaronson, Associate Professor
Anant Agarwal, Professor
Saman Amarasinghe, Professor

Arvind, Professor
Constantinos Daskalakis, Assistant Professor
Eric Demaine, Professor
Jack Dennis, Professor Emeritus
Srini Devadas, Professor
Shafi Goldwasser, Professor
Piotr Indyk, Professor
David Karger, Professor
Nancy A. Lynch, Professor
Albert R. Meyer, Professor
Silvio Micali, Professor
Dana Moshkovitz, Assistant Professor
Martin Rinard, Professor
Ronald L. Rivest, Professor
Ronitt Rubinfeld, Professor
Nir Shavit, Professor

7. Name and Rank of Faculty in Other Departments in the Same Field

Bonnie Berger, Professor (Mathematics)
Alan Edelman, Professor (Mathematics)
Michel X. Goemans, Professor (Mathematics)
Jonathan Kelner, Assistant Professor (Mathematics) F. Thomson Leighton, Professor (Mathematics)
Peter W. Shor, Professor (Mathematics) Michael F. Sipser, Professor (Mathematics)

8. Non-MIT Experience

Employer	**Position**	**Beginning**	**Ending**
International Computing Centre (*United Nations, Geneva, Switzerland*)	Programmer Assistant	June 1973	Sep. 1973
Yale University (*Department of Computer Science*)	Programmer	May 1974	Sep. 1974
POS Corporation (*New Haven, CT*)	Software Consultant (*part time*)	Sep. 1974	May 1975
Computervision Corporation (*Bedford, MA*)	Programmer	June 1975	Sep. 1976
Max Planck Institute für Informatik (*Saarbrücken, Germany*)	Fachbeirat (Visiting Committee)	Sep. 1992	Aug. 1997
Ecole Normale Superiéure de Lyon	Visiting Professor	June 1993	July 1993

(*Lyon, France*)

National University of Singapore (*Republic of Singapore*)	Shaw Visiting Professor	Aug. 1995	Aug. 1996
Akamai Technologies (*Cambridge, MA*)	Director of System Architecture	June 1999	May 2001
Cilk Arts (*Burlington, MA*)	Founder, Chief Technology Officer	Sep. 2006	July 2009

9. History of MIT Appointments

Rank	**Beginning**	**Ending**
Assistant Professor	Jan. 1981	June 1984
Associate Professor	July 1984	June 1988
Associate Professor (with tenure)	July 1988	June 1992
Professor	July 1992	present

10. Consulting Record

Firm	**Beginning**	**Ending**
MIT Lincoln Laboratory	Feb. 1982	Aug. 1984
AT&T Bell Laboratories	Jan. 1983	Dec. 1986
Harris Corporation (GASD)	Feb. 1983	May 1985
Cognition	Dec. 1984	June 1985
Analog Devices	Feb. 1985	June 1985
Thinking Machines	July 1985	Aug. 1994
Harris Corporation (GCSD)	May 1986	June 1986
W. W. Oliver Company	Jan. 1987	Jan. 1987
Wolfsort Corporation	Mar. 1991	Mar. 1991
National University of Singapore, Adjunct Professor	Sep. 1996	Aug. 2005
NKK Corporation	Mar. 1997	Mar. 1997
Pratt & Whitney	May 1997	Dec. 1999
EMC^2 Corporation	June 1998	Feb. 1999
Akamai Technologies	June 1999	May 2001
Etisalat University, UAE	Apr. 2003	Aug. 2005
RealNetworks	May 2003	June 2007
National University of Singapore	Feb. 2005	Feb. 2005
Carnegie Mellon University	Oct. 2006	Oct. 2006
Cilk Arts	Sept. 2006	Mar. 2009
Harvard University	Jul. 2011	Jul. 2011
University of California, Berkeley	Jan. 2012	Jan. 2012

Intel Corporation	Sept. 2009	present

11. Department and Institute Committees, Other Assigned Duties

Activity	**Beginning**	**Ending**
Graduate Counselor (EECS)	Sep. 1981	May 1988
Area II Committee (EECS)	Sep. 1981	May 1988
LCS Executive Committee	Sep. 1981	Sep. 1982
Graduate Admissions Committee (EECS)	Nov. 1981	May 1985
LCS Executive Committee	Sep. 1984	Dec. 1987
MIT/LCS Student Workshop (Chairman)	July 1990	July 1994
Undergraduate Advisor (EECS)	Sep. 1990	May 1995
VI-A liaison for IBM Research	Feb. 1991	Mar. 1993
MIT VLSI & Parallel Systems Student Workshop (Chairman)	May 1991	July 1991
MIT VLSI & Parallel Systems Student Workshop (Chairman)	May 1992	July 1992
Leader, Supertech Research Group	Sep. 1993	present
MIT Supercomputing Technologies Student Workshop (Chairman)	May 1993	July 1993
Graduate Counselor (EECS)	Sep. 1996	present
Area II Committee (EECS)	Sep. 1996	present
EECS Professional Education Policy Committee	Mar. 1992	May 1993
MIT Commencement Committee	Sep. 1996	May 2001
Singapore Engineering Education Assessment Committee	Mar. 1997	June 1998
MIT Student Workshop (Chairman)	Apr. 1997	July 1997
EECS Client Building Committee	Apr. 1997	July 1999
EECS Faculty Search Committee	Nov. 1998	Sep. 1999
Head of Singapore-MIT Alliance program in Computer Science	Sep. 2001	Feb. 2005
UPOP Workshop Engineering Co-Chair	Sep. 2001	present
OpenCourseWare Underwriting Committee	Feb. 2010	present

12. Government Committees, Service, etc.

Activity	**Date**	
NSF *Ad Hoc* Committee on Supercomputing Software	1985	
DARPA/ISTO TeraOps Working Group	1987–1989	
Joint DARPA/NSF and ESPRIT Exploratory Workshop on Information Science and Technology	1990	
Presentation to the Computer Science and Telecommunications Board at the National Academies	2007	
ACM SPAA Steering Committee	1989	present

13. Awards Received

Award	**Date**
Benjamin F. Barge Prize in Mathematics (*Yale University*)	1972
Hertz Fellowship	1977
Hertz Doctoral Thesis Award	1982

ACM Doctoral Dissertation Award	1982
NSF Presidential Young Investigator Award	1985
IEEE Int. Conf. on Parallel Processing Best Presentation Award	1985
IEEE Int. Conf. on Parallel Processing Best Presentation Award (with Thomas H. Cormen)	1986
IEEE Int. Conf. on Parallel Processing Most Original Paper Award (with Bruce M. Maggs)	1986
Best 1990 Professional and Scholarly Book in Computer Science and Data Processing, Association of American Publishers (with Thomas H. Cormen and Ronald L. Rivest)	1990
Richard B. Adler Scholar, MIT EECS Department	1991
3rd Place in ACM International Computer Chess Championship for StarTech	1993
3rd Place in ACM International Computer Chess Championship for ⋆Socrates	1994
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'95	1995
2nd Place in ICCA 8th Computer Chess World Championship for ⋆Socrates 2.0	1995
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'96	1996
1st Place in Dutch Open Computer Chess Championship for Cilkchess	1996
IEEE Computer Society Distinguished Visitor for the Asia-Pacific Region	1996–1998
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'97	1997
2nd Place in Dutch Open Computer Chess Championship for Cilkchess	1997
1st Prize in the *International Conference on Functional Programming*'s ICFP Programming Contest	1998
2nd Place in Dutch Open Computer Chess Championship for Cilkchess	1998
IEEE Micro Top Picks	2006
ACM Fellow	2007
Margaret MacVicar Faculty Fellow, MIT	2007–present
ACM SIGPLAN Most Influential 1998 PLDI Paper Award	2008
ACM SPAA Best Paper Award	2009
ACM SPAA Best Paper Award	2012

14. Organization Membership

Organization	**Offices Held**
AAAS	
ACM	
IEEE	
SIAM	
ACM Turing Award Committee	1983–1987, (Chair, 1986)
Journal of VLSI and Computer Systems	Editor, 1983–1985
1982 MIT VLSI Conference	Program Committee
1984 MIT VLSI Conference	Program Committee

1986 MIT VLSI Conference Committee	Program Chair
Springer-Verlag Texts and Monographs in Computer Science	Editorial Board, 1986–1993
1986 IEEE Symposium on Foundations of Computer Science	Program Committee
Journal of Parallel and Distributed Computing	Editor, 1986–1988
Applied Mathematics Letters	Editor, 1987–1990
1989 ACM Symposium on Parallel Algorithms and Architectures	Program Committee
1989 IEEE Symposium on Foundations of Computer Science	Program Committee
Supercomputing '91	Program Committee
1993 DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation	Organizing Committee
1994 ACM Symposium on Parallel Algorithms and Architectures	Program Chair
ACM Symposium on Parallel Algorithms and Architectures	General Chair, 1994–1997
Journal of Computer and Systems Science	Guest Editor, 1996
SC'xy Steering Committee, 1999	
Journal of Parallel and Distributed Computing	Advisory Board, 1999
2003 ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming	Program Committee
Dagstuhl Seminar 04301 in Cache-Oblivious and Cache-Aware Algorithms	Organizer, 2004

15. Patents and Patent Applications Pending

1. H. T. Kung and Charles E. Leiserson, "Systolic array apparatuses for matrix computations," *United States Patent* 4,493,048, filed May 16, 1983, issued January 8, 1985.

2. Thomas H. Cormen and Charles E. Leiserson, "Message merging device," *United States Patent* 4,922,246, filed November 25, 1986, issued May 1, 1990.

3. David C. Douglas, Mahesh N. Ganmukhi, Jeffrey V. Hill, W. Daniel Hillis, Bradley C. Kuszmaul, Charles E. Leiserson, David S. Wells, Monica C. Wong, Shaw-Wen Yang, and Robert C. Zak, Jr., "Parallel computer system," *United States Patent* 5,333,268, filed September 16, 1992, issued July 26, 1994.

4. Robert C. Zak, Charles E. Leiserson, Bradley C. Kuszmaul, Shaw-Wen Yang, W. Daniel Hillis, David C. Douglas, and David Potter, "Parallel computer system including arrangement for transferring messages from a source processor to selected ones of a plurality of destination processors and combining responses," *United States Patent* 5,265,207, filed April 8, 1993, issued November 23, 1993.

5. Charles E. Leiserson, Robert C. Zak, Jr., W. Daniel, Hillis, Bradley C. Kuszmaul, and Jeffrey V. Hill, "Parallel computer system including request distribution network for distributing

processing requests to selected sets of processors in parallel," *United States Patent* 5,388,214, filed January 14, 1994, issued February 7, 1995.

6. Bradley C. Kuszmaul, Charles E. Leiserson, Shaw-Wen Yang, Carl R. Feynman, W. Daniel Hillis, David Wells, and Cynthia J. Spiller, "Parallel computer system including arrangement for quickly draining messages from message router," *United States Patent* 5,390,298, filed January 14, 1994, issued February 14, 1995.

7. David C. Douglas, Charles E. Leiserson, Bradley C. Kuszmaul, Shaw-Wen Yang, Daniel W. Hillis, David Wells, Carl R. Feynman, Bruce J. Walker, and Brewster Kahle, "Router for parallel computer including arrangement for redirecting messages," *United States Patent* 5,530,809, filed January 14, 1994, issued June 25, 1996.

8. W. Daniel Hillis, David C. Douglas, Charles E. Leiserson, Bradley C. Kuszmaul, Mahesh N. Ganmukhi, Jeffrey V. Hill, and Monica C. Wong-Chan, "Parallel computer system with physically separate tree networks for data and control messages," *United States Patent* 5,590,283, filed January 27, 1995, issued December 31, 1996.

9. Bradley C. Kuszmaul, Charles E. Leiserson, Shaw-Wen Yang, Carl R. Feynman, W. Daniel Hillis, and David C. Douglas, "Digital computer for determining a combined tag value from tag values selectively incremented and decremented reflecting the number of messages transmitted and not received," *United States Patent* 5,680,550, filed February 13, 1995, issued October 21, 1997.

10. Timothy N. Weller and Charles E. Leiserson, "Content delivery network service provider (CDNSP)-managed content delivery network (CDN) for network service provider (NSP)," *United States Patent* 7,149,797, filed April 2, 2002, issued December 12, 2006.

11. Timothy N. Weller and Charles E. Leiserson, "Content delivery network service provider (CDNSP)-managed content delivery network (CDN) for network service provider (NSP)," *United States Patent* 7,376,727, filed December 11, 2006, issued May 20, 2008.

12. Steven C. Miller, Martin M. Deneroff, Curt F. Schimmel, Larry Rudolph, Charles E. Leiserson, Bradley C. Kuszmaul, and Krste Asanovic, "System and method for performing memory operations in a computing system," *United States Patent* 7,398,359, Filed April 30, 2004, issued July 8, 2008.

13. Charles E. Leiserson, Kunal Agrawal, Wen-Jing Hsu, and Yuxiong He, "Computing the Processor Desires of Jobs in an Adaptively Parallel Scheduling Environment," *United Stages Patent Application* 11/729,176, filed March 13, 2008.

14. Matteo Frigo, Charles E. Leiserson, Stephen T. Lewin-Berlin, "A method of implementing hyperobjects in a parallel processing software programming environment," *United States Patent Application* 12/247,420, filed October 8, 2008.

15. Steven C. Miller, Martin M. Deneroff, Curt F. Schimmel, Larry Rudolph, Charles E. Leiserson, Bradley C. Kuszmaul, and Krste Asanovic, "System and method for performing memory operations in a computing system," *United States Patent* 7,925,839, Filed July 7, 2008, issued April 12, 2011.

Teaching Experience of Charles E. Leiserson

Term	Subj.	Title	Role
ST 81	6.001	*Structure and Interpretation of Computer Programs*	Recitation (2 sections)
FT 81	6.032	*Computation Structures*	Recitation (2 sections)
ST 82	6.002	*Circuits and Electronics*	Recitation (2 sections)
FT 82	6.033	*Computer System Engineering*	Recitation (2 sections)
ST 83	6.045	*Computability, Automata, and Formal Languages*	Lectures, in charge
FT 83	6.045	*Computability, Automata, and Formal Languages*	Lectures, in charge
ST 84	6.895	*VLSI Algorithms*	Lectures, in charge
FT 84	6.001	*Structure and Interpretation of Computer Programs*	Recitation (2 sections)
FT 85	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 86	6.891	*Theory of Computing Machinery*	Lectures, in charge
FT 86	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 86	6.848	*Introduction to VLSI and Parallel Computation*	Lectures
ST 87	6.849	*Advanced VLSI and Parallel Computation*	Lectures, in charge
SS 87	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 87	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 87	6.848	*Introduction to VLSI and Parallel Computation*	Lectures
SS 88	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
ST 89	6.004	*Computation Structures*	Recitation (2 sections)
SS 89	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 89	6.046	*Introduction to Algorithms*	Lectures, in charge
SS 90	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 90	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 91	6.046	*Introduction to Algorithms*	Lectures, in charge
SS 91	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 91		Richard B. Adler Scholar (6.035 and 6.918)	
ST 92	6.851	*Theory of Algorithms*	Lectures, in charge
FT 92	6.004	*Computation Structures*	Recitation (1 section)
ST 93	6.851	*Theory of Algorithms*	Lectures, in charge
SS 93	6.84s	*Parallel Algorithms and Architectures*	Lectures, in charge
FT 93	6.042	*Mathematics for Computer Science*	Development, in charge
ST 94	6.042	*Mathematics for Computer Science*	Lectures, in charge
FT 94	6.042	*Mathematics for Computer Science*	Lectures, in charge
ST 95	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 96	CS413	*Introduction to Parallel Systems* (National University of Singapore)	Lectures, in charge
FT 96	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 97	6.892	*Theory of Parallel Systems*	Lectures, in charge
FT 98	6.972	*The Structure of Engineering Revolutions*	Development, in charge.
ST 98	6.046	*Introduction to Algorithms*	Lectures, in charge
ST 99	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 99	6.046	*Introduction to Algorithms*	Lectures, in charge
FT 01	6.046	*Introduction to Algorithms*	Lectures, in charge

ST	02 6.033	*Computer System Engineering*	Recitation (2 sections)
FT	02 6.042	*Mathematics for Computer Science*	Lectures, development
ST	03 6.042	*Mathematics for Computer Science*	Lectures, in charge
FT	03 6.895	*Theory of Parallel Systems*	Lectures, in charge
ST	04 6.895	*Theory of Parallel Hardware*	Lectures, in charge
FT	04 6.046	*Introduction to Algorithms*	Lectures, in charge
ST	05 6.046	*Introduction to Algorithms*	Lectures, in charge
FT	05 6.046	*Introduction to Algorithms*	Lectures, in charge
ST	06	*Leadership Skills for Engineering Faculty*	Lectures, in charge
SS	07 PI.61s	*Leadership Skills for Engineering and Science Faculty*	Lectures, in charge
FT	08 6.197	*Performance Engineering of Software Systems*	Lectures, in charge
SS	09 6.02s	*Concepts in Multicore Programming*	Lectures, in charge
SS	09 PI.61s	*Leadership Skills for Engineering and Science Faculty*	Lectures, in charge
FT	09 6.172	*Performance Engineering of Software Systems*	Lectures, in charge
ST	10 6.884	*Concepts in Multicore Programming*	Lectures, in charge
SS	10 PI.61s	*Leadership Skills for Engineering and Science Faculty*	Lectures, in charge
FT	10 6.172	*Performance Engineering of Software Systems*	Lectures, in charge
ST	11 6.046	*Design and Analysis of Algorithms*	Lectures, in charge
SS	11 PI.61s	*Leadership Skills for Engineering and Science Faculty*	Lectures, in charge
FT	11 6.172	*Performance Engineering of Software Systems*	Lectures, in charge
ST	12 6.172	*Performance Engineering of Software Systems*	Development
SS	12 PI.61s	*Leadership Skills for Engineering and Science Faculty*	Lectures, in charge
FT	12 6.172	*Performance Engineering of Software Systems*	Lectures, in charge
ST	13 6.UAT	*Preparation for Undergraduate Advanced Project*	Recitation (3 sections)

Publications of Charles E. Leiserson

16. Books

1. Charles E. Leiserson, *Area-Efficient VLSI Computation*, ACM Doctoral Dissertation Award Series, The MIT Press, Cambridge, Massachusetts, 1983. (Won the ACM award for best Ph.D. thesis in computer science for the 1981–1982 academic year, as well as the John and Fannie Hertz Foundation award for best Ph.D. thesis in 1981.)

2. Charles E. Leiserson, editor, *Advanced Research in VLSI,* The MIT Press, Cambridge, Massachusetts, 1986.

3. Thomas H. Cormen, Charles E. Leiserson, and Ronald L. Rivest, *Introduction to Algorithms*, The MIT Press and McGraw-Hill, 1990. Chosen by the Association of American Publishers as the Best 1990 Professional and Scholarly Book in Computer Science and Data Processing. Translated into 11 languages.

4. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein, *Introduction to Algorithms*, second edition, The MIT Press and McGraw-Hill, 2001. Translated into 15 languages.

5. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein, *Introduction to Algorithms*, third edition, The MIT Press, 2009. (The three editions have sold over 500,000 copies.)

17. Papers in Refereed Journals

1. Charles E. Leiserson and James B. Saxe, "Optimizing synchronous systems," *Journal of VLSI and Computer Systems,* Vol. 1, No. 1, Spring 1983, pp. 41–67. An early version appears in the *Twenty-Second Annual Symposium on Foundations of Computer Science,* IEEE Computer Society, November 1981, pp. 23–36.

2. Charles E. Leiserson and Ron Y. Pinter, "Optimal placement for river routing," *SIAM Journal on Computing,* Vol. 12, No. 3, August 1983, pp. 447–462. An early version appears in *CMU Conference on VLSI Systems and Computations,* Pittsburgh, Pennsylvania, October 1981, pp. 126–142.

3. Sandeep N. Bhatt and Charles E. Leiserson, "How to assemble tree machines," *Advances in Computing Research,* Vol. 2, 1984, pp. 95–114. An early version appears in the *Fourteenth Annual ACM Symposium on Theory of Computing,* San Francisco, California, ACM Special Interest Group for Automata and Computability Theory, May 1982, pp. 77–84.

4. Benny Chor, Charles E. Leiserson, Ronald L. Rivest, and James Shearer, "An application of number theory to the organization of raster-graphics memory," *JACM*, Vol. 33, No. 1, January 1986, pp. 86–104. An early version by the first three authors appears in the *Twenty-Third Annual Symposium on Foundations of Computer Science,* Chicago, Illinois, IEEE Computer Society, November 1982, pp. 92–99.

5. Tom Leighton and Charles E. Leiserson, "Wafer-scale integration of systolic arrays," *IEEE Transactions on Computers,* Vol. C-34, No. 5, May 1985, pp. 448–461. An early version appears in the *Twenty-Third Annual Symposium on Foundations of Computer Science,* Chicago, Illinois, IEEE Computer Society, November 1982, pp. 297–311.

6. Charles E. Leiserson, "Fat-trees: universal networks for hardware-efficient supercomputing," *IEEE Transactions on Computers,* Vol. C-34, No. 10, October 1985, pp. 892–901. An early version appears in the *1985 International Conference on Parallel Processing*, St. Charles, Illinois, IEEE Computer Society Press, August 1985, pp. 393–402. (Received Best Presentation Award at the conference.)

7. Ronald I. Greenberg and Charles E. Leiserson, "Randomized routing on fat-trees," *Advances in Computing Research*, Vol. 5, JAI Press, Inc., 1989, pp. 345–374. An early version appears in *Twenty-Sixth Annual Symposium on Foundations of Computer Science*, Portland, Oregon, IEEE Computer Society, October 1985, pp. 241–249.

8. Charles E. Leiserson and James B. Saxe, "A mixed-integer linear programming problem which is efficiently solvable," *Journal of Algorithms,* Vol. 9, 1988, pp. 114–128. An early version appears in *Twenty-First Annual Allerton Conference on Communication, Control, and Computing*, Department of Electrical Engineering and the Coordinated Science Laboratory of the

University of Illinois at Urbana-Champaign, Allerton House, Monticello, Illinois, October 1983, pp. 204–213.

9. Charles E. Leiserson and Bruce M. Maggs, "Communication-efficient parallel algorithms for distributed random-access machines," *Algorithmica*, Vol. 3, 1988, pp. 53–77. An early version appears as "Communication-efficient parallel graph algorithms," in *1986 International Conference on Parallel Processing,* St. Charles, Illinois, August 1986, pp. 861–868. (Received Most Original Paper Award at the conference.)

10. Ronald I. Greenberg and Charles E. Leiserson, "A compact layout for the three-dimensional tree of meshes," *Applied Mathematics Letters,* Vol. 1, No. 2, 1988, pp. 171–176.

11. Joe Kilian, Shlomo Kipnis, and Charles E. Leiserson, "The organization of permutation architectures with bussed interconnections," *IEEE Transactions on Computers*, Vol. 39, No. 11, November 1990, pp. 1346–1358. An early version appears in *Twenty-Eighth Annual Symposium on Foundations of Computer Science,* Syracuse, New York, IEEE Computer Society, October 1987, pp. 305–315.

12. Thomas H. Cormen and Charles E. Leiserson, "A hyperconcentrator switch for routing bit-serial messages," *Journal of Parallel and Distributed Computing*, Vol. 10, 1990, pp. 193–204. An early version appears in *1986 International Conference on Parallel Processing,* St. Charles, Illinois, August 1986, pp. 721–728. (Received Best Presentation Award at the conference.)

13. Charles E. Leiserson and James B. Saxe, "Retiming synchronous circuitry," *Algorithmica*, Vol. 6, 1991, pp. 5–35.

14. Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, W. Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, and Robert Zak, "The network architecture of the Connection Machine CM-5," *Journal of Parallel and Distributed Computing*, Vol. 33, No. 2, March 15, 1996, pp. 145–158. An early version appears in the *4th Annual ACM Symposium on Parallel Algorithms and Architectures*, San Diego, California, July 1992, pp. 272–285.

15. Robert D. Blumofe and Charles E. Leiserson, "Space-efficient scheduling of multithreaded computations," *SIAM Journal on Computing*, Vol. 7, No. 1, February 1998, pp. 202–229. An early version appears in *Proceedings of the 25th Symposium on Theory of Computing*, ACM, San Diego, California, May, 1993, pp. 362–371.

16. Robert D. Blumofe and Charles E. Leiserson, "Scheduling multithreaded computations by work stealing," *Journal of the ACM*, Vol. 46, No. 5, September 1999, pp. 720–748. An early version appears in the *Thirty-Fifth Annual Symposium on Foundations of Computer Science*, IEEE Computer Society, November 1994, pp. 356–368.

17. Robert D. Blumofe, Christopher F. Joerg, Bradley C. Kuszmaul, Charles E. Leiserson, Keith H. Randall, and Yuli Zhou, "Cilk: An efficient multithreaded runtime system," *Journal of Parallel and Distributed Computing*, Vol. 37, No. 1, August 1996, pp. 55–69. An early version appears in the *Fifth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, July 1995, pp. 207–216.

18. Alexander T. Ishii, Charles E. Leiserson, and Marios Papaefthymiou, "Optimizing two-phase, level-clocked circuitry," *Journal of the ACM*, Vol. 44, No. 1, January 1997, pp. 148–199. An early version appears in the *Brown/MIT Conference on Advanced Research in VLSI and Parallel Systems*, Providence, Rhode Island, March 1992, pp. 245–264.

19. Charles E. Leiserson and Keith H. Randall, "Parallel algorithms for the circuit value update problem," *Theory of Computing Systems*, Vol. 30, 1997, pp. 583–597. An early version appears in the *Seventh Annual ACM Symposium on Parallel Algorithms and Architectures*, July 1995, pp. 13–20.

20. Guy E. Blelloch, Charles E. Leiserson, Bruce M. Maggs, C. Gregory Plaxton, Stephen J. Smith, and Marco Zagha, "An experimental analysis of parallel sorting algorithms," *Theory of Computing Systems*, Vol. 31, No. 2, 1998, pp. 135–167. An early version appears under the title, "A comparison of sorting algorithms for the Connection Machine CM-2," in the *3rd Annual ACM Symposium on Parallel Algorithms and Architectures*, Hilton Head, South Carolina, July 1991, pp. 3–16.

21. Don Dailey and Charles E. Leiserson, "Using Cilk to write multiprocessor chess programs," *Advances in Computer Games*, H.J. van den Herik and B. Monien, eds., volume 9, University of Maastricht, 2001, pp. 25–52.

22. C. Scott Ananian, Krste Asanovic, Bradley C. Kuszmaul, Charles E. Leiserson, Sean Lie, "Unbounded transactional memory," *IEEE Micro*, Vol. 26, No. 1, January 2006, pp. 59–69. (Won the *IEEE Micro* "Top Picks" Award for the most industry relevant and significant papers of the year in computer architecture.) An early version appeared in *11th International Symposium on High-Performance Computer Architecture*, San Francisco, CA, February, 2005, pp. 316–327.

23. John S. Danaher, I-Ting Angelina Lee, and Charles E. Leiserson, "Programming with exceptions in JCilk," *Science of Computer Programming*, Vol. 63, No. 2, December 2006, pp. 147–171.

24. Yuxiong He, Wen Jing Hsu, and Charles E. Leiserson, "Provably efficient online nonclairvoyant adaptive scheduling," *IEEE Transactions on Parallel and Distributed Systems*, Vol. 19, No. 9, Feb. 2008, pp. 1263–1279. An early version appeared in *2007 IEEE International Parallel and Distributed Processing Symposium (IPDPS)*, Long Beach, CA, March 2007, pp. 1–10.

25. Kunal Agrawal, Yuxiong He, Wen Jing Hsu, and Charles E. Leiserson, "Adaptive scheduling with parallelism feedback," *ACM Transactions on Computing Systems*, Vol. 16, No. 3, September 2008, pp. 7:1–7:32. An early version appeared in the *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, March 2006, pp. 100–109.

26. Charles E. Leiserson, "The Cilk++ concurrency platform," *Journal of Supercomputing*, Vol. 51, No. 3, March 2010, pp. 244–257.

27. Matteo Frigo, Charles E. Leiserson, Harald Prokop, and Sridhar Ramachandran, "Cache-oblivious algorithms," *ACM Transactions on Algorithms*, January 2012.

Papers in Proceedings of Refereed Conferences

(*Other than early versions of those above.*)

1. H. T. Kung and Charles E. Leiserson, "Systolic arrays (for VLSI)," *Sparse Matrix Proceedings 1978,* I. S. Duff and G. W. Stewart, ed., Knoxville, Tennessee, Society for Industrial and Applied Mathematics, 1979, pp. 256–282.

2. Charles E. Leiserson, "Systolic priority queues," *Proceedings of the Caltech Conference on Very Large Scale Integration,* Charles L. Seitz, ed., Pasadena, California, January 1979, pp. 199–214.

3. Dan Hoey and Charles E. Leiserson, "A layout for the shuffle-exchange network," *1980 International Conference on Parallel Processing,* August 1980, pp. 329–336.

4. Charles E. Leiserson, "Area-efficient graph layouts (for VLSI)," *Twenty-First Annual Symposium on Foundations of Computer Science,* Syracuse, New York, IEEE Computer Society, October 1980, pp. 270–281.

5. Charles E. Leiserson, Flavio M. Rose, and James B. Saxe, "Optimizing synchronous circuitry by retiming," *Third Caltech Conference on VLSI,* Randal Bryant, ed., Pasadena, California, March 1983, pp. 87–116.

6. Charles E. Leiserson, "Systolic and semisystolic design," *IEEE International Conference on Computer Design/VLSI in Computers (ICCD '83),* Rye, New York, October 1983, pp. 627–632.

7. Kyle A. Gallivan and Charles E. Leiserson, "High-performance architectures for adaptive filtering," *SPIE Conference on Real Time Signal Processing*, Vol. 495, No. 7, San Diego, California, August 1984, pp. 30–38.

8. Charles E. Leiserson and F. Miller Maley, "Algorithms for routing and testing routability of planar VLSI layouts," *Proceedings of the 17th Symposium on Theory of Computing,* ACM, Providence, Rhode Island, May 1985, pp. 69–78.

9. Alexander T. Ishii and Charles E. Leiserson, "A timing analysis of level-clocked circuitry," *Proceedings of the Sixth MIT Conference on Advanced Research in VLSI*, April 1990, pp. 113–130.

10. Charles E. Leiserson, Satish Rao, and Sivan Toledo, "Efficient out-of-core algorithms for linear relaxation using blocking covers," *Thirty-Fourth Annual Symposium on Foundations of Computer Science,* IEEE Computer Society, November 1993, pp. 704–713.

11. Robert D. Blumofe, Matteo Frigo, Christopher F. Joerg, Charles E. Leiserson, and Keith H. Randall, "Dag-consistent distributed shared memory," *Tenth International Parallel Processing Symposium*, IEEE Computer Society, April 1996, pp. 132–141.

12. Robert D. Blumofe, Matteo Frigo, Christopher F. Joerg, Charles E. Leiserson, and Keith H. Randall, "An analysis of dag-consistent distributed shared-memory algorithms," *Eighth Annual ACM Symposium on Parallel Algorithms and Architectures*, June 1996, pp. 297–308.

13. Charles E. Leiserson, "Programming irregular parallel applications in Cilk," *Solving Irregularly Structured Problems in Parallel: 4th International Symposium, IRREGULAR'97*, Paderborn, Germany, June 1997, Springer-Verlag, pp. 61–71.

14. Mingdong Feng and Charles E. Leiserson, "Efficient detection of determinacy races in Cilk programs," *Ninth Annual ACM Symposium on Parallel Algorithms and Architectures*, June 1997, pp. 1–11.

15. Matteo Frigo, Charles E. Leiserson, and Keith Randall, "The implementation of the Cilk-5 multithreaded language," *1998 ACM SIGPLAN Conference on Programming Language Design and Implementation*, Montreal, Canada, June 1998, pp. 212–223. (Won the 2008 retrospective award for Most Influential Paper.)

16. Guang-Ien Cheng, Mingdong Feng, Charles E. Leiserson, Keith H. Randall, and Andrew F. Stark, "Detecting data races in Cilk programs that use locks," *Tenth ACM Symposium on Parallel Algorithms and Architectures*, June 1998, pp. 298–309.

17. Matteo Frigo, Charles E. Leiserson, Harald Prokop, and Sridhar Ramachandran, "Cache-oblivious algorithms," *40th Annual Symposium on Foundations of Computer Science*, New York, New York, October 17–19, 1999, pp. 285–297.

18. Ching Law and Charles E. Leiserson, "A new competitive analysis of randomized caching," *Eleventh Annual International Symposium on Algorithms And Computation*, December 2000, pp. 35–46.

19. Michael A. Bender, Jeremy T. Fineman, Seth Gilbert, and Charles E. Leiserson, "On-the-fly maintenance of series-parallel relationships in fork-join multithreaded programs," *16th Annual ACM Symposium on Parallelism in Algorithms and Architectures*, June 2004, pp. 133–144.

20. Michael A. Bender, Martin Farach-Colton, Simai He, Bradley C. Kuszmaul, and Charles E. Leiserson, "Adversarial analyses of window backoff strategies for simple multiple-access channels," *ACM Symposium on Parallelism in Algorithms and Architectures*, July 2005, pp. 325–332.

21. John S. Danaher, I-Ting Angelina Lee, and Charles E. Leiserson, "The JCilk language for multithreaded computing," *Synchronization and Concurrency in Object-Oriented Languages, OOPSLA 2005 Workshop*, October 2005.

22. Yuxiong He, Wen-Jing Hsu, and Charles E. Leiserson, "Provably efficient two-level adaptive scheduling," *12th Workshop on Job Scheduling Strategies for Parallel Processing*, Saint Malo, France, June 2006, pp. 1–32.

23. Kunal Agrawal, Yuxiong He, and Charles E. Leiserson, "An empirical evaluation of work stealing with parallelism feedback," *Proceedings of the International Conference on Distributed Computing Systems (ICDCS)*, July, 2006.

24. Kunal Agrawal, Yuxiong He, and Charles E. Leiserson, "Work stealing with parallelism feedback," *26th International Conference on Distributed Computing Systems*, Lisboa, Portugal, July 2006.

25. Kunal Agrawal, Charles E. Leiserson, and Jim Sukha, "Memory models for open-nested transactions," *Proceedings of the ACM SIGPLAN Workshop on Memory Systems Performance and Correctness*, October 2006.

26. Kunal Agrawal, Yuxiong He, and Charles E. Leiserson, "Adaptive work stealing with parallelism feedback," *12th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, San Jose, CA, March 2007, pp. 112-120.

27. Edya Ladan-Mozes and Charles E. Leiserson, "A consistency architecture for hierarchical shared caches," *ACM Symposium on Parallelism in Algorithms and Architectures*, June 2008, pp. 11–22.

28. Charles E. Leiserson, "The Cilk++ concurrency platform," *DAC '09: Proceedings of the 46th Annual Design Automation Conference*, San Francisco, CA, July 2009, pp. 522–527.

29. Aydın Buluç, Jeremy T. Fineman, Matteo Frigo, John R. Gilbert, and Charles E. Leiserson, "Parallel sparse matrix-vector and matrix-transpose-vector multiplication using compressed sparse blocks," *ACM Symposium on Parallelism in Algorithms and Architectures*, August 2009, pp. 233–244.

30. Matteo Frigo, Pablo Halpern, Charles E. Leiserson, and Stephen Lewin-Berlin, "Reducers and other Cilk++ hyperobjects," *ACM Symposium on Parallelism in Algorithms and Architectures*, August 2009, pp. 79–90. (Won Best Paper Award.)

31. Kunal Agrawal, Charles E. Leiserson, and Jim Sukha, "Helper locks for fork-join parallel programming," *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, January 2010, pp. 245–256.

32. Kunal Agrawal, Charles E. Leiserson, and Jim Sukha, "Executing task graphs using work stealing," *IEEE International Parallel and Distributed Processing Symposium*, April 2010, pp. 1–12.

33. Yuxiong He, Charles E. Leiserson, and William M. Leiserson, "The Cilkview scalability analyzer," *ACM Symposium on Parallelism in Algorithms and Architectures*, June 2010, pp. 145–156.

34. Charles E. Leiserson and Tao B. Schardl, "A work-efficient parallel breadth-first search algorithm (or how to cope with the nondeterminism of reducers)," *ACM Symposium on Parallelism in Algorithms and Architectures*, June 2010, pp. 303–314.

35. Charles E. Leiserson, Liyun Li, Marc Moreno Maza, and Yuzhen Xie, "Parallel computation of the minimal elements of a poset," *International Workshop on Parallel and Symbolic Computation*, July 2010, pp. 53–62.

36. Charles E. Leiserson, Liyun Li, Marc Moreno Maza, and Yuzhen Xie, "Efficient evaluation of large polynomials," *International Congress on Mathematical Software*, September 2010, pp. 342–353.

37. I-Ting Angelina Lee, Silas Boyd-Wickizer, Zhiyi Huang, and Charles E. Leiserson, "Using memory mapping to support cactus stacks in work-stealing runtime systems," *International Conference on Parallel Architectures and Compilation Techniques*, September 2010, pp. 411–420.

38. Yuan Tang, Rezaul Chowdhury, Chi-Keung Luk, and Charles E. Leiserson, "Coding stencil computations using the Pochoir stencil-specification language," *USENIX Workshop on Hot Topics in Parallelism*, May 2011, available from `http://www.usenix.org/events/hotpar11/poster.html`.

39. Yuan Tang, Rezaul Chowdhury, Bradley C. Kuszmaul, Chi-Keung Luk, and Charles E. Leiserson, "The Pochoir stencil compiler," *ACM Symposium on Parallelism in Algorithms and Architectures*, June 2011, pp. 117–128.

40. Charles E. Leiserson, Tao B. Schardl, and Jim Sukha, "Deterministic Parallel Random-Number Generation for Dynamic-Multithreading Platforms," *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, January 2012, pp. 193–204.

41. I-Ting Angelina Lee, Aamir Shafi, and Charles E. Leiserson, "Memory-mapping support for reducer hyperobjects," *ACM Symposium on Parallelism in Algorithms and Architectures*, June 2012, pp. 287–297. (Won Best Paper Award.)

42. Kunal Agrawal, Jeremy T. Fineman, Jordan Krage, Charles E. Leiserson, and Sivan Toledo, "Cache-Conscious Scheduling of Streaming Applications," *ACM Symposium on Parallelism in Algorithms and Architectures*, June 2012, pp. 236–245.

Other Major Publications

1. H. T. Kung and Charles E. Leiserson, "Algorithms for VLSI processor arrays," Chapter 8.3 of *Introduction to VLSI Systems* by Carver A. Mead and Lynn A. Conway, Addison-Wesley, 1978.

2. Charles E. Leiserson, Jill P. Mesirov, Lena Nekludova, Stephen M. Omohundro, and John Reif, "Solving sparse linear systems via parallel nested dissection on the Connection Machine," *SIAM 1986 National Meeting*, Boston, Mass., July 1986. Also appears as a Thinking Machines Corporation technical memorandum (unnumbered).

3. Tom Leighton and Charles E. Leiserson, "A survey of algorithms for integrating wafer-scale systolic arrays," in *Wafer-Scale Integration*, G. Saucier and J. Trilhe, eds., North-Holland, 1986, pp. 177–195.

4. Charles E. Leiserson and John G. Lewis, "Orderings for parallel sparse symmetric factorization," Chapter 5 of *Parallel Processing for Scientific Computing*, Garry Rodrigue, ed., SIAM, 1989.

5. Charles E. Leiserson, "VLSI theory and parallel supercomputing," Chapter 2 of *Carnegie Mellon University School of Computer Science 25th Anniversary Symposium*, Richard F. Rashid, ed., Addison-Wesley, 1991, pp. 29–44. An early version appeared in *Decennial Caltech Conference on VLSI*, March 1989, The MIT Press, pp. 5–16.

6. Charles E. Leiserson, "Timekeeper," *SIGACT News*, Vol. 23, No. 4, ACM Press, Fall 1992, pp. 81–82.

7. Charles E. Leiserson and Aske Plaat, "Programming parallel applications in Cilk," *SIAM News*, Vol. 31, No. 4, May 1998, pp. 6–7.

8. Erik D. Demaine, Martin L. Demaine, Alan Edelman, Charles E. Leiserson, and Per-Olof Persson, "Building blocks and excluded sums," SIAM News, Volume 38, Number 1, January/February 2005.

9. Charles E. Leiserson and Ilya Mirman, "How to survive the multicore software revolution (or at least survive the hype)," *Journal of Advancing Technology*, Vol. 9, Summer 2009, pp. 42–53.

Internal Memoranda and Progress Reports

(*Other than early versions of those above.*)

1. Sandeep N. Bhatt and Charles E. Leiserson, "Minimizing the longest edge in a VLSI layout," MIT VLSI Memo No. 82-86, May 1981.

2. Charles E. Leiserson and Cynthia A. Phillips, "A space-efficient algorithm for finding the connected components of rectangles in the plane," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-323, February 1987.

3. Charles E. Leiserson and Cynthia A. Phillips, "Parallel contraction of planar graphs," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-343, October 1987.

4. Tom Leighton, Charles E. Leiserson, Bruce Maggs, Serge Plotkin, and Joel Wein, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 1, March 1988.

5. Tom Leighton, Charles E. Leiserson, Bruce Maggs, Serge Plotkin, and Joel Wein, "Advanced Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 2, March 1988.

6. C. E. Leiserson, F. T. Leighton, and S. A. Plotkin, editors, "Connection Machine Projects," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 4, January 1989.

7. Tom Leighton, Charles E. Leiserson, and Eric Schwabe, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 6, March 1989.

8. Tom Leighton and Charles E. Leiserson, "Advanced Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 7, December 1989.

9. Tom Leighton, Charles E. Leiserson, and Dina Kravets, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 8, May 1990.

10. Charles E. Leiserson, editor, "Proceedings of the 1991 MIT Student Workshop on VLSI and Parallel Systems," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-513, August 1991.

11. Alexander T. Ishii, Charles E. Leiserson, and Marios C. Papaefthymiou, "An algorithm for the tramp steamer problem based on mean-weight cycles," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-457, November 1991.

12. Charles E. Leiserson, editor, "Proceedings of the 1992 MIT Student Workshop on VLSI and Parallel Systems," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-546, August 1992.

13. Charles E. Leiserson, editor, "Proceedings of the 1993 MIT Student Workshop on Supercomputing Technologies," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-575, August 1993.

14. Phillip B. Gibbons, Richard M. Karp, Charles E. Leiserson, Gregory M. Papadopoulos, editors, "DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation," DIMACS Center for Discrete Mathematics and Theoretical Computer Science, Technical Report 93-87, September, 1993.

15. Charles E. Leiserson, editor, "Proceedings of the 1994 MIT Student Workshop on Supercomputing Technologies," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-622, July 1994.

16. Supercomputing Technologies Group, MIT Laboratory for Computer Science, *Cilk-5.2 (Beta 1) Reference Manual*, unpublished manuscript, available on the World Wide Web at `http://supertech.lcs.mit.edu/cilk`, 1998. Earlier versions of this manual are also available.

17. Charles E. Leiserson, Harald Prokop, and Keith H. Randall, "Using de Bruijn sequences to index a 1 in a computer word," unpublished manuscript, available on the World Wide Web at `http://supertech.lcs.mit.edu/cilk`, 1998.

18. Charles E. Leiserson and Harald Prokop, "A minicourse on multithreaded programming," unpublished manuscript, available on the World Wide Web at `http://supertech.lcs.mit.edu/cilk`, 1999.

Invited Lectures

Systolic Systems
May 1981 MIT, Cambridge, Massachusetts

Optimizing Synchronous Systems

July 1981 Digital Equipment Corporation, Maynard, Massachusetts
Sep. 1981 Harvard University, Cambridge, Massachusetts
Dec. 1981 MIT Lincoln Laboratory, Lexington, Massachusetts

Optimal Placement for River Routing
Dec. 1981 MIT, Cambridge, Massachusetts

Digital Circuit Optimization
May 1982 MIT, Cambridge, Massachusetts

Optimization of Digital Circuitry by Retiming
Oct. 1982 Duke University, Durham, North Carolina
Nov. 1982 University of Rochester, Rochester, New York
Jan. 1983 Bell Laboratories, Murray Hill, New Jersey
Apr. 1984 Brown University, Providence, Rhode Island

Wafer-Scale Integration of Systolic Arrays
Nov. 1982 Carnegie-Mellon University, Pittsburgh, Pennsylvania
Mar. 1983 University of California at Berkeley, Berkeley, California
July 1983 MIT, Cambridge, Massachusetts

Systolic and Semisystolic Systems
July 1983 MIT, Cambridge, Massachusetts
July 1983 Harris Corporation, Melbourne, Florida

Systolic and Semisystolic Design
Aug. 1983 AT&T Bell Laboratories, Murray Hill, New Jersey
Aug. 1983 Princeton University, Princeton, New Jersey

Fat-Trees: Universal Networks for Hardware-Efficient Supercomputing
June 1984 MIT, Cambridge, Massachusetts
June 1984 AT&T Bell Laboratories, Murray Hill, New Jersey
Oct. 1984 IBM Research, Yorktown Heights, New York
Jan. 1985 Bolt, Baranek, and Newman, Inc., Cambridge, Massachusetts
Jan. 1985 Stanford University, Stanford, California
Jan. 1985 University of California at Berkeley, Berkeley, California
Jan. 1985 Lawrence Livermore National Laboratory, Livermore, California
Feb. 1985 University of Minnesota, Minneapolis, Minnesota
Feb. 1985 University of Toronto, Toronto, Canada
Mar. 1985 Cornell University, Ithaca, New York
Apr. 1985 New York University, New York, New York
Apr. 1985 Thinking Machines Corporation, Cambridge, Massachusetts

The Relevance of VLSI Theory to Parallel Supercomputing
Jan. 1986 Microelectronics and Computer Technology Corporation

Workshop on Interconnection Networks, Austin, Texas
May 1986 Mathematical Sciences Research Institute, Berkeley, California
June 1986 SIAM Annual Conference, Boston, Massachusetts
Nov. 1987 Siemens-MIT Conference, Munich, West Germany

Communication-Efficient Parallel Graph Algorithms
Oct. 1986 Graph Theory Day (New York Academy of Sciences), Albany, New York

New Machine Models for Synchronous Parallel Algorithms
Dec. 1987 Institute for Mathematics and Its Applications, University of Minnesota, Minneapolis, Minnesota

Very Large Scale Computing
Oct. 1988 Project MAC 25th Anniversary Symposium, MIT, Cambridge, Massachusetts

VLSI Theory and Parallel Supercomputing
Mar. 1989 Decennial Caltech Conference on VLSI, California Institute of Technology, Pasadena, California
Apr. 1989 Thinking Machines Corporation, Cambridge, Massachusetts
Sep. 1990 CMU School of Computer Science 25th Anniversary Symposium, Carnegie Mellon University, Pittsburgh, Pennsylvania
Oct. 1990 Texas Instruments Corporation, Dallas, Texas
Dec. 1990 NEC Research Institute, Princeton, New Jersey
Apr. 1992 AT&T Bell Laboratories, Holmdel, New Jersey

Highly Reliable Large-Scale Computing
Nov. 1990 MIT VLSI Research Review, Cambridge, Massachusetts

A Comparison of Sorting Algorithms for the Connection Machine CM-2
Mar. 1991 Purdue University, West Lafayette, Indiana
Mar. 1991 Indiana University, Bloomington, Indiana
Oct. 1991 University of Texas, Austin, Texas
Nov. 1991 Yale University, New Haven, Connecticut

Engineering Parallel Algorithms
May 1991 Second Annual Workshop on Parallel Algorithms, New Orleans, Louisiana

The Network Architecture of the Connection Machine CM-5
Nov. 1991 Yale University, New Haven, Connecticut
Nov. 1991 Sandia National Laboratory, Albuquerque, New Mexico
Apr. 1992 Carnegie Mellon University, Pittsburgh, Pennsylvania
Apr. 1992 MIT, Cambridge, Massachusetts

May 1992 University of Washington, Seattle, Washington
June 1992 Dartmouth Institute for Advanced Graduate Studies, Hanover, New Hampshire
Sep. 1992 International Conference on Parallel Processing Ecole Normale Supérieure de Lyon, Lyon, France
Sep. 1992 Commisariat à l'Energie Atomique, Saclay, France
Sep. 1992 Thinking Machines Corporation, Cambridge, Massachusetts
Sep. 1992 DARPA Joint Microsystems/Computer Systems/HPC Software PI Meeting Daytona, Florida
Oct. 1992 Symposium on New Directions in Parallel and Concurrent Computing New York, New York
Oct. 1992 IEEE Foundations of Computer Science Conference (informal, invited presentation), Pittsburgh, Pennsylvania
Nov. 1992 International Heinz Nixdorf Symposium on Parallel Architectures and Their Efficient Use, Paderborn, Germany
Dec. 1992 IEEE Symposium on Parallel and Distributed Processing (keynote) Dallas, Texas
Dec. 1992 Princeton University, Princeton, New Jersey
Dec. 1992 University of Massachusetts, Amherst, Massachusetts
Feb. 1993 Stanford University, Stanford, California
July 1993 International Workshop on Interconnection Networks, Marseille, France
Sep. 1993 University of Zurich, Zurich, Switzerland
Sep. 1993 Max Planck Institut für Informatik, Saarbrücken, Germany

A Menagerie of Parallel Computing Networks
June 1991 MIT Technology Day, Cambridge, Massachusetts

Special-Purpose vs. General-Purpose Parallel Computing Networks
Aug. 1992 International Conference on Application-Specific Array Processors San Francisco, California (keynote)

How to Interconnect One Million Processors (panel session)
Oct. 1992 Frontiers of Massively Parallel Computation, McLean, Virginia

Space-Efficient Scheduling of Multithreaded Computations
Sep. 1993 DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation, Rutgers University, New Jersey
Dec. 1993 Université de Paris-Sud, Paris, France
Apr. 1994 Columbia University Theory Day, New York, New York
Sep. 1994 Carleton University, Ottawa, Canada

Efficient Scheduling of Multithreaded Computations
Mar. 1995 National University of Singapore, Singapore
Apr. 1995 Distinguished Lecture, Carnegie Mellon University, Pittsburgh, Pennsylvania
Apr. 1995 Harvard University, Cambridge, Massachusetts

Sep. 1995 Workshop on High-Performance Computing Activities in Singapore
National Supercomputing Research Centre, Singapore

What Is Theoretical Computer Science?

Mar. 1996 Keynote Address, Science Research Seminar, National University of Singapore

Can Multithreaded Programming Save Massively Parallel Computing?

Apr. 1996 Keynote Address, International Parallel Processing Symposium, Honolulu, Hawaii
May 1996 GINTIC Institute of Manufacturing Technology, Singapore

Algorithmic Multithreaded Computing

June 1996 Keynote Address, International Conference on Algorithms and Architectures for Parallel Processing, Singapore
Sep. 1996 Distinguished Lecture, Courant Institute, NYU, New York, New York
Nov. 1996 Theory of Computation Seminar, MIT, Cambridge, MA
Nov. 1996 Distinguished Lecture, University of Maryland, College Park, MD

Efficient Detection of Determinacy Races in Cilk Programs

Jan. 1997 National University of Singapore, Singapore
Jan. 1997 Dartmouth College, Hanover, New Hampshire
June 1997 Max Planck Institut für Informatik, Saarbrücken, Germany
Nov. 1997 Distinguished Lecture, University of California, Santa Barbara
Jan. 1998 DEC Systems Research Center, Palo Alto, CA

Teaching Parallel Algorithms using the Cilk Multithreaded Programming Language

June 1997 Forum on Parallel Computing Curricula, Newport, RI
June 1998 Yale Workshop on Multithreaded Algorithms, New Haven, CT
July 1998 National University of Singapore, Singapore
July 1998 Academia Sinica, Taipei, Taiwan

Algorithmic Multithreaded Programing Using Cilk

July 1997 National University of Singapore, Singapore
Jan. 1998 NASA Ames Research Center, Moffett Field, CA
Jan. 1998 Silicon Graphics, Inc., Mountain View, CA
Jan. 1998 Sun Microsystems, Inc., Palo Alto, CA
Aug. 1998 11th International Workshop on Languages and Compilers for Parallel Computing, Chapel Hill, NC

Programming Shared-Memory Multiprocessors Using the Cilk Multithreaded Language

Sep. 1998 MIT EECS Department Colloquium, Cambridge, MA
Sep. 1998 Intel Corporation, Beaverton, OR
Sep. 1998 University of California, Berkeley; Berkeley, CA
Oct. 1998 Stanford University, Stanford, CA
Oct. 1998 University of Delaware, Wilmington, DL
Nov. 1998 Rice University, Houston, TX

Dec. 1998 5th Intl. Conference on High-Performance Computing, Chennai, India
Jan. 1999 Workshop on Parallel Computing for Irregular Applications, Orlando, FL
Mar. 1999 NTT Corporation, Atsugi, Japan
Apr. 1999 Seminar on High-Level Parallel Programming, Dagstuhl, Germany
May 1999 Understanding the New World of Information '99, Taipei, Taiwan
Mar. 2003 George Washington University, Washington, DC
July 2004 Scandinavian Workshop on Algorithm Theory, Copenhagen, Denmark
Oct. 2004 Reflections Projections, University of Illinois, Urbana-Champaign, IL

Debugging Multithreaded Programs

Sep. 1998 Microsoft Research, Redmond, WA
Nov. 1998 University of Texas at Austin, Austin, TX

Design and Analysis of Algorithms for Shared-Memory Multiprocessors

May 1999 Workshop on Parallel Algorithms, Atlanta, GA
Aug. 1999 Workshop on Algorithms and Data Structures, Vancouver, CA

Using Cilk to Write Multiprocessor Chess Programs

June 1999 International Conference on Computer Chess, Paderborn, Germany

Cache-Oblivious Algorithms

June 2004 Seminar on Cache-Oblivious and Cache-Aware Algorithms, Dagstuhl, Germany
July 2005 Computational Research in Boston, Cambridge, MA

Unbounded Transactional Memory

Apr. 2005 Workshop on Transactional Systems, Chicago, IL
Sep. 2005 Workshop on High-Performance Embedded Systems, Lexington, MA
Oct. 2005 University of Rochester, Rochester, NY
Jan. 2006 Intel Corporation, Cambridge, MA

MIT.001 Final Exam

Sep. 2005 CSAIL Student Workshop, Gloucester, MA

Multithreaded Programming in Cilk

Dec. 2005 Keynote, 4th Intel Programming Systems Conference, Santa Clara, CA
June 2006 Keynote, International Workshop on OpenMP, Reims, France
Apr. 2007 Intel Research Laboratory, Berkeley, CA
Nov. 2007 Workshop on Manycore and Multicore Computing at *Supercomputing 2007*, Reno, NV

Leadership and Engineering

Apr. 2006 50th Anniversary Celebration of Computer Science at Carnegie Mellon, Pittsburgh, PA

Cache-Oblivious Jeopardy

Aug. 2007 Center for Massive Data Algorithmics (MADALGO) Inaugural Event

Cilk++: Multicore-Enabling Legacy C++ Code

Apr. 2008 Carnegie Mellon University, Pittsburgh, PA

Sept. 2008 University of California, Berkeley, CA

Multicore Programming in Cilk++

May 2009 Distinguished Visiting Professor, American University in Cairo

The Cilk++ Runtime System

May 2009 Distinguished Visiting Professor, American University in Cairo

Designing Cilk++ Algorithms

May 2009 Distinguished Visiting Professor, American University in Cairo

The Design and Analysis of Multithreaded Algorithms

July 2009 Plenary talk, SIAM Annual Meeting, Denver, CO

The Cilk++ Concurrency Platform

July 2009 Design Automation Conference Special Session on Multicore Computing and EDA, San Francisco, CA

Cilk++

Nov. 2009 The 21st IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS)

Cilk++ and Reducers

Jan. 2010 Indo-US Workshop on Parallelism and the Future of High Performance Computing, Bangalore, India

Reducers and Other Cilk++ Hyperobjects

Mar. 2010 Distinguished Lecture, University of Illinois at Urbana-Champaign, Champaign, IL

Nonnumeric Computing: A Cilk Perspective

Mar. 2010 Intel Workshop on Parallel Algorithms for Nonnumeric Computing Intel Corporation, Santa Clara, CA

Using Thread-Local Memory Mapping to Support Cactus Stacks in Work-Stealing Runtime Systems

Mar. 2010 Intel Corporation, Champaign, IL

The Pochoir Stencil Compiler

Apr. 2011 Distinguished Lecture, University of Connecticut, Storrs, CT

Oct. 2011 Applied Mathematics Colloquium, MIT, Cambridge, MA

Mar. 2012 Distinguished Lecture, University of Texas at Austin, Austin TX

Cilk Runtime Support for Deterministic Parallel Random-Number Generation
Mar. 2011 Invited Talk, The 2nd Workshop on Determinism and Correctness in Parallel Programming, Newport Beach, CA

Theses Supervised by Charles E. Leiserson

Summary

	Total	**Completed**	**In Progress**
S.B.	20	20	0
S.M.	19	19	0
M.Eng.	22	21	1
Engineers	1	1	0
Doctoral			
As Supervisor:	28	25	3
As Reader:	22	22	0

S.B. Theses and Advanced Undergraduate Projects

1. David H. Covert, *Graphic Objects That Draw Themselves,* May 1983.
2. Csaba Peter Gabor, *A Comparison of VLSI Designs for Complex Multiplication,* January 1984.
3. David J. Jilk, *Methodology for User-Aided Silicon Compilation,* January 1985.
4. Alexander T. Ishii, *A Comparison of Routing Algorithms for Fat-Tree Supercomputers,* May 1985.
5. Bruce M. Maggs, *Computing Minimum Spanning Trees on a Fat-Tree Architecture,* May 1985.
6. Marie J. Sullivan, *Parallel Graph Algorithms on the Connection Machine,* February 1987.
7. Vu Le Phan, *Massively Parallel Solutions to the Sparse Assignment Problem*, May 1991.
8. Michele L. Monclova, *An Experimental Comparison of Red-Black Trees and Skip Lists*, May 1991.
9. David B. Wilson, *Embedding Weak Hypercubes in Strong Hypercubes*, May 1991. (Winner of the William Martin Prize for best undergraduate computer science thesis at MIT.)
10. Keith Randall, *TIM: A CAD Tool for Designing Two-Phase Level-Clocked Circuitry*, May 1993.
11. Daniel Schmidt, *An Empirical Comparison of Four Heap Data Structures*, August 1994.

12. Tzu-Yi Chen, *Efficient Implementation of Out-of-Core Conjugate Gradient Algorithms*, May 1995. (Honorable Mention in the Computer Research Association's Outstanding Undergraduates Competition.)

13. Arup R. Guha, *Implementation of Band Cholesky Factorization in Cilk*, May 1997.

14. Adrian Soviani, 5×5 *Magic Squares in Cilk*, May 1999.

15. Svetoslav Tzvetkov, *Parallel Memory Allocation*, May 1999.

16. David Venturini, *Chess Endgame Database Compression*, May 1999.

17. John Danaher, *A Real-Time Distributed Score-Keeping System*, May 2004.

18. Tao Benjamin Schardl, *A Work-Efficient Parallel Breadth-First Search Algorithm*, May 2009. (Won the Robert M. Fano UROP Award for Outstanding EECS UROP and the Arnold L. Nylander Advanced Undergraduate Project Award.)

19. Boon Teik Ooi, *An Ordered-Set Reducer*, May 2012.

20. Tim Kaler, *Parallel Iterative Graph Computation*, May 2012.

S.M. Theses

1. Martin I. Eiger, *Analysis of Algorithms to Compute Wirings Within Test Fixtures,* June 1985.

2. Cynthia A. Phillips, *Space-Efficient Algorithms for Computational Geometry,* August 1985.

3. F. Miller Maley, *Compaction with Automatic Jog Introduction,* May 1986.

4. Thomas H. Cormen, *Concentrator Switches for Routing Messages in Parallel Computers,* August 1986.

5. Bruce M. Maggs, *Communication-Efficient Parallel Graph Algorithms,* August 1986.

6. Alexander T. Ishii, *A Digital Model for Level-Clocked Circuitry*, January 1989.

7. James A. Park, *Notes on Searching in Multidimensional Monotone Arrays*, January 1989.

8. Jeffrey A. Fried, *VLSI Processor Design for Communication Networks*, January 1989.

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