

**Massachusetts Institute of Technology  
School of Engineering Faculty Personnel Record**

**Date:** January 19, 2008

**Full Name:** Charles E. Leiserson

**Department:** Electrical Engineering and Computer Science

**1. Date of Birth:**

November 10, 1953

**2. Citizenship:**

U.S.A.

**3. Education:**

<b>School</b>	<b>Degree</b>	<b>Date</b>
Yale University	B. S. ( <i>cum laude</i> )	May 1975
Carnegie Mellon University	Ph.D.	Dec. 1981

**4. Title of Thesis for Most Advanced Degree:**

*Area-Efficient VLSI Computation*

**5. Principal Fields of Interest:**

Analysis of algorithms  
Parallel algorithms and architectures  
Digital hardware and computing machinery  
Supercomputing technologies  
Computer network architecture  
Parallel languages and runtime systems  
Parallel and distributed computing  
Scalable computing systems  
Distance education and interaction  
Computer chess Leadership and Engineering

**6. Name and Rank of Other Department Faculty in the Same Field:**

Anant Agarwal, Professor  
Saman Amarasinghe, Associate Professor  
Krstje Asanovic, Associate Professor  
Arvind, Professor  
Jack Dennis, Professor Emeritus  
Eric Demaine, Assistant Professor  
Shafi Goldwasser, Professor  
Piotr Indyk, Assistant Professor

David Karger, Associate Professor  
 Nancy A. Lynch, Professor  
 Albert R. Meyer, Professor  
 Silvio Micali, Professor  
 Martin Rinard, Associate Professor  
 Ronald L. Rivest, Professor  
 Madhu Sudan, Professor

### 7. Name and Rank of Faculty in Other Departments in the Same Field:

Alan Edelman, Professor (Mathematics)  
 Bonnie Berger, Professor (Mathematics)  
 Michel Goemans, Professor (Mathematics)  
 F. Thomson Leighton, Professor (Mathematics)  
 Michael F. Sipser, Professor (Mathematics)

### 8. Non-MIT Experience:

<b>Employer</b>	<b>Position</b>	<b>Beginning</b>	<b>Ending</b>
International Computing Centre ( <i>United Nations, Geneva, Switzerland</i> )	Programmer Assistant	Jun. 1973	Sep. 1973
Yale University ( <i>Department of Computer Science</i> )	Programmer	May 1974	Sep. 1974
POS Corporation ( <i>New Haven, CT</i> )	Software Consultant ( <i>part time</i> )	Sep. 1974	May 1975
Computervision Corporation ( <i>Bedford, MA</i> )	Programmer	Jun. 1975	Sep. 1976
Max Planck Institute für Informatik ( <i>Saarbrücken, Germany</i> )	Fachbeirat ( <i>Visiting Committee</i> )	Sep. 1992	present
Ecole Normale Supérieure de Lyon ( <i>Lyon, France</i> )	Visiting Professor	Jun. 1993	Jul. 1993
National University of Singapore ( <i>Republic of Singapore</i> )	Shaw Visiting Professor	Aug. 1995	Aug. 1996
Akamai Technologies	Director of System	Jun. 1999	

(Cambridge, MA)

Architecture

## 9. History of MIT Appointments:

<b>Rank</b>	<b>Beginning</b>	<b>Ending</b>
Assistant Professor	Jan. 1981	Jun. 1984
Associate Professor	Jul. 1984	Jun. 1988
Associate Professor (with tenure)	Jul. 1988	Jun. 1992
Professor	Jul. 1992	present

## 10. Consulting Record:

<b>Firm</b>	<b>Beginning</b>	<b>Ending</b>
MIT Lincoln Laboratory	Feb. 1982	Aug. 1984
AT&T Bell Laboratories	Jan. 1983	Dec. 1986
Harris Corporation (GASD)	Feb. 1983	May 1985
Cognition	Dec. 1984	June 1985
Analog Devices	Feb. 1985	Jun. 1985
Thinking Machines	July 1985	Aug. 1994
Harris Corporation (GCSD)	May 1986	Jun. 1986
W. W. Oliver Company	Jan. 1987	Jan. 1987
Wolfsort Corporation	Mar. 1991	Mar. 1991
National University of Singapore, Adjunct Professor	Sep. 1996	Aug. 2005
NKK Corporation	Mar. 1997	Mar. 1997
Pratt & Whitney	May 1997	Dec. 1999
EMC <sup>2</sup> Corporation	Jun. 1998	Feb. 1999
Akamai Technologies	Jun. 1999	present
Etisalat University, UAE	Apr. 2003	Aug. 2005
RealNetworks	May 2003	present

## 11. Department and Institute Committees, Other Assigned Duties:

<b>Activity</b>	<b>Beginning</b>	<b>Ending</b>
Graduate Counselor (EECS)	Sep. 1981	May 1988
Area II Committee (EECS)	Sep. 1981	May 1988
LCS Executive Committee	Sep. 1981	Sep. 1982
Graduate Admissions Committee (EECS)	Nov. 1981	May 1985
LCS Executive Committee	Sep. 1984	Dec. 1987
MIT/LCS Student Workshop (Chairman)	Jul. 1990	Jul. 1994
Undergraduate Advisor (EECS)	Sep. 1990	May 1995
VI-A liaison for IBM Research	Feb. 1991	Mar. 1993
MIT VLSI & Parallel Systems Student Workshop (Chairman)	May 1991	Jul. 1991
MIT VLSI & Parallel Systems Student Workshop (Chairman)	May 1992	Jul. 1992
Leader, Supercomputing Technologies Group	Sep. 1993	present
MIT Supercomputing Technologies Student Workshop (Chairman)	May 1993	Jul. 1993
Graduate Counselor (EECS)	Sep. 1996	present

Area II Committee (EECS)	Sep. 1996	present
EECS Professional Education Policy Committee	Mar. 1992	May 1993
MIT Commencement Committee	Sep. 1996	May 2001
Singapore Engineering Education Assessment Committee	Mar. 1997	Jun. 1998
MIT Student Workshop (Chairman)	Apr. 1997	Jul. 1997
EECS Client Building Committee	Apr. 1997	Jul. 1999
EECS Faculty Search Committee	Nov. 1998	Sep. 1999
UPOP Workshop Committee (Engineering Chair)	Sep. 2001	present

## 12. Government Committees, Service, etc.:

Activity	Date
NSF <i>Ad Hoc</i> Committee on Supercomputing Software	1985
DARPA/ISTO TeraOps Working Group	1987–1989
Joint DARPA/NSF and ESPRIT Exploratory Workshop on Information Science and Technology	1990

## 13. Awards Received:

Award	Date
Benjamin F. Barge Prize in Mathematics ( <i>Yale University</i> )	1972
Hertz Fellowship	1977
Hertz Doctoral Thesis Award	1982
ACM Doctoral Dissertation Award	1982
NSF Presidential Young Investigator Award	1985
IEEE Int. Conf. on Parallel Processing Best Presentation Award	1985
IEEE Int. Conf. on Parallel Processing Best Presentation Award (with Thomas H. Cormen)	1986
IEEE Int. Conf. on Parallel Processing Most Original Paper Award (with Bruce M. Maggs)	1986
Best 1990 Professional and Scholarly Book in Computer Science and Data Processing, Association of American Publishers (with Thomas H. Cormen and Ronald L. Rivest)	1990
Richard B. Adler Scholar, MIT EECS Department	1991
3rd Place in ACM International Computer Chess Championship for StarTech	1993
3rd Place in ACM International Computer Chess Championship for ★Socrates	1994
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'95	1995
2nd Place in ICCA 8th Computer Chess World Championship for ★Socrates 2.0	1995
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'96	1996
1st Place in Dutch Open Computer Chess Championship for Cilkchess	1996
IEEE Computer Society Distinguished Visitor for the Asia-Pacific Region	1996–1998
Recognition of Service Award by ACM for service as Conference General Chair for SPAA'97	1997
2nd Place in Dutch Open Computer Chess Championship for Cilkchess	1997

1st Prize in the International Conference on Functional Programming's ICFP Programming Contest	1998
2nd Place in Dutch Open Computer Chess Championship for Cilkchess	1998
<i>IEEE Micro</i> Top Picks for "Unbounded Transactional Memory"	2006
ACM Fellow	2007
Margaret MacVicar Faculty Fellow, MIT	2007–present

#### 14. Organization Membership:

##### Organization

AAAS

ACM

IEEE

SIAM

ACM Turing Award Committee

*Journal of VLSI and Computer Systems*

1982 MIT VLSI Conference

1984 MIT VLSI Conference

1986 MIT VLSI Conference Committee

Springer-Verlag Texts and Monographs  
in Computer Science

1986 IEEE Symposium on Foundations  
of Computer Science

*Journal of Parallel and Distributed Computing*

*Applied Mathematics Letters*

1989 ACM Symposium on Parallel Algorithms  
and Architectures

1989 IEEE Symposium on Foundations  
of Computer Science

Supercomputing '91

1993 DIMACS Workshop on Models, Architectures, and  
Technologies for Parallel Computation

1994 ACM Symposium on Parallel Algorithms  
and Architectures

ACM Symposium on Parallel Algorithms  
and Architectures

*Journal of Computer and Systems Science*

SC'xy Steering Committee, 1999

*Journal of Parallel and Distributed Computing*

2003 ACM SIGPLAN Symposium on Principles and  
Practice of Parallel Programming

Dagstuhl Seminar 04301 in Cache-Oblivious and  
Cache-Aware Algorithms

##### Offices Held

1983–1987, (Chair, 1986)

Editor, 1983–1985

Program Committee

Program Committee

Program Chair

Editorial Board, 1986–1993

Program Committee

Editor, 1986–1988

Editor, 1987–1990

Program Committee

Program Committee

Program Committee

Organizing Committee

Program Chair

General Chair, 1994–1997

Guest Editor, 1996

Advisory Board, 1999

Program Committee

Organizer, 2004

## 15. Patents and Patent Applications Pending:

1. H. T. Kung and Charles E. Leiserson, "Systolic array apparatuses for matrix computations," *United States Patent* 4,493,048, filed May 16, 1983, issued January 8, 1985.
2. Thomas H. Cormen and Charles E. Leiserson, "Message merging device," *United States Patent* 4,922,246, filed November 25, 1986, issued May 1, 1990.
3. Robert C. Zak, Charles E. Leiserson, Bradley C. Kuszmaul, Shaw-Wen Yang, W. Daniel Hillis, David C. Douglas, and David Potter, "Parallel computer system including arrangement for transferring messages from a source processor to selected ones of a plurality of destination processors and combining responses," *United States Patent* 5,265,207, filed April 8, 1993, issued November 23, 1993.
4. David C. Douglas, Mahesh N. Ganmukhi, Jeffrey V. Hill, W. Daniel Hillis, Bradley C. Kuszmaul, Charles E. Leiserson, David S. Wells, Monica C. Wong, Shaw-Wen Yang, and Robert C. Zak, Jr., "Parallel computer system," *United States Patent* 5,333,268, filed September 16, 1992, issued July 26, 1994.
5. Charles E. Leiserson, Robert C. Zak, Jr., W. Daniel Hillis, Bradley C. Kuszmaul, and Jeffrey V. Hill, "Parallel computer system including request distribution network for distributing processing requests to selected sets of processors in parallel," *United States Patent* 5,388,214, filed January 14, 1994, issued February 7, 1995.
6. Bradley C. Kuszmaul, Charles E. Leiserson, Shaw-Wen Yang, Carl R. Feynman, W. Daniel Hillis, David Wells, and Cynthia J. Spiller, "Parallel computer system including arrangement for quickly draining messages from message router," *United States Patent* 5,390,298, filed January 14, 1994, issued February 14, 1995.
7. David C. Douglas, Charles E. Leiserson, Bradley C. Kuszmaul, Shaw-Wen Yang, Daniel W. Hillis, David Wells, Carl R. Feynman, Bruce J. Walker, and Brewster Kahle, "Router for parallel computer including arrangement for redirecting messages," *United States Patent* 5,530,809, filed January 14, 1994, issued June 25, 1996.
8. W. Daniel Hillis, David C. Douglas, Charles E. Leiserson, Bradley C. Kuszmaul, Mahesh N. Ganmukhi, Jeffrey V. Hill, and Monica C. Wong-Chan, "Parallel computer system with physically separate tree networks for data and control messages," *United States Patent* 5,590,283, filed January 27, 1995, issued December 31, 1996.
9. Bradley C. Kuszmaul, Charles E. Leiserson, Shaw-Wen Yang, Carl R. Feynman, W. Daniel Hillis, and David C. Douglas, "Digital computer for determining a combined tag value from tag values selectively incremented and decremented reflecting the number of messages transmitted and not received," *United States Patent* 5,680,550, filed February 13, 1995, issued October 21, 1997.
10. Timothy N. Weller and Charles E. Leiserson, "Content delivery network service provider (CDNSP)-managed content delivery network (CDN) for network service provider (NSP)," *United States Patent Application* 10/114,080, filed April 2, 2002.

## Teaching Experience of Charles E. Leiserson:

Term	Subject	Title	Role
ST 81	6.001	<i>Structure and Interpretation of Computer Programs</i>	Recitation (2 sections)
FT 81	6.032	<i>Computation Structures</i>	Recitation (2 sections)
ST 82	6.002	<i>Circuits and Electronics</i>	Recitation (2 sections)
FT 82	6.033	<i>Computer System Engineering</i>	Recitation (2 sections)
ST 83	6.045	<i>Computability, Automata, and Formal Languages</i>	Lectures, in charge
FT 83	6.045	<i>Computability, Automata, and Formal Languages</i>	Lectures, in charge
ST 84	6.895	<i>VLSI Algorithms</i>	Lectures, in charge
FT 84	6.001	<i>Structure and Interpretation of Computer Programs</i>	Recitation (2 sections)
FT 85	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 86	6.891	<i>Theory of Computing Machinery</i>	Lectures, in charge
FT 86	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
FT 86	6.848	<i>Introduction to VLSI and Parallel Computation</i>	Lectures
ST 87	6.849	<i>Advanced VLSI and Parallel Computation</i>	Lectures, in charge
SS 87	6.84s	<i>Parallel Algorithms and Architectures</i>	Lectures, in charge
FT 87	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
FT 87	6.848	<i>Introduction to VLSI and Parallel Computation</i>	Lectures
SS 88	6.84s	<i>Parallel Algorithms and Architectures</i>	Lectures, in charge
ST 89	6.004	<i>Computation Structures</i>	Recitation (2 sections)
SS 89	6.84s	<i>Parallel Algorithms and Architectures</i>	Lectures, in charge
FT 89	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
SS 90	6.84s	<i>Parallel Algorithms and Architectures</i>	Lectures, in charge
FT 90	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 91	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
SS 91	6.84s	<i>Parallel Algorithms and Architectures</i>	Lectures, in charge
FT 91		Richard B. Adler Scholar (6.035 and 6.918)	
ST 92	6.851	<i>Theory of Algorithms</i>	Lectures, in charge
FT 92	6.004	<i>Computation Structures</i>	Recitation (1 section)
ST 93	6.851	<i>Theory of Algorithms</i>	Lectures, in charge
SS 93	6.84s	<i>Parallel Algorithms and Architectures</i>	Lectures, in charge
FT 93	6.042	<i>Mathematics for Computer Science</i>	Development, in charge
ST 94	6.042	<i>Mathematics for Computer Science</i>	Lectures, in charge
FT 94	6.042	<i>Mathematics for Computer Science</i>	Lectures, in charge
ST 95	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 96	CS413	<i>Introduction to Parallel Systems</i> (National University of Singapore)	Lectures, in charge
FT 96	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge

ST 97	6.892	<i>Theory of Parallel Systems</i>	Lectures, in charge
FT 98	6.972	<i>The Structure of Engineering Revolutions</i>	Development, in charge.
ST 98	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 99	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
FT 99	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
FT 01	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 02	6.033	<i>Computer System Engineering</i>	Recitation (2 sections)
FT 02	6.042	<i>Mathematics for Computer Science</i>	Lectures, development
ST 03	6.042	<i>Mathematics for Computer Science</i>	Lectures, in charge
FT 03	6.895	<i>Theory of Parallel Systems</i>	Lectures, in charge
ST 04	6.895	<i>Theory of Parallel Hardware</i>	Lectures, in charge
FT 04	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 05	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
FT 05	6.046	<i>Introduction to Algorithms</i>	Lectures, in charge
ST 06		<i>Leadership Skills for Engineering Faculty</i>	Lectures, in charge
SS 07	PI.61s	<i>Leadership Skills for Engineering and Science Faculty</i>	Lectures, in charge

## Publications of Charles E. Leiserson:

### 16. Books:

1. Charles E. Leiserson, *Area-Efficient VLSI Computation*, ACM Doctoral Dissertation Award Series, The MIT Press, Cambridge, Massachusetts, 1983. (Won the ACM award for best Ph.D. thesis in computer science for the 1981–1982 academic year, as well as the John and Fannie Hertz Foundation award for best Ph.D. thesis in 1981.)
2. Charles E. Leiserson, editor, *Advanced Research in VLSI*, The MIT Press, Cambridge, Massachusetts, 1986.
3. Thomas H. Cormen, Charles E. Leiserson, and Ronald L. Rivest, *Introduction to Algorithms*, The MIT Press and McGraw-Hill, 1990. Chosen by the Association of American Publishers as the Best 1990 Professional and Scholarly Book in Computer Science and Data Processing. Translated into eight languages.
4. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein, *Introduction to Algorithms*, second edition, The MIT Press and McGraw-Hill, 2001.

### 17. Papers in Refereed Journals:

1. Charles E. Leiserson and James B. Saxe, “Optimizing synchronous systems,” *Journal of VLSI and Computer Systems*, Vol. 1, No. 1, Spring 1983, pp. 41–67. An early version appears in the *Twenty-Second Annual Symposium on Foundations of Computer Science*, IEEE Computer Society, November 1981, pp. 23–36.
2. Charles E. Leiserson and Ron Y. Pinter, “Optimal placement for river routing,” *SIAM Journal on Computing*, Vol. 12, No. 3, August 1983, pp. 447–462. An early version appears in *CMU Conference on VLSI Systems and Computations*, Pittsburgh, Pennsylvania, October 1981, pp. 126–142.

3. Sandeep N. Bhatt and Charles E. Leiserson, "How to assemble tree machines," *Advances in Computing Research*, Vol. 2, 1984, pp. 95–114. An early version appears in the *Fourteenth Annual ACM Symposium on Theory of Computing*, San Francisco, California, ACM Special Interest Group for Automata and Computability Theory, May 1982, pp. 77–84.
4. Benny Chor, Charles E. Leiserson, Ronald L. Rivest, and James Shearer, "An application of number theory to the organization of raster-graphics memory," *JACM*, Vol. 33, No. 1, January 1986, pp. 86–104. An early version by the first three authors appears in the *Twenty-Third Annual Symposium on Foundations of Computer Science*, Chicago, Illinois, IEEE Computer Society, November 1982, pp. 92–99.
5. Tom Leighton and Charles E. Leiserson, "Wafer-scale integration of systolic arrays," *IEEE Transactions on Computers*, Vol. C-34, No. 5, May 1985, pp. 448–461. An early version appears in the *Twenty-Third Annual Symposium on Foundations of Computer Science*, Chicago, Illinois, IEEE Computer Society, November 1982, pp. 297–311.
6. Charles E. Leiserson, "Fat-trees: universal networks for hardware-efficient supercomputing," *IEEE Transactions on Computers*, Vol. C-34, No. 10, October 1985, pp. 892–901. An early version appears in the *1985 International Conference on Parallel Processing*, St. Charles, Illinois, IEEE Computer Society Press, August 1985, pp. 393–402. (Received Best Presentation Award at the conference.)
7. Ronald I. Greenberg and Charles E. Leiserson, "Randomized routing on fat-trees," *Advances in Computing Research*, Vol. 5, JAI Press, Inc., 1989, pp. 345–374. An early version appears in *Twenty-Sixth Annual Symposium on Foundations of Computer Science*, Portland, Oregon, IEEE Computer Society, October 1985, pp. 241–249.
8. Charles E. Leiserson and James B. Saxe, "A mixed-integer linear programming problem which is efficiently solvable," *Journal of Algorithms*, Vol. 9, 1988, pp. 114–128. An early version appears in *Twenty-First Annual Allerton Conference on Communication, Control, and Computing*, Department of Electrical Engineering and the Coordinated Science Laboratory of the University of Illinois at Urbana-Champaign, Allerton House, Monticello, Illinois, October 1983, pp. 204–213.
9. Charles E. Leiserson and Bruce M. Maggs, "Communication-efficient parallel algorithms for distributed random-access machines," *Algorithmica*, Vol. 3, 1988, pp. 53–77. An early version appears as "Communication-efficient parallel graph algorithms," in *1986 International Conference on Parallel Processing*, St. Charles, Illinois, August 1986, pp. 861–868. (Received Most Original Paper Award at the conference.)
10. Ronald I. Greenberg and Charles E. Leiserson, "A compact layout for the three-dimensional tree of meshes," *Applied Mathematics Letters*, Vol. 1, No. 2, 1988, pp. 171–176.
11. Joe Kilian, Shlomo Kipnis, and Charles E. Leiserson, "The organization of permutation architectures with bussed interconnections," *IEEE Transactions on Computers*, Vol. 39, No. 11, November 1990, pp. 1346–1358. An early version appears in *Twenty-Eighth Annual Symposium on Foundations of Computer Science*, Syracuse, New York, IEEE Computer Society, October 1987, pp. 305–315.

12. Thomas H. Cormen and Charles E. Leiserson, "A hyperconcentrator switch for routing bit-serial messages," *Journal of Parallel and Distributed Computing*, Vol. 10, 1990, pp. 193–204. An early version appears in *1986 International Conference on Parallel Processing*, St. Charles, Illinois, August 1986, pp. 721–728. (Received Best Presentation Award at the conference.)
13. Charles E. Leiserson and James B. Saxe, "Retiming synchronous circuitry," *Algorithmica*, Vol. 6, 1991, pp. 5–35.
14. Charles E. Leiserson, Zahi S. Abuhamdeh, David C. Douglas, Carl R. Feynman, Mahesh N. Ganmukhi, Jeffrey V. Hill, W. Daniel Hillis, Bradley C. Kuszmaul, Margaret A. St. Pierre, David S. Wells, Monica C. Wong, Shaw-Wen Yang, and Robert Zak, "The network architecture of the Connection Machine CM-5," *Journal of Parallel and Distributed Computing*, Vol. 33, No. 2, March 15, 1996, pp. 145–158. An early version appears in the *4th Annual ACM Symposium on Parallel Algorithms and Architectures*, San Diego, California, July 1992, pp. 272–285.
15. Robert D. Blumofe and Charles E. Leiserson, "Space-efficient scheduling of multithreaded computations," *SIAM Journal on Computing*, Vol. 7, No. 1, February 1998, pp. 202–229. An early version appears in *Proceedings of the 25th Symposium on Theory of Computing*, ACM, San Diego, California, May, 1993, pp. 362–371.
16. Robert D. Blumofe and Charles E. Leiserson, "Scheduling multithreaded computations by work stealing," *Journal of the ACM*, Vol. 46, No. 5, September 1999, pp. 720–748. An early version appears in the *Thirty-Fifth Annual Symposium on Foundations of Computer Science*, IEEE Computer Society, November 1994, pp. 356–368.
17. Robert D. Blumofe, Christopher F. Joerg, Bradley C. Kuszmaul, Charles E. Leiserson, Keith H. Randall, and Yuli Zhou, "Cilk: An efficient multithreaded runtime system," *Journal of Parallel and Distributed Computing*, Vol. 37, No. 1, August 1996, pp. 55–69. An early version appears in the *Fifth ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, July 1995, pp. 207–216.
18. Alexander T. Ishii, Charles E. Leiserson, and Marios Papaefthymiou, "Optimizing two-phase, level-clocked circuitry," *Journal of the ACM*, Vol. 44, No. 1, January 1997, pp. 148–199. An early version appears in the *Brown/MIT Conference on Advanced Research in VLSI and Parallel Systems*, Providence, Rhode Island, March 1992, pp. 245–264.
19. Charles E. Leiserson and Keith H. Randall, "Parallel algorithms for the circuit value update problem," *Theory of Computing Systems*, Vol. 30, 1997, pp. 583–597. An early version appears in the *Seventh Annual ACM Symposium on Parallel Algorithms and Architectures*, July 1995, pp. 13–20.
20. Guy E. Blelloch, Charles E. Leiserson, Bruce M. Maggs, C. Gregory Plaxton, Stephen J. Smith, and Marco Zagha, "An experimental analysis of parallel sorting algorithms," *Theory of Computing Systems*, Vol. 31, No. 2, 1998, pp. 135–167. An early version appears under the title, "A comparison of sorting algorithms for the Connection Machine CM-2," in the *3rd Annual ACM Symposium on Parallel Algorithms and Architectures*, Hilton Head, South Carolina, July 1991, pp. 3–16.

21. Don Dailey and Charles E. Leiserson, “Using Cilk to write multiprocessor chess programs,” *Advances in Computer Games*, H.J. van den Herik and B. Monien, eds., volume 9, University of Maastricht, 2001, pp. 25–52.
22. C. Scott Ananian, Krste Asanovic, Bradley C. Kuszmaul, Charles E. Leiserson, Sean Lie, “Unbounded transactional memory,” *IEEE Micro*, Vol. 26, No. 1, January 2006. (Won the *IEEE Micro* “Top Picks” award for the most industry relevant and significant papers of the year in computer architecture.) An early version appeared in *11th International Symposium on High-Performance Computer Architecture*, San Francisco, CA, February, 2005, pp. 316–327.
23. John S. Danaher, I-Ting Angelina Lee, and Charles E. Leiserson, “Programming with exceptions in JCilk,” *Science of Computer Programming*, Vol. 63, No. 2, December 2006, pp. 147–171.
24. Yuxiong He, Wen Jing Hsu, and Charles E. Leiserson, “Provably Efficient Nonclairvoyant Adaptive Scheduling,” *IEEE Transactions on Parallel and Distributed Systems*, 2008, to appear.

### Papers in Proceedings of Refereed Conferences:

(Other than early versions of those above.)

1. H. T. Kung and Charles E. Leiserson, “Systolic arrays (for VLSI),” *Sparse Matrix Proceedings 1978*, I. S. Duff and G. W. Stewart, ed., Knoxville, Tennessee, Society for Industrial and Applied Mathematics, 1979, pp. 256–282.
2. Charles E. Leiserson, “Systolic priority queues,” *Proceedings of the Caltech Conference on Very Large Scale Integration*, Charles L. Seitz, ed., Pasadena, California, January 1979, pp. 199–214.
3. Dan Hoey and Charles E. Leiserson, “A layout for the shuffle-exchange network,” *1980 International Conference on Parallel Processing*, August 1980, pp. 329–336.
4. Charles E. Leiserson, “Area-efficient graph layouts (for VLSI),” *Twenty-First Annual Symposium on Foundations of Computer Science*, Syracuse, New York, IEEE Computer Society, October 1980, pp. 270–281.
5. Charles E. Leiserson, Flavio M. Rose, and James B. Saxe, “Optimizing synchronous circuitry by retiming,” *Third Caltech Conference on VLSI*, Randal Bryant, ed., Pasadena, California, March 1983, pp. 87–116.
6. Charles E. Leiserson, “Systolic and semisystolic design,” *IEEE International Conference on Computer Design/VLSI in Computers (ICCD ’83)*, Rye, New York, October 1983, pp. 627–632.
7. Kyle A. Gallivan and Charles E. Leiserson, “High-performance architectures for adaptive filtering,” *SPIE Conference on Real Time Signal Processing*, Vol. 495, No. 7, San Diego, California, August 1984, pp. 30–38.

8. Charles E. Leiserson and F. Miller Maley, “Algorithms for routing and testing routability of planar VLSI layouts,” *Proceedings of the 17th Symposium on Theory of Computing*, ACM, Providence, Rhode Island, May 1985, pp. 69–78.
9. Alexander T. Ishii and Charles E. Leiserson, “A timing analysis of level-clocked circuitry,” *Proceedings of the Sixth MIT Conference on Advanced Research in VLSI*, April 1990, pp. 113–130.
10. Charles E. Leiserson, Satish Rao, and Sivan Toledo, “Efficient out-of-core algorithms for linear relaxation using blocking covers,” *Thirty-Fourth Annual Symposium on Foundations of Computer Science*, IEEE Computer Society, November 1993, pp. 704–713.
11. Robert D. Blumofe, Matteo Frigo, Christopher F. Joerg, Charles E. Leiserson, and Keith H. Randall, “Dag-consistent distributed shared memory,” *Tenth International Parallel Processing Symposium*, IEEE Computer Society, April 1996, pp. 132–141.
12. Robert D. Blumofe, Matteo Frigo, Christopher F. Joerg, Charles E. Leiserson, and Keith H. Randall, “An analysis of dag-consistent distributed shared-memory algorithms,” *Eighth Annual ACM Symposium on Parallel Algorithms and Architectures*, June 1996, pp. 297–308.
13. Charles E. Leiserson, “Programming irregular parallel applications in Cilk,” *Solving Irregularly Structured Problems in Parallel: 4th International Symposium, IRREGULAR’97*, Paderborn, Germany, June 1997, Springer-Verlag, pp. 61–71.
14. Mingdong Feng and Charles E. Leiserson, “Efficient detection of determinacy races in Cilk programs,” *Ninth Annual ACM Symposium on Parallel Algorithms and Architectures*, June 1997, pp. 1–11.
15. Matteo Frigo, Charles E. Leiserson, and Keith Randall, “The implementation of the Cilk-5 multithreaded language,” *1998 ACM SIGPLAN Conference on Programming Language Design and Implementation*, Montreal, Canada, June 1998, pp. 212–223.
16. Guang-Ien Cheng, Mingdong Feng, Charles E. Leiserson, Keith H. Randall, and Andrew F. Stark, “Detecting data races in Cilk programs that use locks,” *Tenth ACM Symposium on Parallel Algorithms and Architectures*, June 1998, pp. 298–309.
17. Matteo Frigo, Charles E. Leiserson, Harald Prokop, and Sridhar Ramachandran, “Cache-oblivious algorithms,” *40th Annual Symposium on Foundations of Computer Science*, New York, New York, October 17–19, 1999, pp. 285–297.
18. Ching Law and Charles E. Leiserson, “A new competitive analysis of randomized caching,” *Eleventh Annual International Symposium on Algorithms And Computation*, December 2000, pp. 35–46.
19. Michael A. Bender, Jeremy T. Fineman, Seth Gilbert, and Charles E. Leiserson, “On-the-fly maintenance of series-parallel relationships in fork-join multithreaded programs,” *16th Annual ACM Symposium on Parallelism in Algorithms and Architectures*, June 2004, pp. 133–144.

20. Michael A. Bender, Martin Farach-Colton, Simai He, Bradley C. Kuszmaul, and Charles E. Leiserson, “Adversarial analyses of window backoff strategies for simple multiple-access channels,” *ACM Symposium on Parallelism in Algorithms and Architectures*, July 2005, pp. 325–332.
21. John S. Danaher, I-Ting Angelina Lee, and Charles E. Leiserson, “The JCilk language for multithreaded computing,” *Synchronization and Concurrency in Object-Oriented Languages, OOPSLA 2005 Workshop*, October 2005.
22. Kunal Agrawal, Yuxiong He, Wen Jing Hsu, and Charles E. Leiserson, “Adaptive scheduling with parallelism feedback,” *ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming*, March 2006, pp. 100–109.
23. Yuxiong He, Wen-Jing Hsu, and Charles E. Leiserson, “Provably Efficient Two-Level Adaptive Scheduling,” *12th Workshop on Job Scheduling Strategies for Parallel Processing*, Saint Malo, France, June 2006, pp. 1–32.
24. Kunal Agrawal, Yuxiong He, and Charles E. Leiserson, “An Empirical Evaluation of Work Stealing with Parallelism Feedback,” *Proceedings of the International Conference on Distributed Computing Systems (ICDCS)*, July, 2006.
25. Kunal Agrawal, Yuxiong He, and Charles E. Leiserson, “Work stealing with parallelism feedback,” *26th International Conference on Distributed Computing Systems*, Lisboa, Portugal, July 2006.
26. Kunal Agrawal, Charles E. Leiserson, and Jim Sukha, “Memory models for open-nested transactions,” *Proceedings of the ACM SIGPLAN Workshop on Memory Systems Performance and Correctness*, October 22, 2006.

### Other Major Publications:

1. H. T. Kung and Charles E. Leiserson, “Algorithms for VLSI processor arrays,” Chapter 8.3 of *Introduction to VLSI Systems* by Carver A. Mead and Lynn A. Conway, Addison-Wesley, 1978.
2. Charles E. Leiserson, Jill P. Mesirov, Lena Nekludova, Stephen M. Omohundro, and John Reif, “Solving sparse linear systems via parallel nested dissection on the Connection Machine,” *SIAM 1986 National Meeting*, Boston, Mass., July 1986. Also appears as a Thinking Machines Corporation technical memorandum (unnumbered).
3. Tom Leighton and Charles E. Leiserson, “A survey of algorithms for integrating wafer-scale systolic arrays,” in *Wafer-Scale Integration*, G. Saucier and J. Trilhe, eds., North-Holland, 1986, pp. 177–195.
4. Charles E. Leiserson and John G. Lewis, “Orderings for parallel sparse symmetric factorization,” Chapter 5 of *Parallel Processing for Scientific Computing*, Garry Rodrigue, ed., SIAM, 1989.

5. Charles E. Leiserson, "VLSI theory and parallel supercomputing," Chapter 2 of *Carnegie Mellon University School of Computer Science 25th Anniversary Symposium*, Richard F. Rashid, ed., Addison-Wesley, 1991, pp. 29–44. An early version appeared in *Decennial Caltech Conference on VLSI*, March 1989, The MIT Press, pp. 5–16.
6. Charles E. Leiserson, "Timekeeper," *SIGACT News*, Vol. 23, No. 4, ACM Press, Fall 1992, pp. 81–82.
7. Charles E. Leiserson and Aske Plaatt, "Programming parallel applications in Cilk," *SIAM News*, Vol. 31, No. 4, May 1998, pp. 6–7.
8. Erik D. Demaine, Martin L. Demaine, Alan Edelman, Charles E. Leiserson, and Per-Olof Persson, "Building blocks and excluded sums," *SIAM News*, Volume 38, Number 1, January/February 2005.

### **Internal Memoranda and Progress Reports:**

*(Other than early versions of those above.)*

1. Sandeep N. Bhatt and Charles E. Leiserson, "Minimizing the longest edge in a VLSI layout," MIT VLSI Memo No. 82-86, May 1981.
2. Charles E. Leiserson and Cynthia A. Phillips, "A space-efficient algorithm for finding the connected components of rectangles in the plane," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-323, February 1987.
3. Charles E. Leiserson and Cynthia A. Phillips, "Parallel contraction of planar graphs," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-343, October 1987.
4. Tom Leighton, Charles E. Leiserson, Bruce Maggs, Serge Plotkin, and Joel Wein, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 1, March 1988.
5. Tom Leighton, Charles E. Leiserson, Bruce Maggs, Serge Plotkin, and Joel Wein, "Advanced Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 2, March 1988.
6. C. E. Leiserson, F. T. Leighton, and S. A. Plotkin, editors, "Connection Machine Projects," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 4, January 1989.
7. Tom Leighton, Charles E. Leiserson, and Eric Schwabe, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 6, March 1989.
8. Tom Leighton and Charles E. Leiserson, "Advanced Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 7, December 1989.

9. Tom Leighton, Charles E. Leiserson, and Dina Kravets, "Theory of Parallel and VLSI Computation," MIT Laboratory for Computer Science Research Seminar Series Memorandum MIT/LCS/RSS 8, May 1990.
10. Charles E. Leiserson, editor, "Proceedings of the 1991 MIT Student Workshop on VLSI and Parallel Systems," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-513, August 1991.
11. Alexander T. Ishii, Charles E. Leiserson, and Marios C. Papaefthymiou, "An algorithm for the tramp steamer problem based on mean-weight cycles," MIT Laboratory for Computer Science Technical Memorandum MIT/LCS/TM-457, November 1991.
12. Charles E. Leiserson, editor, "Proceedings of the 1992 MIT Student Workshop on VLSI and Parallel Systems," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-546, August 1992.
13. Charles E. Leiserson, editor, "Proceedings of the 1993 MIT Student Workshop on Supercomputing Technologies," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-575, August 1993.
14. Phillip B. Gibbons, Richard M. Karp, Charles E. Leiserson, Gregory M. Papadopolous, editors, "DIMACS Workshop on Models, Architectures, and Technologies for Parallel Computation," DIMACS Center for Discrete Mathematics and Theoretical Computer Science, Technical Report 93-87, September, 1993.
15. Charles E. Leiserson, editor, "Proceedings of the 1994 MIT Student Workshop on Supercomputing Technologies," MIT Laboratory for Computer Science Technical Report MIT/LCS/TR-622, July 1994.
16. Supercomputing Technologies Group, MIT Laboratory for Computer Science, *Cilk-5.2 (Beta 1) Reference Manual*, unpublished manuscript, available on the World Wide Web at <http://supertech.lcs.mit.edu/cilk>, 1998. Earlier versions of this manual are also available.
17. Charles E. Leiserson, Harald Prokop, and Keith H. Randall, "Using de Bruijn sequences to index a 1 in a computer word," unpublished manuscript, available on the World Wide Web at <http://supertech.lcs.mit.edu/cilk>, 1998.
18. Charles E. Leiserson and Harald Prokop, "A minicourse on multithreaded programming," unpublished manuscript, available on the World Wide Web at <http://supertech.lcs.mit.edu/cilk>, 1999.

## Invited Lectures:

### *Systolic Systems*

May 1981 MIT, Cambridge, Massachusetts

### *Optimizing Synchronous Systems*

- Jul. 1981 Digital Equipment Corporation, Maynard, Massachusetts
- Sep. 1981 Harvard University, Cambridge, Massachusetts
- Dec. 1981 MIT Lincoln Laboratory, Lexington, Massachusetts

*Optimal Placement for River Routing*

- Dec. 1981 MIT, Cambridge, Massachusetts

*Digital Circuit Optimization*

- May 1982 MIT, Cambridge, Massachusetts

*Optimization of Digital Circuitry by Retiming*

- Oct. 1982 Duke University, Durham, North Carolina
- Nov. 1982 University of Rochester, Rochester, New York
- Jan. 1983 Bell Laboratories, Murray Hill, New Jersey
- Apr. 1984 Brown University, Providence, Rhode Island

*Wafer-Scale Integration of Systolic Arrays*

- Nov. 1982 Carnegie-Mellon University, Pittsburgh, Pennsylvania
- Mar. 1983 University of California at Berkeley, Berkeley, California
- Jul. 1983 MIT, Cambridge, Massachusetts

*Systolic and Semisystolic Systems*

- Jul. 1983 MIT, Cambridge, Massachusetts
- Jul. 1983 Harris Corporation, Melbourne, Florida

*Systolic and Semisystolic Design*

- Aug. 1983 AT&T Bell Laboratories, Murray Hill, New Jersey
- Aug. 1983 Princeton University, Princeton, New Jersey

*Fat-Trees: Universal Networks for Hardware-Efficient Supercomputing*

- Jun. 1984 MIT, Cambridge, Massachusetts
- Jun. 1984 AT&T Bell Laboratories, Murray Hill, New Jersey
- Oct. 1984 IBM Research, Yorktown Heights, New York
- Jan. 1985 Bolt, Baranek, and Newman, Inc., Cambridge, Massachusetts
- Jan. 1985 Stanford University, Stanford, California
- Jan. 1985 University of California at Berkeley, Berkeley, California
- Jan. 1985 Lawrence Livermore National Laboratory, Livermore, California
- Feb. 1985 University of Minnesota, Minneapolis, Minnesota
- Feb. 1985 University of Toronto, Toronto, Canada
- Mar. 1985 Cornell University, Ithaca, New York
- Apr. 1985 New York University, New York, New York
- Apr. 1985 Thinking Machines Corporation, Cambridge, Massachusetts

*The Relevance of VLSI Theory to Parallel Supercomputing*

- Jan. 1986 Microelectronics and Computer Technology Corporation

- Workshop on Interconnection Networks, Austin, Texas  
May 1986 Mathematical Sciences Research Institute, Berkeley, California  
Jun. 1986 SIAM Annual Conference, Boston, Massachusetts  
Nov. 1987 Siemens-MIT Conference, Munich, West Germany

*Communication-Efficient Parallel Graph Algorithms*

- Oct. 1986 Graph Theory Day (New York Academy of Sciences),  
Albany, New York

*New Machine Models for Synchronous Parallel Algorithms*

- Dec. 1987 Institute for Mathematics and Its Applications,  
University of Minnesota, Minneapolis, Minnesota

*Very Large Scale Computing*

- Oct. 1988 Project MAC 25th Anniversary Symposium,  
MIT, Cambridge, Massachusetts

*VLSI Theory and Parallel Supercomputing*

- Mar. 1989 Decennial Caltech Conference on VLSI,  
California Institute of Technology, Pasadena, California  
Apr. 1989 Thinking Machines Corporation, Cambridge, Massachusetts  
Sep. 1990 CMU School of Computer Science 25th Anniversary Symposium,  
Carnegie Mellon University, Pittsburgh, Pennsylvania  
Oct. 1990 Texas Instruments Corporation, Dallas, Texas  
Dec. 1990 NEC Research Institute, Princeton, New Jersey  
Apr. 1992 AT&T Bell Laboratories, Holmdel, New Jersey

*Highly Reliable Large-Scale Computing*

- Nov. 1990 MIT VLSI Research Review, Cambridge, Massachusetts

*A Comparison of Sorting Algorithms for the Connection Machine CM-2*

- Mar. 1991 Purdue University, West Lafayette, Indiana  
Mar. 1991 Indiana University, Bloomington, Indiana  
Oct. 1991 University of Texas, Austin, Texas  
Nov. 1991 Yale University, New Haven, Connecticut

*Engineering Parallel Algorithms*

- May 1991 Second Annual Workshop on Parallel Algorithms,  
New Orleans, Louisiana

*The Network Architecture of the Connection Machine CM-5*

- Nov. 1991 Yale University, New Haven, Connecticut  
Nov. 1991 Sandia National Laboratory, Albuquerque, New Mexico  
Apr. 1992 Carnegie Mellon University, Pittsburgh, Pennsylvania  
Apr. 1992 MIT, Cambridge, Massachusetts

- May 1992 University of Washington, Seattle, Washington
- Jun. 1992 Dartmouth Institute for Advanced Graduate Studies,  
Hanover, New Hampshire
- Sep. 1992 International Conference on Parallel Processing  
Ecole Normale Supérieure de Lyon, Lyon, France
- Sep. 1992 Commissariat à l’Energie Atomique, Saclay, France
- Sep. 1992 Thinking Machines Corporation, Cambridge, Massachusetts
- Sep. 1992 DARPA Joint Microsystems/Computer Systems/HPC Software PI Meeting  
Daytona, Florida
- Oct. 1992 Symposium on New Directions in Parallel and Concurrent Computing  
New York, New York
- Oct. 1992 IEEE Foundations of Computer Science Conference (informal, invited  
presentation), Pittsburgh, Pennsylvania
- Nov. 1992 International Heinz Nixdorf Symposium on Parallel Architectures  
and Their Efficient Use, Paderborn, Germany
- Dec. 1992 IEEE Symposium on Parallel and Distributed Processing (keynote)  
Dallas, Texas
- Dec. 1992 Princeton University, Princeton, New Jersey
- Dec. 1992 University of Massachusetts, Amherst, Massachusetts
- Feb. 1993 Stanford University, Stanford, California
- Jul. 1993 International Workshop on Interconnection Networks, Marseille, France
- Sep. 1993 University of Zurich, Zurich, Switzerland
- Sep. 1993 Max Planck Institut für Informatik, Saarbrücken, Germany

*A Menagerie of Parallel Computing Networks*

- Jun. 1991 MIT Technology Day, Cambridge, Massachusetts

*Special-Purpose vs. General-Purpose Parallel Computing Networks*

- Aug. 1992 International Conference on Application-Specific Array Processors  
San Francisco, California (keynote)

*How to Interconnect One Million Processors (panel session)*

- Oct. 1992 Frontiers of Massively Parallel Computation, McLean, Virginia

*Space-Efficient Scheduling of Multithreaded Computations*

- Sep. 1993 DIMACS Workshop on Models, Architectures, and Technologies  
for Parallel Computation, Rutgers University, New Jersey
- Dec. 1993 Université de Paris-Sud, Paris, France
- Apr. 1994 Columbia University Theory Day, New York, New York
- Sep. 1994 Carleton University, Ottawa, Canada

*Efficient Scheduling of Multithreaded Computations*

- Mar. 1995 National University of Singapore, Singapore
- Apr. 1995 Distinguished Lecture, Carnegie Mellon University, Pittsburgh, Pennsylvania
- Apr. 1995 Harvard University, Cambridge, Massachusetts

Sep. 1995 Workshop on High-Performance Computing Activities in Singapore  
National Supercomputing Research Centre, Singapore

*What Is Theoretical Computer Science?*

Mar. 1996 Keynote Address, Science Research Seminar, National University of Singapore

*Can Multithreaded Programming Save Massively Parallel Computing?*

Apr. 1996 Keynote Address, International Parallel Processing Symposium, Honolulu, Hawaii

May 1996 GINTIC Institute of Manufacturing Technology, Singapore

*Algorithmic Multithreaded Computing*

Jun. 1996 Keynote Address, International Conference on Algorithms and Architectures  
for Parallel Processing, Singapore

Sep. 1996 Distinguished Lecture, Courant Institute, NYU, New York, New York

Nov. 1996 Theory of Computation Seminar, MIT, Cambridge, MA

Nov. 1996 Distinguished Lecture, University of Maryland, College Park, MD

*Efficient Detection of Determinacy Races in Cilk Programs*

Jan. 1997 National University of Singapore, Singapore

Jan. 1997 Dartmouth College, Hanover, New Hampshire

Jun. 1997 Max Planck Institut für Informatik, Saarbrücken, Germany

Nov. 1997 Distinguished Lecture, University of California, Santa Barbara

Jan. 1998 DEC Systems Research Center, Palo Alto, CA

*Teaching Parallel Algorithms using the Cilk Multithreaded Programming Language*

Jun. 1997 Forum on Parallel Computing Curricula, Newport, RI

Jun. 1998 Yale Workshop on Multithreaded Algorithms, New Haven, CT

Jul. 1998 National University of Singapore, Singapore

Jul. 1998 Academia Sinica, Taipei, Taiwan

*Algorithmic Multithreaded Programming Using Cilk*

Jul. 1997 National University of Singapore, Singapore

Jan. 1998 NASA Ames Research Center, Moffett Field, CA

Jan. 1998 Silicon Graphics, Inc., Mountain View, CA

Jan. 1998 Sun Microsystems, Inc., Palo Alto, CA

Aug. 1998 11th International Workshop on Languages and Compilers  
for Parallel Computing, Chapel Hill, NC

*Programming Shared-Memory Multiprocessors Using the Cilk Multithreaded Language*

Sep. 1998 MIT EECS Department Colloquium, Cambridge, MA

Sep. 1998 Intel Corporation, Beaverton, OR

Sep. 1998 University of California, Berkeley; Berkeley, CA

Oct. 1998 Stanford University, Stanford, CA

Oct. 1998 University of Delaware, Wilmington, DL

Nov. 1998 Rice University, Houston, TX

- Dec. 1998 5th Intl. Conference on High-Performance Computing, Chennai, India
- Jan. 1999 Workshop on Parallel Computing for Irregular Applications, Orlando Florida
- Mar. 1999 NTT Corporation, Atsugi, Japan
- Apr. 1999 Seminar on High-Level Parallel Programming, Dagstuhl, Germany
- May 1999 Understanding the New World of Information '99, Taipei, Taiwan
- Mar. 2003 George Washington University, Washington, D.C.
- Jul. 2004 Scandinavian Workshop on Algorithm Theory, Copenhagen, Denmark
- Oct. 2004 Reflections Projections, University of Illinois, Urbana-Champaign, Illinois

*Debugging Multithreaded Programs*

- Sep. 1998 Microsoft Research, Redmond, WA
- Nov. 1998 University of Texas at Austin, Austin, TX

*Design and Analysis of Algorithms for Shared-Memory Multiprocessors*

- May 1999 Workshop on Parallel Algorithms, Atlanta, GA
- Aug. 1999 Workshop on Algorithms and Data Structures, Vancouver, CA

*Using Cilk to Write Multiprocessor Chess Programs*

- Jun. 1999 International Conference on Computer Chess, Paderborn, Germany

*Cache-Oblivious Algorithms*

- Jun. 2004 Seminar on Cache-Oblivious and Cache-Aware Algorithms, Dagstuhl, Germany
- Jul. 2005 Computational Research in Boston, Cambridge, MA

*Unbounded Transactional Memory*

- Apr. 2005 Workshop on Transactional Systems, Chicago, IL
- Sep. 2005 Workshop on High-Performance Embedded Systems, Lexington, MA
- Oct. 2005 University of Rochester, Rochester, NY
- Jan. 2006 Intel Corporation, Cambridge, MA

*MIT.001 Final Exam*

- Sep. 2005 CSAIL Student Workshop, Gloucester, MA

*Multithreaded Programming in Cilk*

- Dec. 2005 Keynote, 4th Intel Programming Systems Conference, Santa Clara, CA
- Jun. 2006 Keynote, International Workshop on OpenMP, Reims, France

*Leadership and Engineering*

- Apr. 2006 50th Anniversary Celebration of Computer Science at Carnegie Mellon, Pittsburgh, PA

**Theses Supervised by Charles E. Leiserson:**

**Summary**

	<b>Total</b>	<b>Completed</b>	<b>In Progress</b>
S.B.	18	18	0
S.M.	19	19	0
M.Eng.	19	19	0
Engineers	1	1	0
Doctoral			
As Supervisor:	20	20	0
As Reader:	21	20	1

### **S.B. Theses and Advanced Undergraduate Projects:**

1. David H. Covert, *Graphic Objects That Draw Themselves*, May 1983.
2. Csaba Peter Gabor, *A Comparison of VLSI Designs for Complex Multiplication*, January 1984.
3. David J. Jilk, *Methodology for User-Aided Silicon Compilation*, January 1985.
4. Alexander T. Ishii, *A Comparison of Routing Algorithms for Fat-Tree Supercomputers*, May 1985.
5. Bruce M. Maggs, *Computing Minimum Spanning Trees on a Fat-Tree Architecture*, May 1985.
6. Marie J. Sullivan, *Parallel Graph Algorithms on the Connection Machine*, February 1987.
7. Vu Le Phan, *Massively Parallel Solutions to the Sparse Assignment Problem*, May 1991.
8. Michele L. Monclova, *An Experimental Comparison of Red-Black Trees and Skip Lists*, May 1991.
9. David B. Wilson, *Embedding Weak Hypercubes in Strong Hypercubes*, May 1991. (Winner of the William Martin Prize for best undergraduate computer science thesis at MIT.)
10. Keith Randall, *TIM: A CAD Tool for Designing Two-Phase Level-Clocked Circuitry*, May 1993.
11. Daniel Schmidt, *An Empirical Comparison of Four Heap Data Structures*, August 1994.
12. Tzu-Yi Chen, *Efficient Implementation of Out-of-Core Conjugate Gradient Algorithms*, May 1995. (Honorable Mention in the Computer Research Association's Outstanding Undergraduates Competition.)
13. Arup R. Guha, *Implementation of Band Cholesky Factorization in Cilk*, May 1997.
14. Runako Godfrey, , January 1998.
15. Adrian Soviani, *5 × 5 Magic Squares in Cilk*, May 1999.
16. Svetoslav Tzvetkov, *Parallel Memory Allocation*, May 1999.

17. David Venturini, *Chess Endgame Database Compression*, May 1999.
18. John Danaher, *A Real-Time Distributed Score-Keeping System*, May 2004.

**S.M. Theses:**

1. Martin I. Eiger, *Analysis of Algorithms to Compute Wirings Within Test Fixtures*, June 1985.
2. Cynthia A. Phillips, *Space-Efficient Algorithms for Computational Geometry*, August 1985.
3. F. Miller Maley, *Compaction with Automatic Jog Introduction*, May 1986.
4. Thomas H. Cormen, *Concentrator Switches for Routing Messages in Parallel Computers*, August 1986.
5. Bruce M. Maggs, *Communication-Efficient Parallel Graph Algorithms*, August 1986.
6. Alexander T. Ishii, *A Digital Model for Level-Clocked Circuitry*, January 1989.
7. James A. Park, *Notes on Searching in Multidimensional Monotone Arrays*, January 1989.
8. Jeffrey A. Fried, *VLSI Processor Design for Communication Networks*, January 1989.
9. Marios C. Papaefthymiou, *On Retiming Synchronous Circuitry and Mixed-Integer Optimization*, August 1990.
10. Michael Ernst, *Serializing Parallel Programs by Removing Redundant Computation*, August 1992.
11. Daniel Tunkelang, *An Aesthetic Layout Algorithm for Undirected Graphs*, August 1992.
12. Robert D. Blumofe, *Efficient Storage Management of Multithreaded Computations*, September 1992.
13. Keith Randall, *Virtual Networks: Implementation and Analysis*, May 1993.
14. Matteo Frigo, *The Weakest Reasonable Memory Model*, January 1998.
15. Bin Song, *Scheduling Adaptively Parallel Jobs*, January 1998.
16. Harald Prokop, *Cache-Oblivious Algorithms*, May 1999.
17. Sridhar Ramachandran, *An Algorithmic Theory of Caching*, February 2000.
18. Jeremy Fineman, *Provably Good Raced Detection That Runs in Parallel*, August 2005.
19. I-Ting Angelina Lee, *The JCilk Multithreaded Language*, August 2005.

### **M.Eng. Theses:**

1. Robert C. Miller, *A Type-checking Preprocessor for Cilk 2, a Multithreaded C Language*, May 1995.
2. Howard J. Lu, *Heterogeneous Multithreaded Computing*, May 1995.
3. Daricha Techopitayakul, *Dynamic Parallel Tables*, May 1995.
4. Philip Lisiecki, *Macroscheduling in the Cilk Network of Workstations Environment*, May 1996.
5. Andrew F. Stark, *Debugging Multithreaded Programs that Incorporate User-Level Locking*, May 1998. (Winner of the William Martin Prize for best computer science M.Eng. thesis at MIT.)
6. Guang-Ien Cheng, *Algorithms for Data-Race Detection in Multithreaded Programs*, May 1998.
7. Nathaniel A. Kushman, *Identifying and Fixing Processor Performance Monotonicity Problems: A Case Study of the SUN UltraSPARC*, May 1998.
8. Igor B. Lyubashevskiy, *Portable Fault-Tolerant File I/O*, May 1998.
9. Ching Law, *A New Competitive Analysis of Randomized Caching*, May 1999.
10. Jeremy Sawicki, *Using Cilk for Parallel Computation in MATLAB*, May 1999.
11. David B. Berman, *Efficient Parallel Binary Decision Diagram Construction Using Cilk*, May 2000.
12. Matthew S. DeBergalis, *A Parallel File I/O API for Cilk*, May 2000.
13. Kai Huang, *Data-Race Detection in Transactions-Everywhere Parallel Programming*, May 2003.
14. Siddhartha Sen, *Dynamic Processor Allocation for Adaptively Parallel Jobs*, August 2004.
15. Jim Sukha, *Memory-Mapped Transactions*, May 2005.
16. John S. Danaher, *The JCilk-1 Runtime System*, May 2005.
17. Tim Olsen, *LexTix: A Multimedia Lecture-Viewer*, May 2005.
18. Tushara Karunaratna, *Parallel Race Detection*, August 2005.
19. Jelani Nelson, *External-Memory Search Trees with Fast Insertions*, May 2006.

### **Engineers Theses:**

1. Flavio Rose, *Models for VLSI Circuits*, March 1982.

### Doctoral Theses, Supervisor:

1. Ron Y. Pinter, *Routability and Its Impact on Placement Algorithms for Integrated Circuits*, August 1982. (Cosupervised by Ronald L. Rivest.)
2. Sandeep N. Bhatt, *The Complexity of Graph Layout and Channel Routing for VLSI*, January 1984.
3. Andrew V. Goldberg, *Efficient Graph Algorithms for Sequential and Parallel Computers*, February 1987.
4. F. Miller Maley, *Single-Layer Wire Routing*, August 1987.
5. Serge A. Plotkin, *Graph-Theoretic Techniques for Parallel, Distributed, and Sequential Computation*, August 1988.
6. Guy E. Blelloch, *Scan Primitives and Parallel Vector Models*, September 1988.
7. Bruce M. Maggs, *Locality in Parallel Computation*, September 1989.
8. Ronald I. Greenberg, *Efficient Interconnection Schemes for VLSI and Parallel Computation*, September 1989.
9. Cynthia A. Phillips, *Theoretical and Experimental Analyses of Parallel Combinatorial Algorithms*, October 1989.
10. Shlomo Kipnis, *Organization of Systems with Bussed Interconnections*, August 1990.
11. James K. Park, *The Monge Array: An Abstraction and Its Applications*, May 1991.
12. Alexander T. Ishii, *Timing Verification of Level-Clocked Circuits*, October 1991.
13. Thomas H. Cormen, *Virtual Memory for Data Parallel Computing*, September 1992.
14. Marios C. Papaefthymiou, *Timing Optimization of VLSI and Parallel Systems*, August 1993.
15. Bradley C. Kuszmaul, *Synchronized MIMD Computation*, May 1994.
16. Sivan Toledo, *Quantitative Performance Modeling of Scientific Computations and Creating Locality in Numerical Algorithms*, May 1995.
17. Robert D. Blumofe, *Executing Multithreaded Programs Efficiently*, September 1995.
18. Christopher F. Joerg, *Cilk: A System for Parallel Multithreaded Computing*, January 1996.
19. Keith H. Randall, *Cilk: Efficient Multithreaded Computing*, May 1998.
20. Matteo Frigo, *Portable High-Performance Programs*, June 1999.

### Doctoral Theses, Reader:

1. Aloysius K. Mok, *Fundamental Design Problems of Distributed Systems for the Hard-Real-Time Environment*, May 1983.
2. G. A. Boughton, *Routing Networks for Packet Communication Systems*, August 1984.
3. James B. Saxe, *Generalized Transformations on Algorithms: Two Case Studies*, August 1985 (Department of Computer Science, Carnegie-Mellon University).
4. Peter W. Shor, *Random Planar Matching and Bin Packing*, (MIT Mathematics Department), August 1985.
5. Thang Nguyen Bui, *Graph Bisection Algorithms*, January 1986.
6. Daniel Weise, *Hierarchical, Multilevel Verification of MOS/VLSI Circuits*, August 1986.
7. Alan T. Sherman, *Cryptology and VLSI*, October 1986.
8. Mark R. Newman, *Randomness and Robustness in Hypercube Computation*, September 1989.
9. Bonnie Berger, *Using Randomness to Design Efficient Deterministic Algorithms*, May 1990.
10. Eric Schwabe, *Theoretical Issues in Parallel Computation: Hypercube-Related Architectures and Dynamic Structures*, May 1991.
11. Joel Wein, *Parallel Computation and Combinatorial Optimization: Scheduling Algorithms for Parallel Machines and Parallel Algorithms for the Assignment Problem*, August 1991.
12. Filip Van Aelten, *Automatic Procedures for the Behavioral Verification of Digital Designs*, May 1991.
13. Clifford Stein, *Approximation Algorithms for Multicommodity Flow and Shop Scheduling*, August 1992.
14. David Williamson, *On the Design of Approximation Algorithms for a Class of Graph Problems*, September 1993.
15. Yuan Ma, *Fault-Tolerant Sorting Networks*, June 1994.
16. Feng Ming Dong, *Compilation and Run-Time Environment of Parallel Lisp on Distributed Systems*, May 1995 (Department of Information Systems and Computer Science, National University of Singapore).
17. James Alexander Stuart Fiske, *Thread Scheduling Mechanisms for Multiple-Context Parallel Processors*, May 1995.
18. Parry Husbands, *Interactive Supercomputing*, January 1999.
19. Rajeev Barua, *Maps: A Compiler-Managed Memory System for Software-Exposed Architectures*, January 2000.

20. Russell Schwartz, *The Local Rules Dynamics Model for Self-Assembly Simulation*, February 2000.
21. Sam Larsen, *Exploiting Vector Parallelism in Software Pipelined Loops*, expected May 2006.