RawNet: Network Processing on the Raw Processor

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Introduction: In the past, the processing of high-speed network streams in routers has been the domain of application specific integrated circuits (ASIC). While this approach can result in very high speed systems that are able to process many gigabits of network packets, it has some distinct disadvantages. Most notably, because custom hardware has been produced, if protocols change, or if any change is needed, new chips need to be produced, which can be very expensive. Also the time required to fabricate new chips is long when compared to reprogramming a microprocessor.

To address these problems, we have started to see the advent of network processors specifically designed to address this need for programmability with ASIC level performance for network processing workloads. While network processors are a step in the right direction in bringing programmability to network routing, they are still very specially tuned to the application of network processing and more specifically route-table lookup. Network processors can be good if a router only needs to do routing, but if more services such as data packet encryption or network address translation are needed in the future these special purpose architectures may not be up to the task.

In the RawNet project we are investigating the use of the Raw[1] general purpose processor as both a network processor and a switch for multi-gigabit IP routing. While previous general purpose architectures have failed to give a useful programmatic interface to sufficient bandwidth to support multi-gigabit IP routing, the Raw processor, through its tiled architecture, and software exposed on-chip networking, has enough internal and external bandwidth to deal with high rate routing problems.

Approach: The RawNet project has two main emphases. First, we are exploring how to map network processing applications such as route-table lookup and packet classification to the Raw processor. This is being done so that we can better understand the problem and explore what forms of architectural enhancements can be added to general purpose processors to increase performance on network applications. Secondly we are researching how to map a complete IP router with both routing calculation and integrated switch fabric onto the Raw processor. Specifically we are focusing on how to use Raw's internal static networks to route semi-dynamic flows like IP packets in an efficient manner.

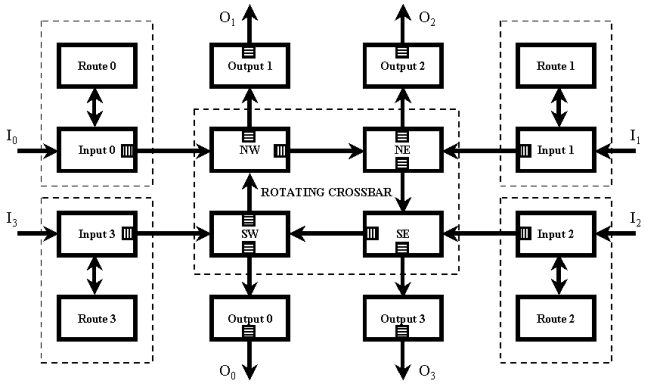

Figure 1: Mapping of a Four Port Router to a Raw Prototype Chip.

Progress: So far, the RawNet team has implemented[2] a very simplistic four port IP router with integrated switch fabric onto a simulated 16-tile Raw prototype chip. Figure 1 shows the mapping that was chosen for this router. One novel thing about this approach is that all of the data for the packets flow over the Raw static network. This was done by building a rotating crossbar that allowed for simplification of the static network routing decisions. Also we have begun looking at other network processors to see how route-table lookup maps to these architectures.

Future: In the future we will be implementing a more complete single chip Raw based IP router with more complicated routing decisions. Also we are very interested in pushing even more computation into a Raw style fabric

such as computation which is currently being done by MAC layer chips. The idea here is to push general purpose digital computation as far as possible into the domain of analog electronics and ASICs. So for instance all that would be needed to implement an IP router with this philosophy would be a Raw fabric, analog to digital converters and digital to analog converters. This approach gives the added bonus of being completely programmable and allows for economies of scale because only one form of chip will be needed, Raw fabric chips.

Research Support: This research is supported by DARPA under Contract # F29601-04-2-0166.

References:

[1] E. Waingold, M. Taylor, D. Srikrishna, V. Sarkar, W. Lee, V. Lee, J. Kim, M. Frank, P. Finch, R. Barua, J. Babb, S. Amarasinghe, and A. Agarwal, "Baring It All to Software: Raw Machines," *IEEE Computer*, vol. 30, no. 9, pp. 86–93, Sept. 1997, Also available as MIT-LCS-TR-709.

[2] G. Chuvpilo, D. Wentzlaff, and S. Amarasinghe, "Gigabit IP Routing on Raw," in *8th International Symposium on High-Performance Computer Architecture, Workshop on Network Processors*, Cambridge, MA, Feb. 2002.