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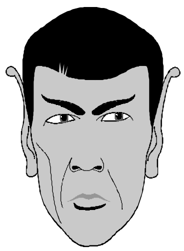
Logic Gates



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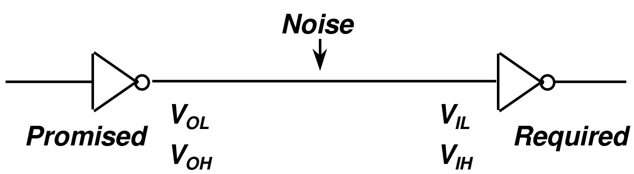
Recap: Static Discipline



V_{OL}	*Highest voltage which may be output as valid "0"*	V_{IL}	*Highest voltage which must be interpreted as valid "0"*
V_{OH}	*Lowest voltage which may be output as valid "1"*	V_{IH}	*Lowest voltage which must be interpreted as valid "1"*

Low Noise Margin: $V_{IL} - V_{OL}$

High Noise Margin: $V_{OH} - V_{IH}$

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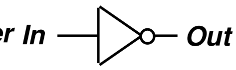
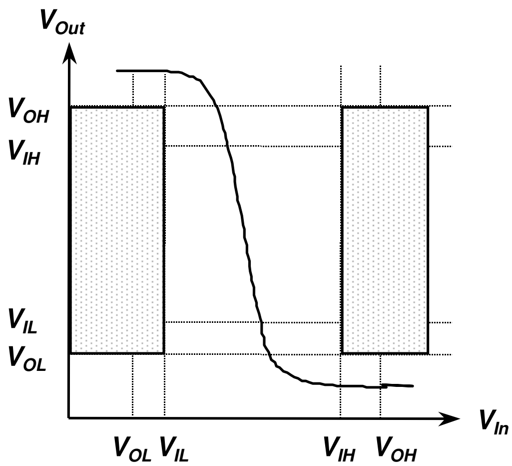
Voltage Transfer Curve

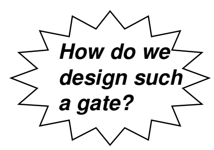
Static Voltage Transfer Curve for Inverter





Need both:

1. ***Gain***
2. ***Non-linearity***



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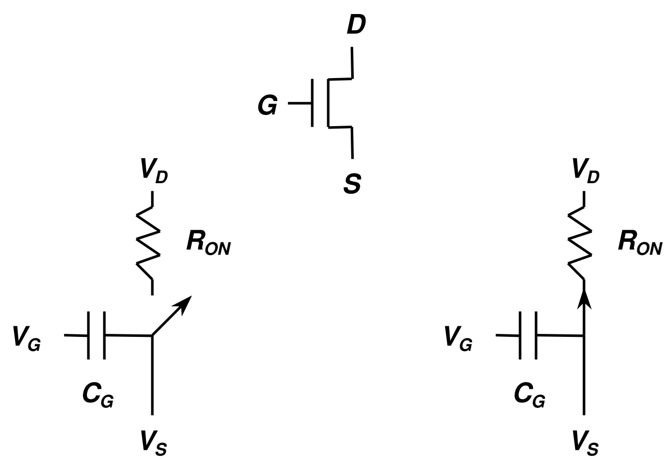
N-Channel Field Effect Transistor



Switch open if V_G is low *Switch closed if V_G is high*

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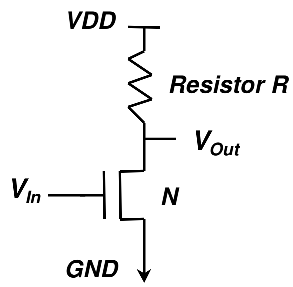
Proposed NMOS Gate



When V_{In} is low, resistor R pulls V_{Out} up to VDD.

What if V_{In} is high?

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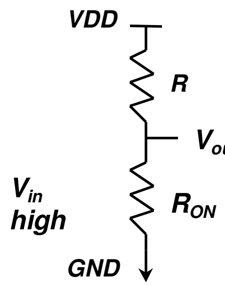
Problems with NMOS Gate



$$V_{out} = \frac{R_{ON}\ VDD}{R + R_{ON}}$$

When V_{In} is high, and if $R_{ON} << R$, V_{Out} close to zero but not quite zero!

Large R causes other complications, e.g., slow rising transition at V_{Out}.

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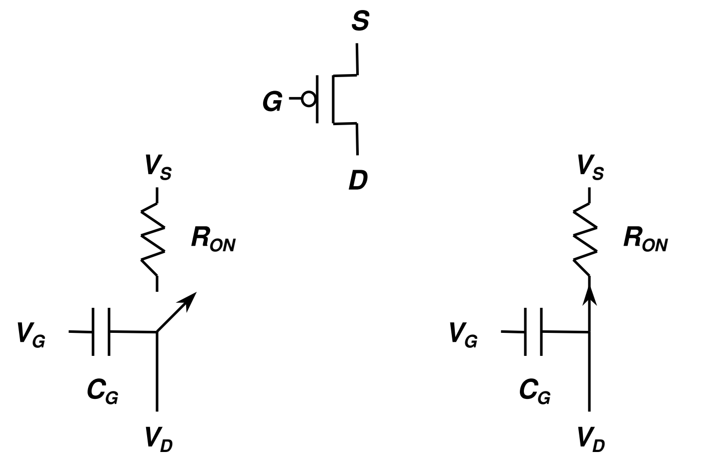
P-Channel Field Effect Transistor



Switch open if V_G is high *Switch closed if V_G is low*

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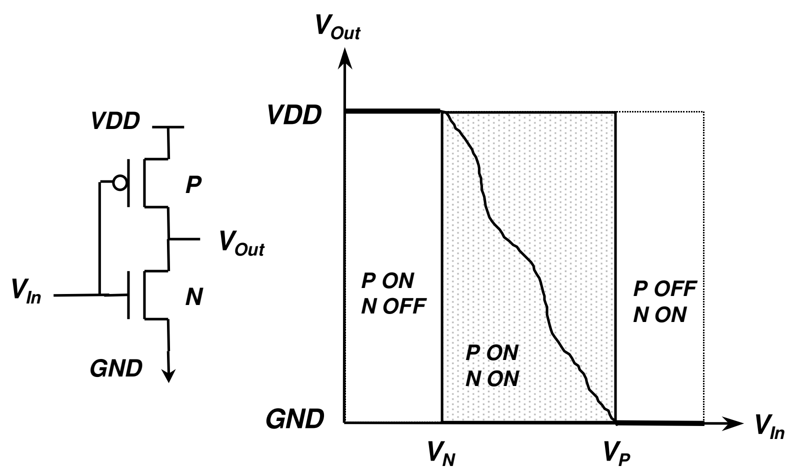
Proposed CMOS Gate



$V_{OL} = 0V$ $V_{OH} = VDD$ $V_{IL} = V_N$ $V_{IH} = V_P$

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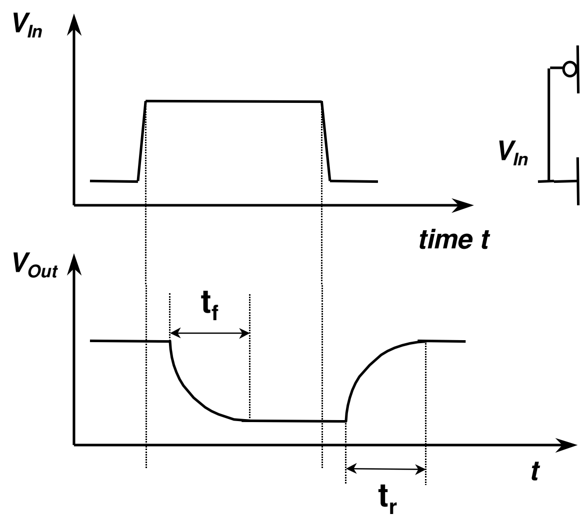
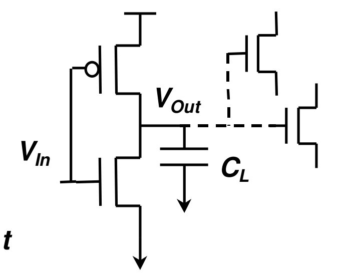
Signal Timing: Rise and Fall Time





Time constant of t_f , t_r equals R_{ON} C_L

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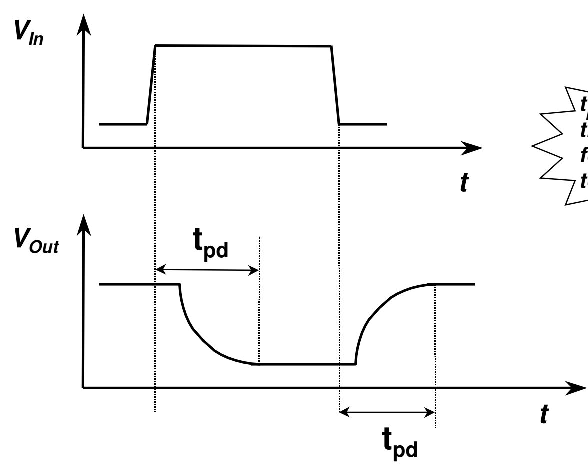
Signal Timing: Propagation Delay

Propagation delay t_{pd} is upper bound between new valid inputs and new valid output



t_{pd} includes time required for transistor to turn on/off

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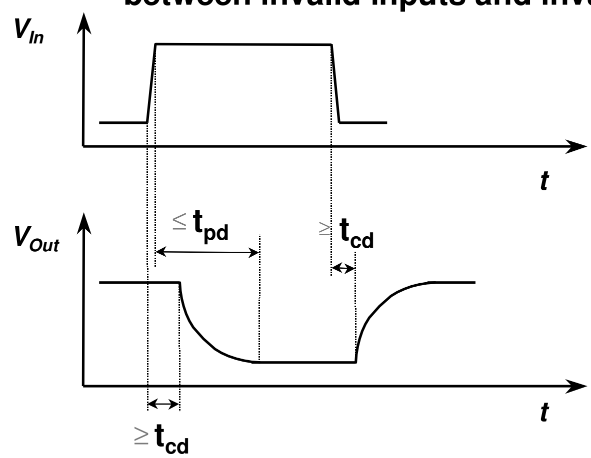
Signal Timing: Contamination Delay

Contamination delay t_{cd} is lower bound between invalid inputs and invalid output



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Formal Definitions

additive

- **Propagation delay t_{pd}: Worst case delay from new valid inputs to new valid outputs**
- **Contamination delay t_{cd}: Best case delay from invalid inputs to invalid outputs**

Over all input combinations, over all input-output paths

property of last stage

- **Rise time t_r: Signal transition time from invalid low to valid high**
- **Fall time t_f: Signal transition time from invalid high to valid low**

Not quite true, but a convenient assumption!

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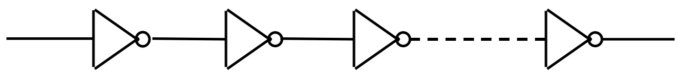
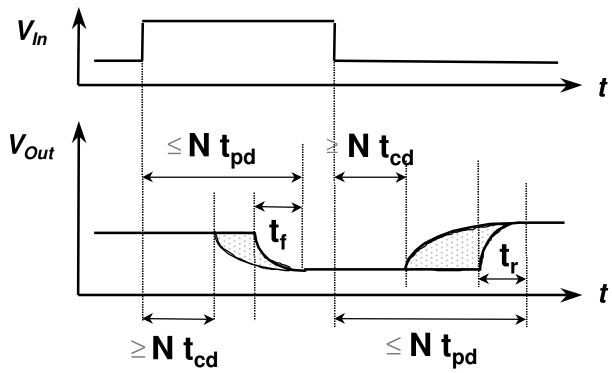
Cascaded Inverters



N inverters each with t_{pd} , t_{cd} , t_r , and t_f



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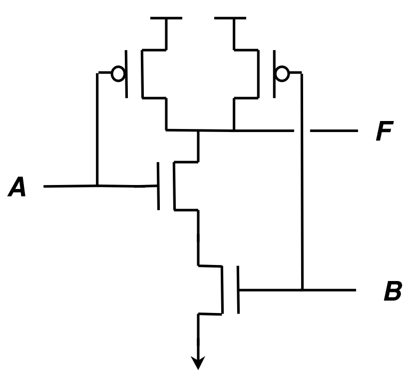
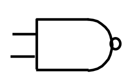
Logic Functions



A	B	F
0	0	1
0	1	1
1	0	1
1	1	0

This gate is a NAND gate ***Symbol:***



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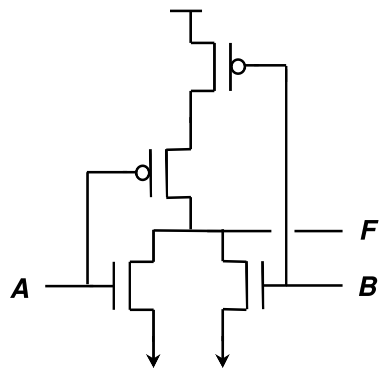
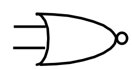
Logic Functions - II



A	B	F
0	0	1
0	1	0
1	0	0
1	1	0

This gate is a NOR gate ***Symbol:*** 

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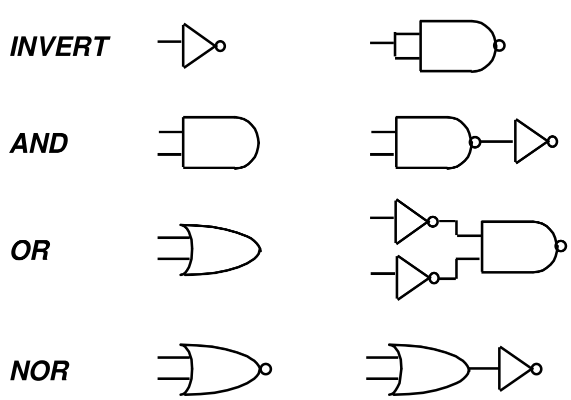
Combinational Composition

- **Can realize any logic function with a two-input NAND**



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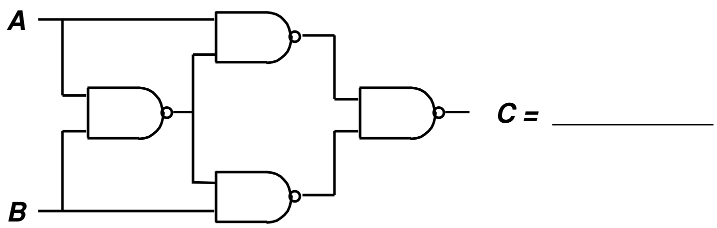
Combinational Composition - II



Logically valid A, B ⇒ Logically valid C (static discipline)

t_{pd} = 5 t_{cd} = 1 for each NAND gate

Propagation delay for circuit is ____________

Contamination delay for circuit is ___________

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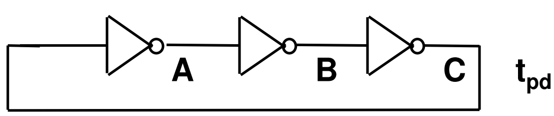
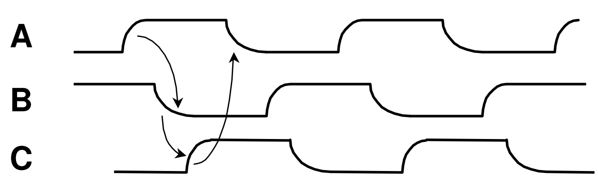
A Cyclic Circuit



- **Not combinational!**
- **Plausible behavior: Oscillates with period $6t_{pd}$**



- **Is the behavior guaranteed by static discipline?**
Answer: *NO!*

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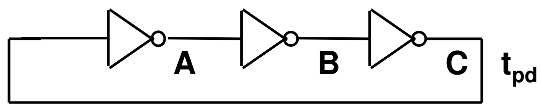
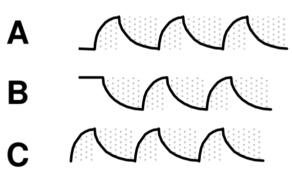
Other Behaviors

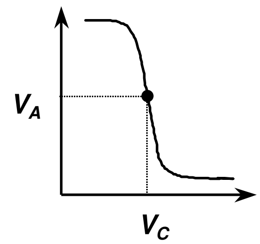


Continuous invalidity



If no signal is ever valid for t_{pd}

Steady DC signal



$V_A = V_B = V_C$, and are in the forbidden zone

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