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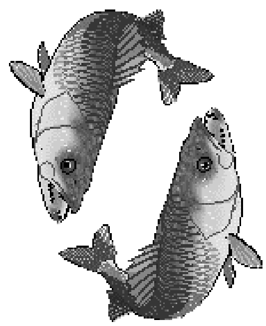
Feedback and State



1

Recap: Combinational Synthesis

Truth Table	*Logic Equation*	*Combinational Circuit*
ONE	*F = AB + BC ..*	*AND-OR*
	F = B (A + C) ..	*NAND-NAND*

t	*t+1*	*t+2*	*t+3*
0	*1*	*0*	*0*
1	*0*	*0*	*1*

→ *Combinational Logic* →

t	*t+1*	*t+2*	*t+3*
1	*1*	*0*	___

Limitation of combinational logic: __________

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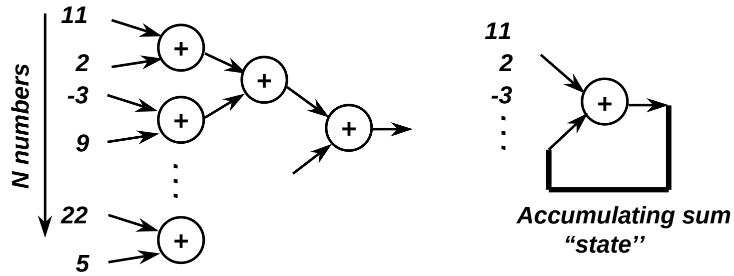
Motivation: Adding a column of numbers

Combinational | **Sequential**



Size grows as N
Delay grows as $\log_2 N$

Size is constant
Delay grows as N

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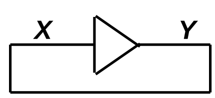
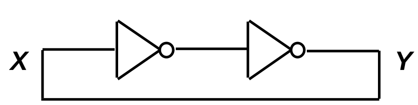
Implementing State

- **How about a single bit?**



- **Need to implement as**



$V_Y = INVERT(\ INVERT(\ V_X\ )\ )$
$V_Y = V_X$

Voltage transfer curve

What are the solutions?

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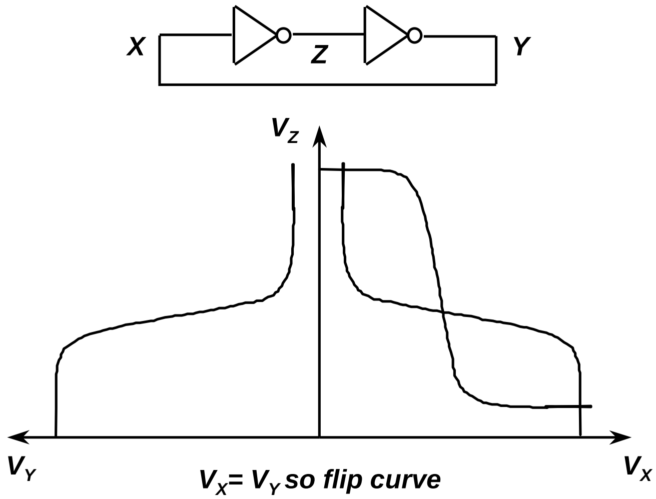
Implementing State - II



$V_X = V_Y$ so flip curve

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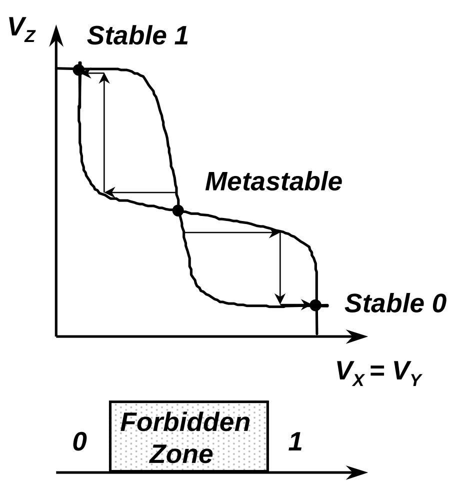
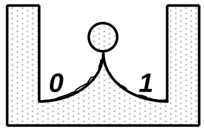
Solutions





probability of staying metastable = $A\ e^{-t/K}$

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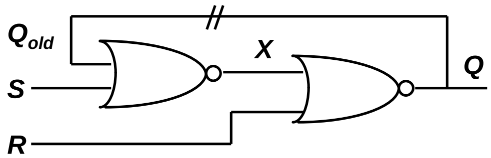
Forcing a 0 or a 1



S-R Latch

S	R	Q
0	0	Q_{old}
0	1	0
1	0	1
1	1	0

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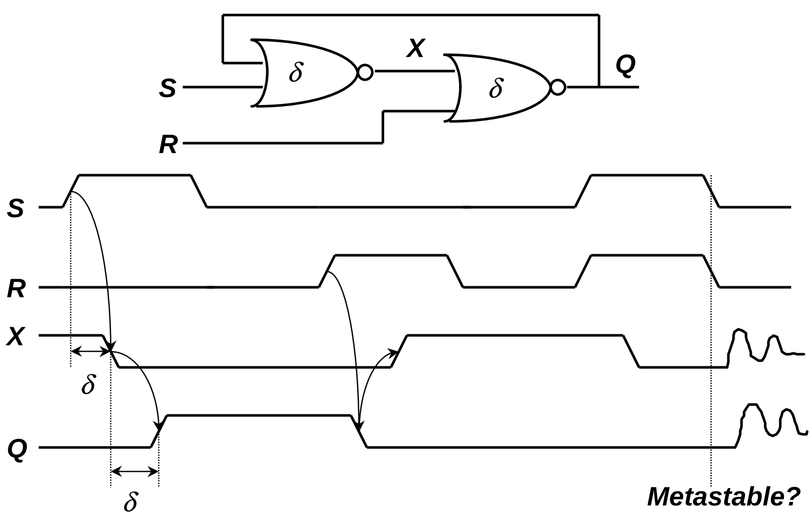
S-R Latch Timing



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Timing Rule

- Only one input can change "at the same time"
- Specifically,
  Input transitions only after
  state has settled
- We will cast this constraint in terms of setup time and hold time

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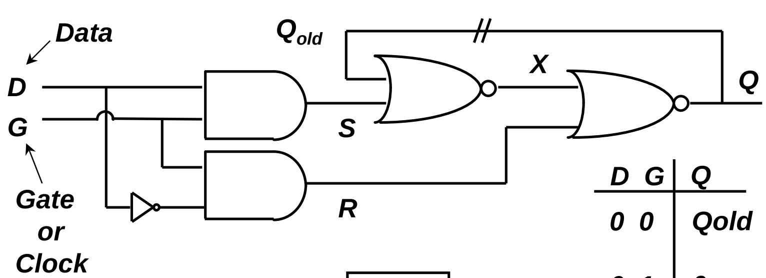
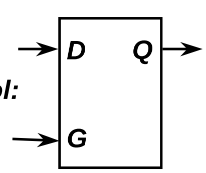
D-Latch or Transparent Latch



D	*G*	*Q*
0	*0*	*Qold*
0	*1*	*0*
1	*0*	*Qold*
1	*1*	*1*

Symbol:



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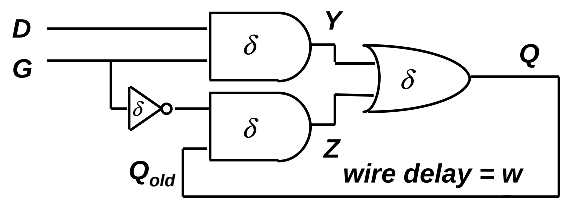
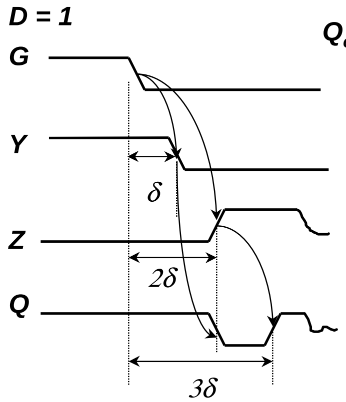
Simplified D-Latch





Only one input G changes to latch

Want Q to _______

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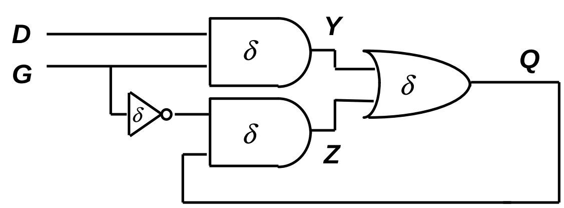
How do we fix it?



Karnaugh Map:

$\bar{G}Q$

D \ GQ	00	01	11	10
0	0	1	0	0
1	0	1	1	1

DG

Hazard due to moving from DG to $\bar{G}Q$

Eliminate hazard by adding gate

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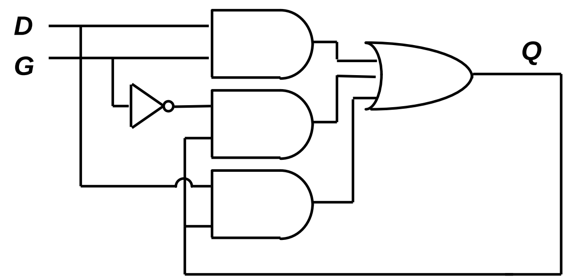
Fixed D-latch



$\bar{G}Q$

D \ GQ	00	01	11	10
0	0	1	0	0
1	0	1	1	1

DG

DQ

No problem for all single input transitions

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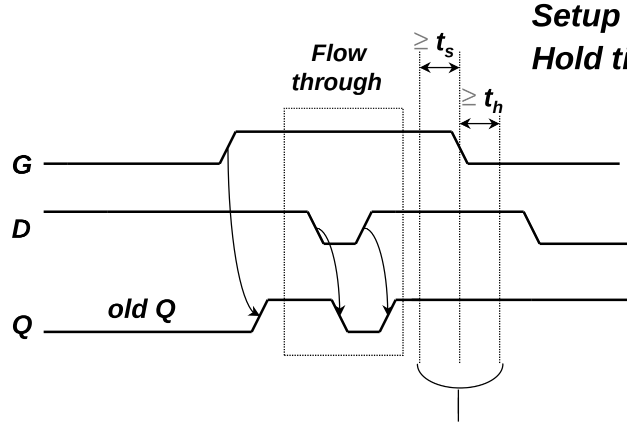
Timing of D-Latch

Setup time = t_s
Hold time = t_h



D must not change in this region

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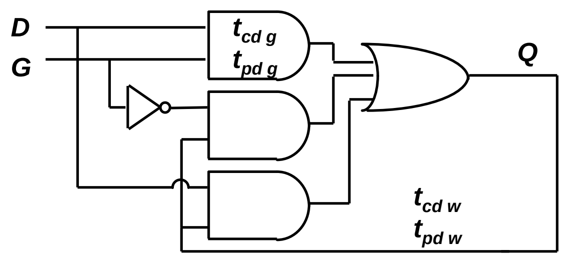
Setup and Hold Times



- Setup and hold times dependent on contamination and propagation delays of gates and wires
- Exhaustive transistor-level simulation required to determine setup and hold times accurately

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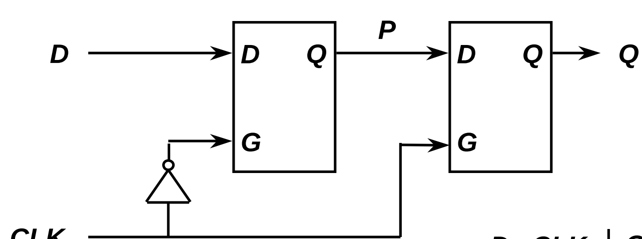
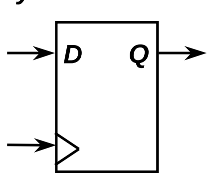
Edge-Triggered Flip-Flop



Symbol:



Sample edge?

D	CLK	Q
{0,1}	0	Q_{old}
{0,1}	1	Q_{old}
D	$\uparrow$	D
{0,1}	$\downarrow$	Q_{old}

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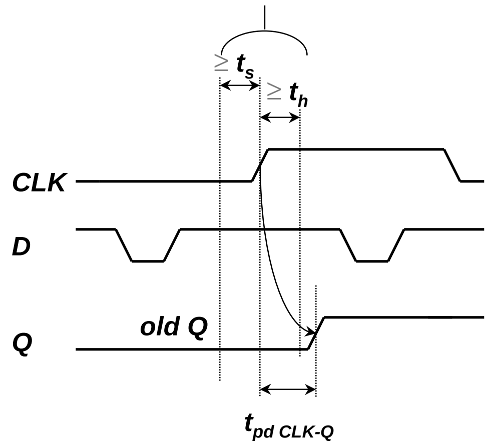
Timing of Edge-Triggered Flip-Flop

D must not change in this region



Setup time = t_s
Hold time = t_h

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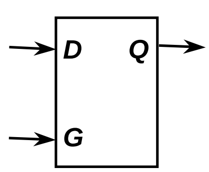
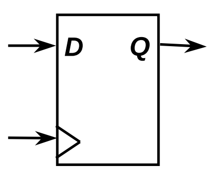
Latches and Flip-Flops



is like a toll-gate



is like an air-lock

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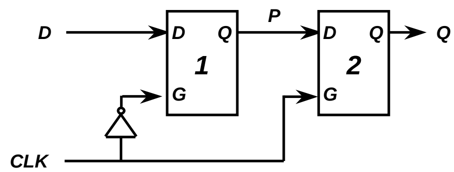
Latch 2 Hold Time (details in recitation)



- Consider hold time requirement for latch 2
  - Negative clock transition implies output Q freezes data
  - Should not have any glitch on output Q
  - But latch 1 output P is contaminated by change in G input!
- Hold time requirement of latch 2 should be less than accumulated contamination delay through inverter, and G-Q path of latch 1

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