Clocking and the Dynamic Discipline

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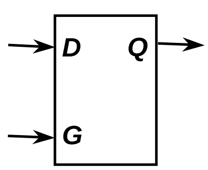
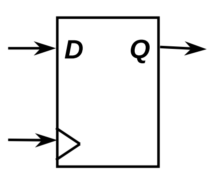
Recap: Latches and Flip-Flops



is like a toll-gate

Level-sensitive: if G is high then value of D flows through to Q



is like a air-lock

Edge-triggered: Q value updated on rising transition of clock. No direct path from D to Q

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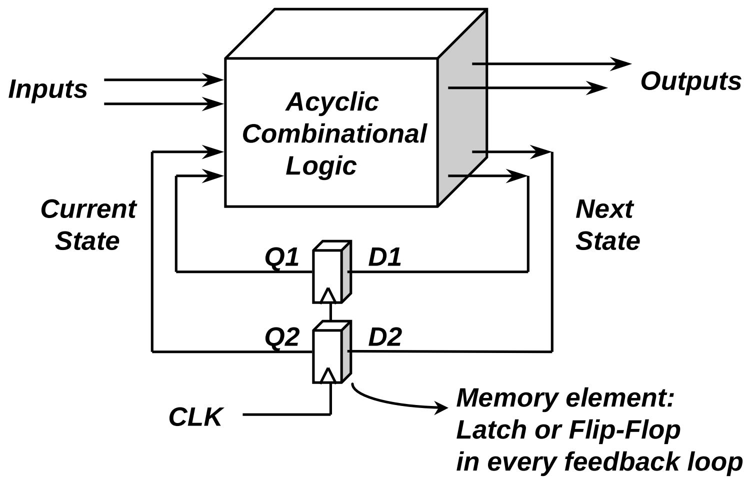
Synchronous Sequential Circuit



Issues: Specification, design, clocking and timing

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It is time to worry about timing...

- What memory element should we use in the feedback loop?
  - Edge-triggered flip-flop
  - Level-sensitive latch
- Given the choice of memory element how fast can we clock the logic circuit?
- What other timing constraints do we have to obey?
- What about asynchronous inputs?

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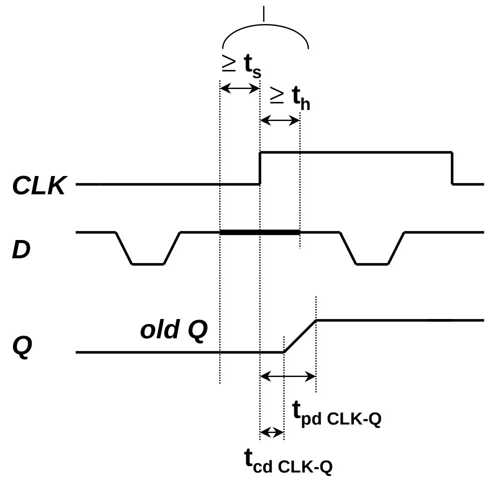
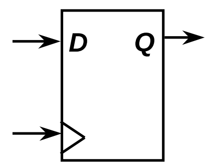
Edge-Triggered Flip-Flop Timing

D must not change in this region



Setup time = t_s
Hold time = t_h



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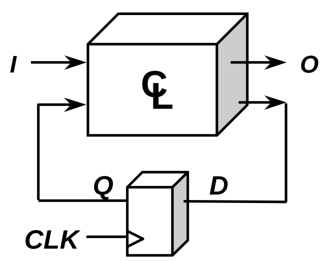
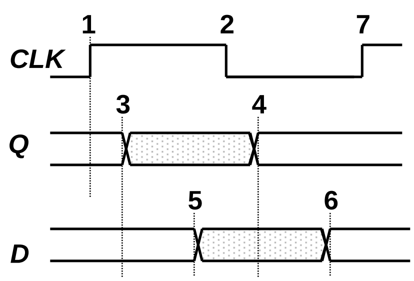
Synchronous Circuit: Clocked Flip-Flop





$t_{13} \geq$ ____ $t_{35} \geq$ ____ $t_{14} \leq$ ____ $t_{46} \leq$ ____

Timing rules for flip-flop dictate:

$t_{67} \geq$ ____ $t_{15} \geq$ ____

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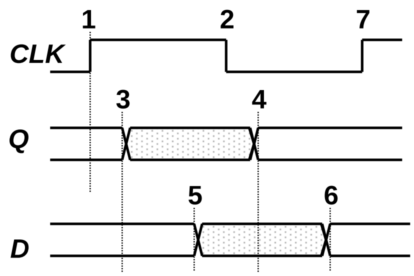
Flip-Flop Clocking Rules



Clock period = t_{17}

$$t_{17} = (t_{14} + t_{46} + t_{67}) \geq t_{pd\ C\text{-}Q} + t_{pd\ C.\ L.} + t_s$$

Hold time constraint:

$$t_{15} = (t_{13} + t_{35}) \geq t_h \Rightarrow t_{cd\ C\text{-}Q} + t_{cd\ C.L.} \geq t_h$$

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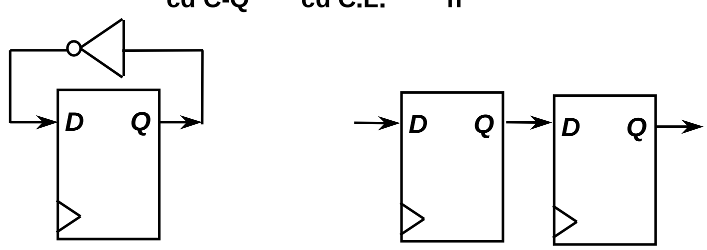
Hold Time Constraint for Flip-Flop

$$t_{cd\ C\text{-}Q} + t_{cd\ C.L.} \geq t_h$$



1-bit Counter **Shift Register**

We should design the flip-flop so ______________

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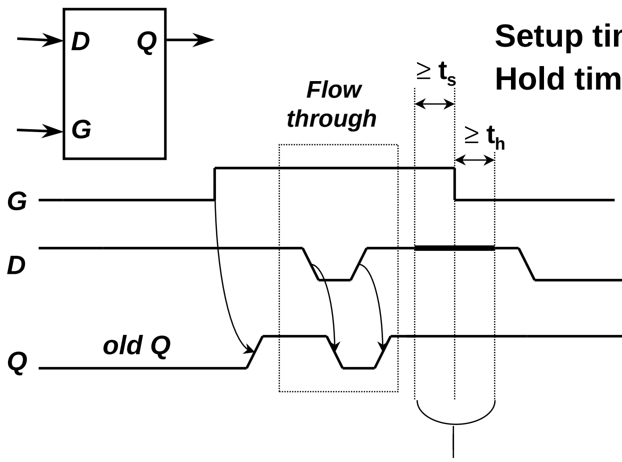
Transparent D-Latch Timing

Setup time = t_s
Hold time = t_h



D must not change in this region

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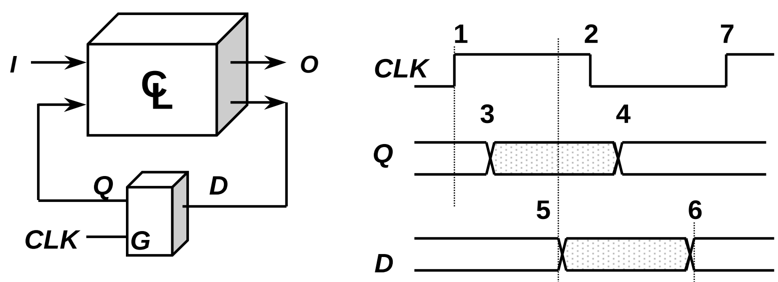
Synchronous Circuit: Clocked Latch



Will the clock shown above work?

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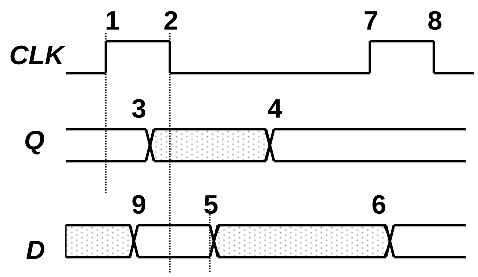
Avoiding Races: Latch Clocking Rules



Need $t_{25} > 0$ to avoid race condition

Timing rules for latch dictate:

$t_{25} \geq t_h \Longrightarrow t_{15} - t_{12} \geq t_h$

$t_{12} \leq t_{13} + t_{35} - t_h \Longrightarrow t_{12} \leq t_{cd\ C\text{-}Q} + t_{cd\ C.L.} - t_h$

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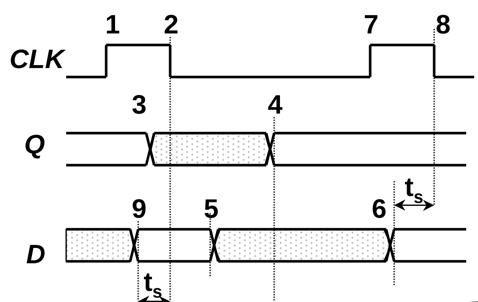
Clock Period Constraint for Latch



Assume same as $t_{pd\ C\text{-}Q}$

Clock period = $t_{28} = t_{96}$

$t_{96} = (t_{94} + t_{46}) \geq t_{pd\ D\text{-}Q} + t_{pd\ C.L.}$

assuming all other timing rules are satisfied!

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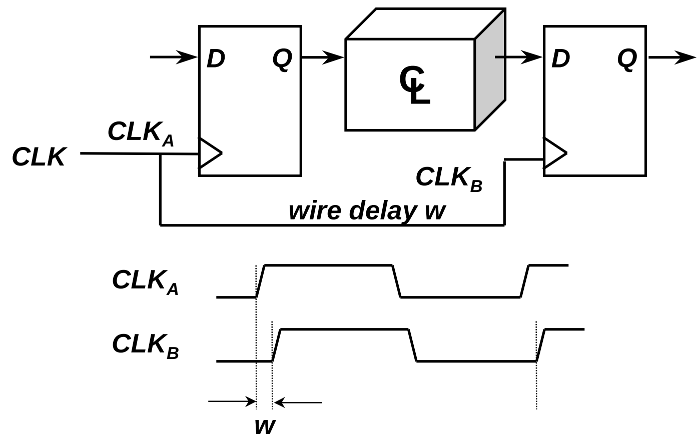
Clock Skew



Skew affects clock period and hold time constraints

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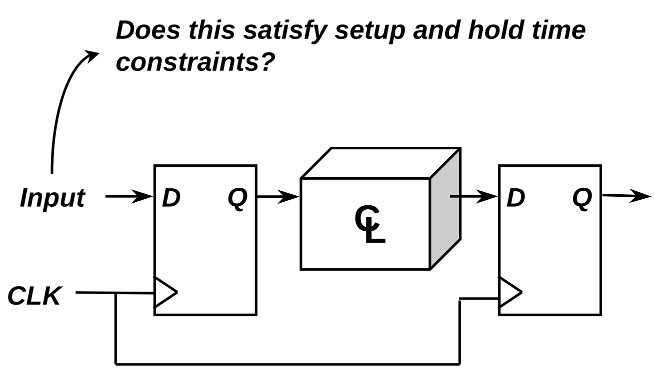
Asynchronous Inputs = Trouble



Need to sample asynchronous inputs reliably

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