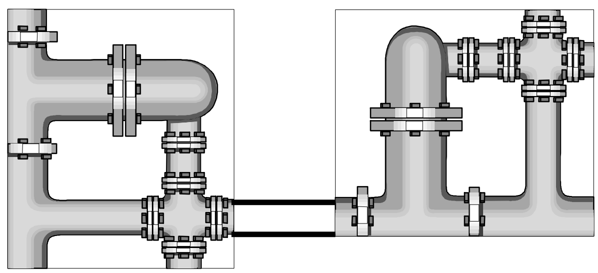
6004 Spring 1998: L16

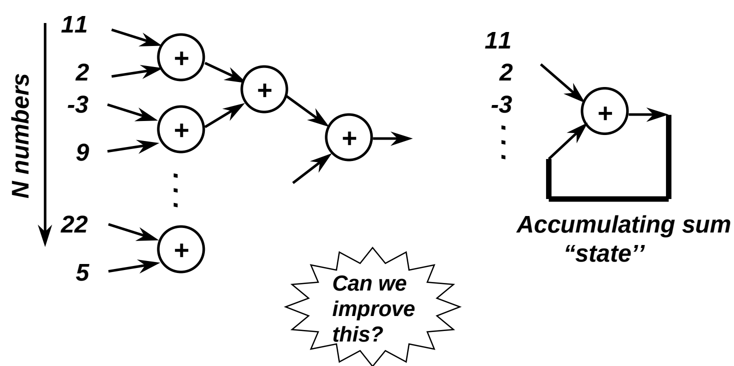
Pipelining



1

Motivation: Adding a column of numbers

Combinational ***Sequential***



Size grows as N
Delay grows as log_2N

Size grows as 1
Delay grows as N

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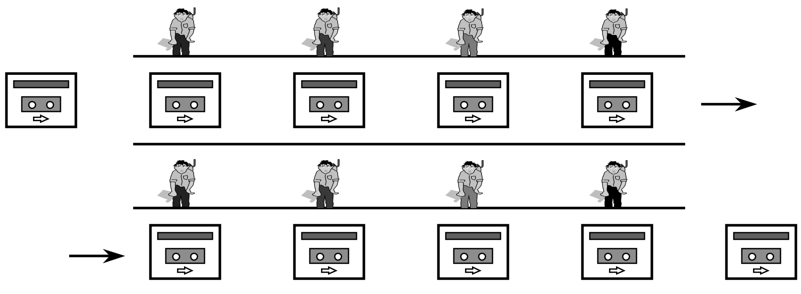
Observe… An Assembly Line



- **Length L objects (and workers), moves at rate R objects/minute**
- **Each task should take at most _____ minutes**
- **An object is processed in _________ minutes**
- **Workers always have an object in front of them**

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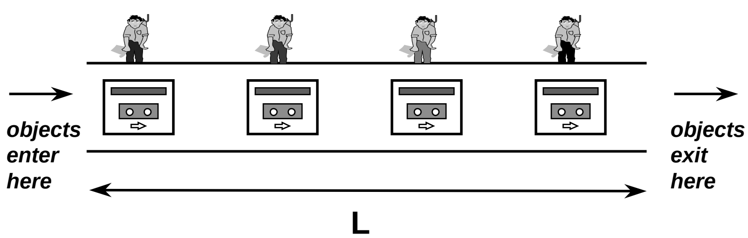
Definitions



- **Latency: Time for one object to pass through the system is L/R**
- **Throughput: Rate of objects going through is R**

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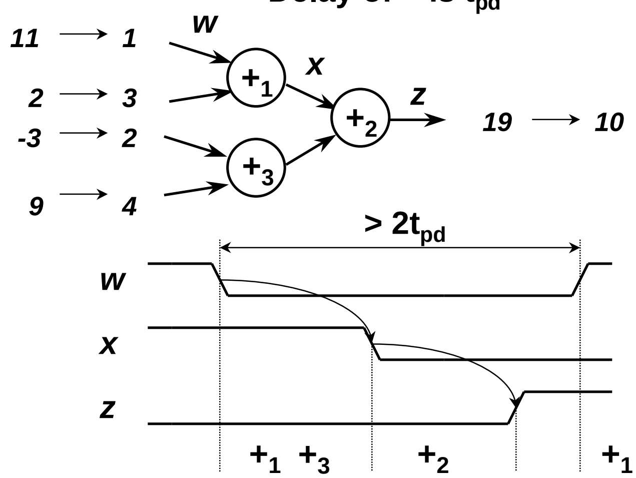
Adding Numbers: A Closer Look

Delay of + is t_{pd}



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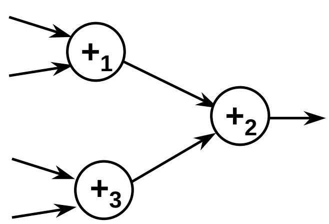
Combinational Throughput and Latency



Delay of + is t_{pd}

Latency = $2\ t_{pd}$

Throughput = $\frac{1}{2\ t_{pd}}$

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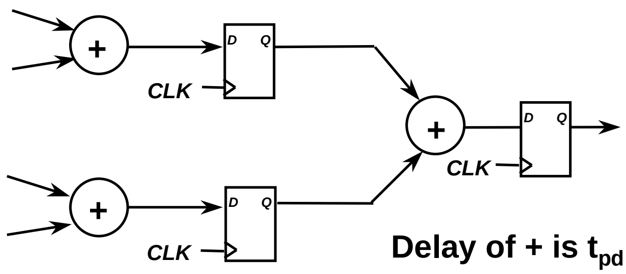
Pipelined Throughput and Latency



Delay of + is t_{pd}

Latency = ________

Throughput = ________

Assume zero setup and hold times and zero flip-flop propagation delays for this lecture only!

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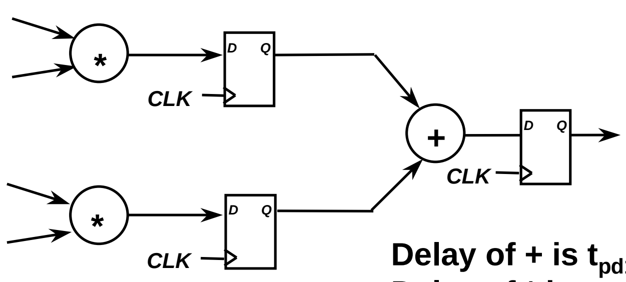
Inhomogenous Pipeline



Delay of + is t_{pd1}
Delay of * is t_{pd2}

Latency = ________

Throughput = ________

Assume zero setup and hold times, and zero flip-flop propagation delays for this lecture only!

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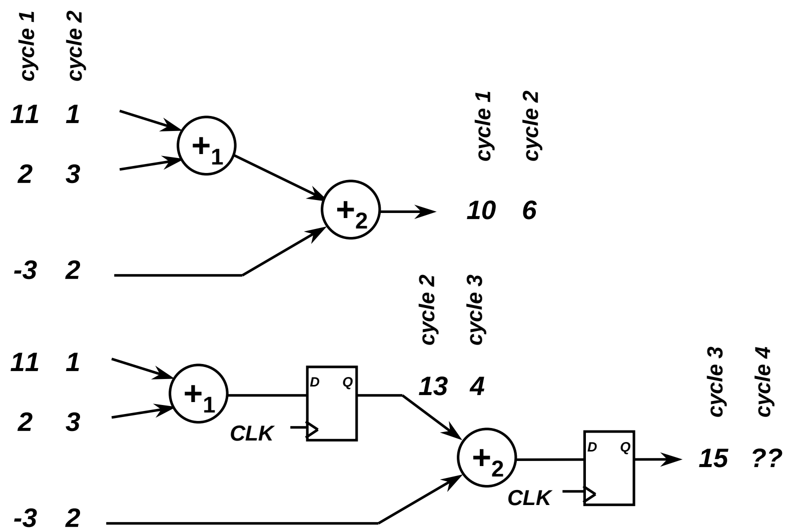
ILL-Formed Pipelines



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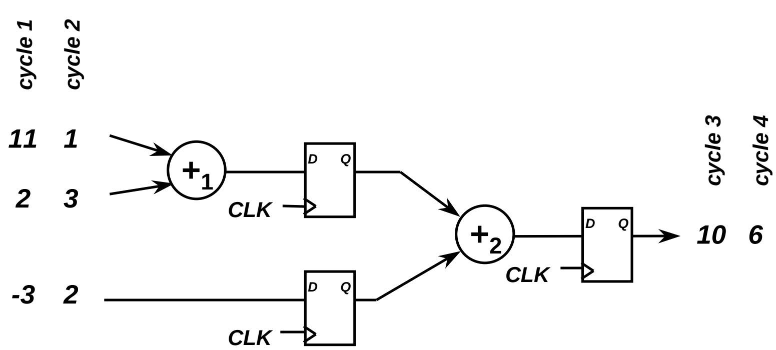
Pipeline Well-Formedness

- **Same number of flip-flops along any path from any input to any output**
  - **Insures that every computational unit sees inputs in phase**



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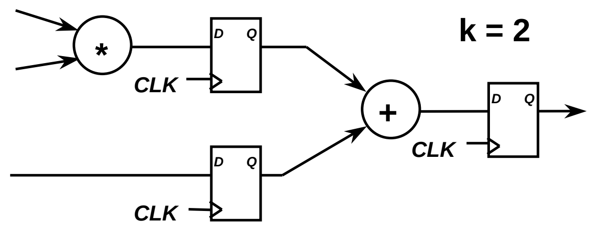
k-Pipelines

- k flip-flops on each input-output path
- Always have flip-flops on each output



Clock period is maximum propagation delay from flip-flop output (or circuit input) to flip-flop input

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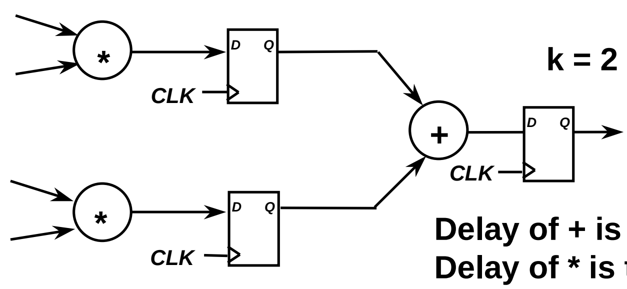
Throughput and Latency of k-Pipelines



Delay of + is t_{pd1}
Delay of * is t_{pd2}

Clock period = MAX(t_{pd1}, t_{pd2})

Throughput in terms of clock period = $\frac{1}{\text{clock period}}$

Latency in terms of clock period = k * clock period

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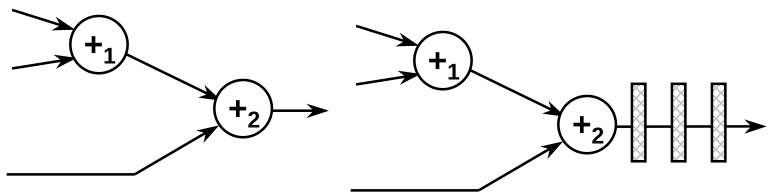
k-Pipelines from Combinational Logic

- **Add k flip-flops to every output**



3-pipeline

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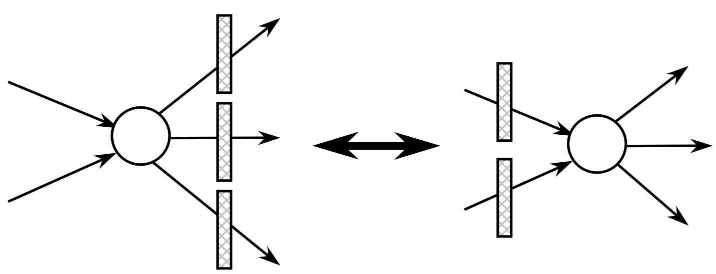
Transforming k-Pipelines



- **Transformation does not change k**
- **Transformation can change number of flip-flops, affect clock period and therefore throughput and latency**

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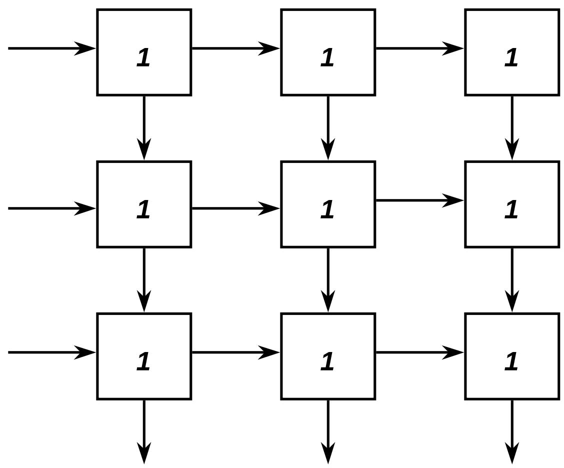
2-Dimensional Combinational Circuit



Throughput = __________

Latency = __________

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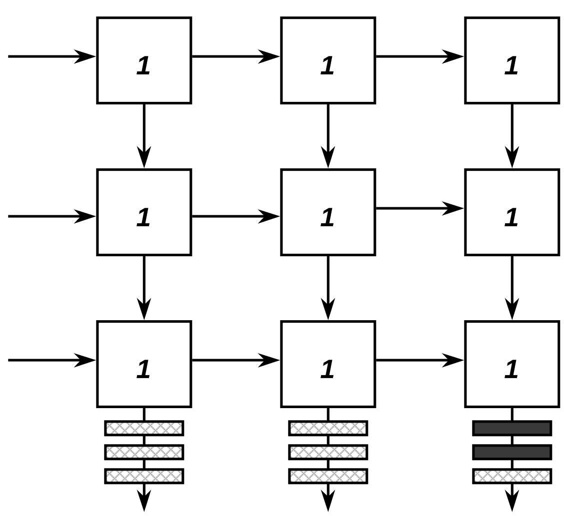
Initial 3-Pipeline



Clock period = __________

Throughput = __________

Latency = __________

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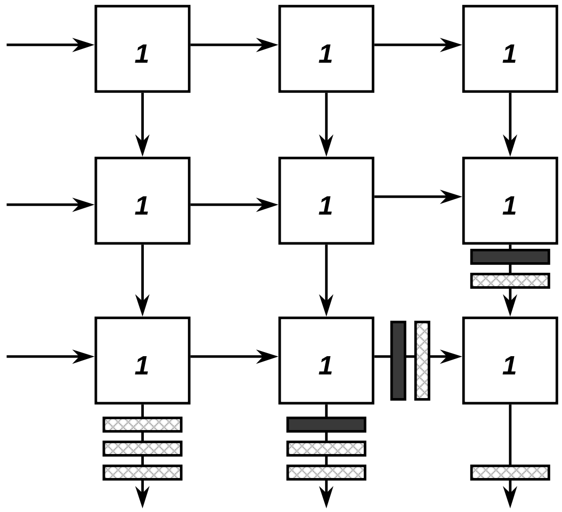
Transformed Pipeline - I



Clock period = ________

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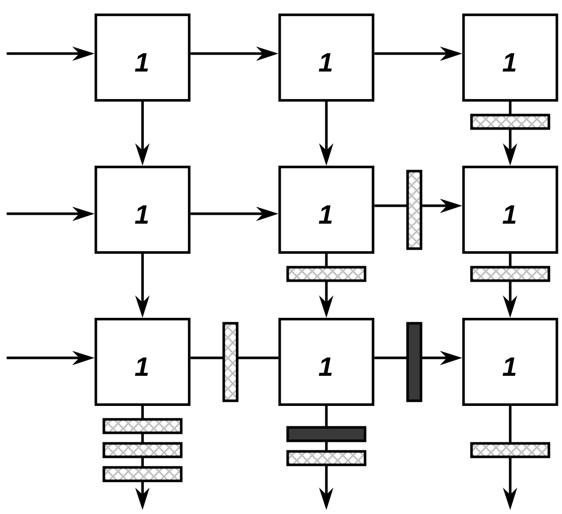
Transformed Pipeline - II



Clock period = ________

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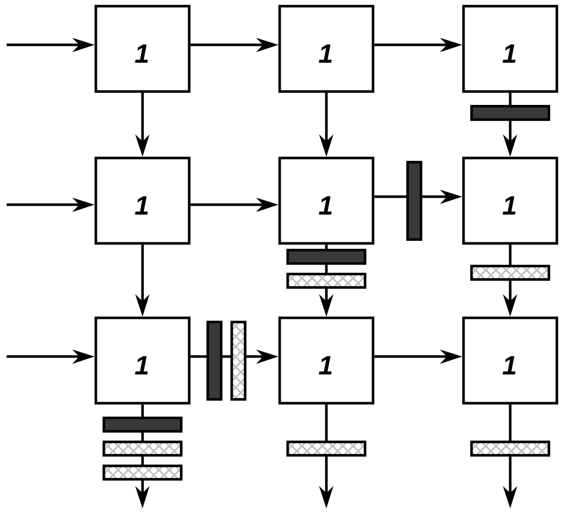
Transformed Pipeline - III



Clock period = ________

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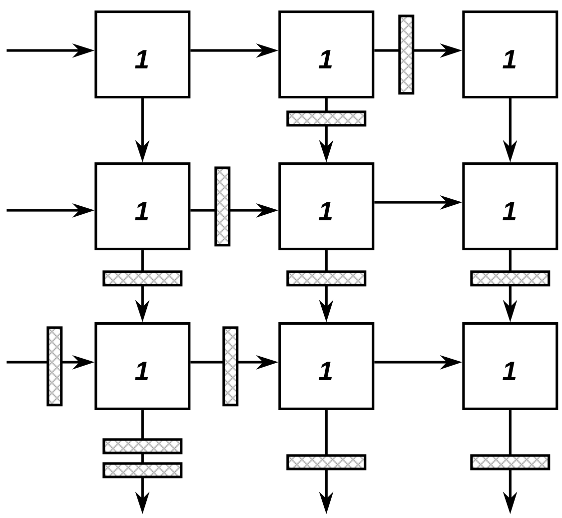
Fastest 3-Pipeline



Clock period = ________

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Pipeline Optimization

How do you <u>systematically</u> find:

- **Maximum throughput (minimize clock period)**
- **Maximum throughput for a given number of stages k**
- **Minimum number of stages k for a given throughput**
- **Minimum number of flip-flops for a given throughput**

Ask Prof. Charles Leiserson, NE43-201
Laboratory for Computer Science

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