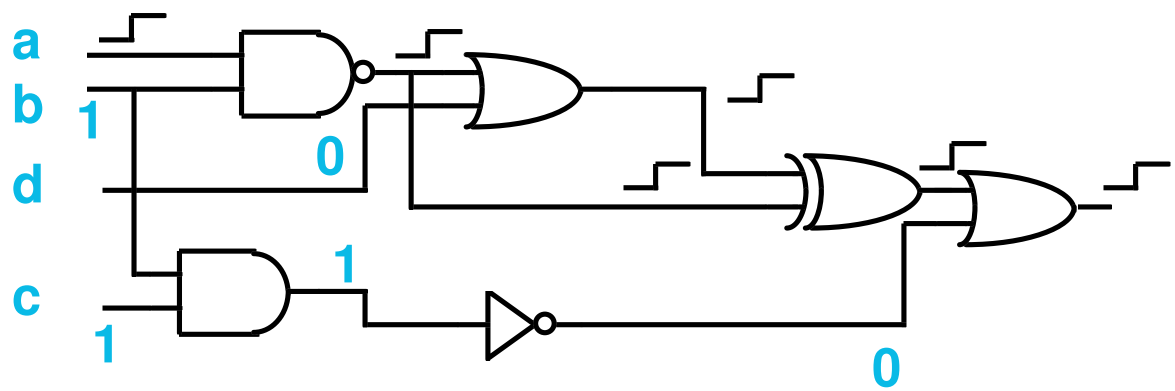
Testability of Multilevel Circuits

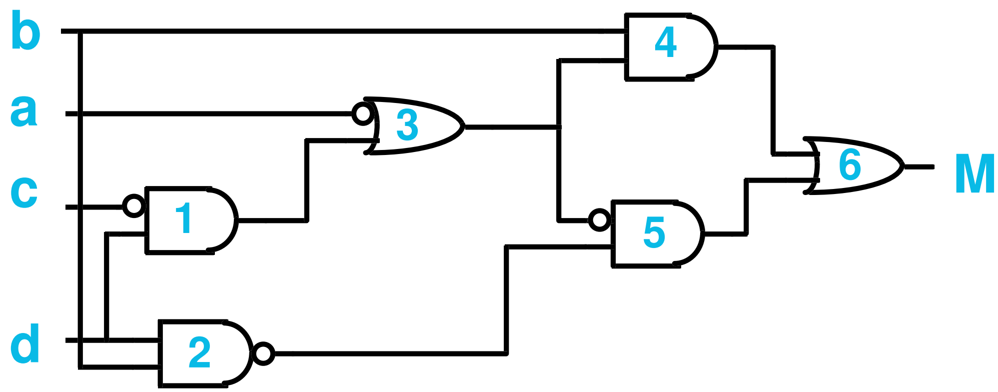
Were able to obtain necessary and sufficient conditions for robust path-delay-fault and multi-fault testability based on primality and irredundancy for two-level circuits



What about multilevel circuits?

Equivalent Normal Form

ENF is a two-level representation of a multilevel circuit



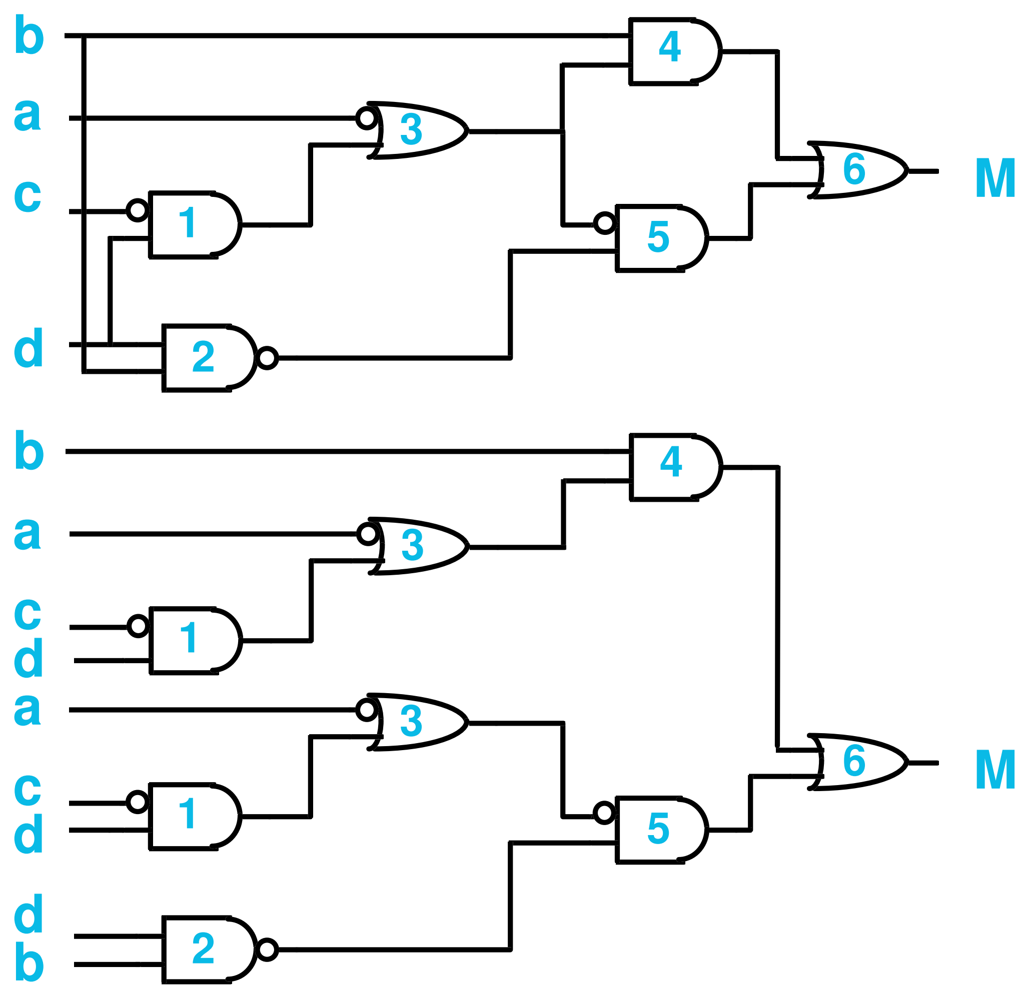
$$E_M = b_{4,6}\,\overline{a}_{3,4,6} + b_{4,6}\,\overline{c}_{1,3,4,6}\,d_{1,3,4,6}$$

$$+ a_{3,5,6}\,c_{1,3,5,6}\,\overline{d}_{2,5,6} + a_{3,5,6}\,c_{1,3,5,6}\,\overline{b}_{2,5,6}$$

$$+ a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{d}_{3,5,6} + a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{b}_{2,5,6}$$

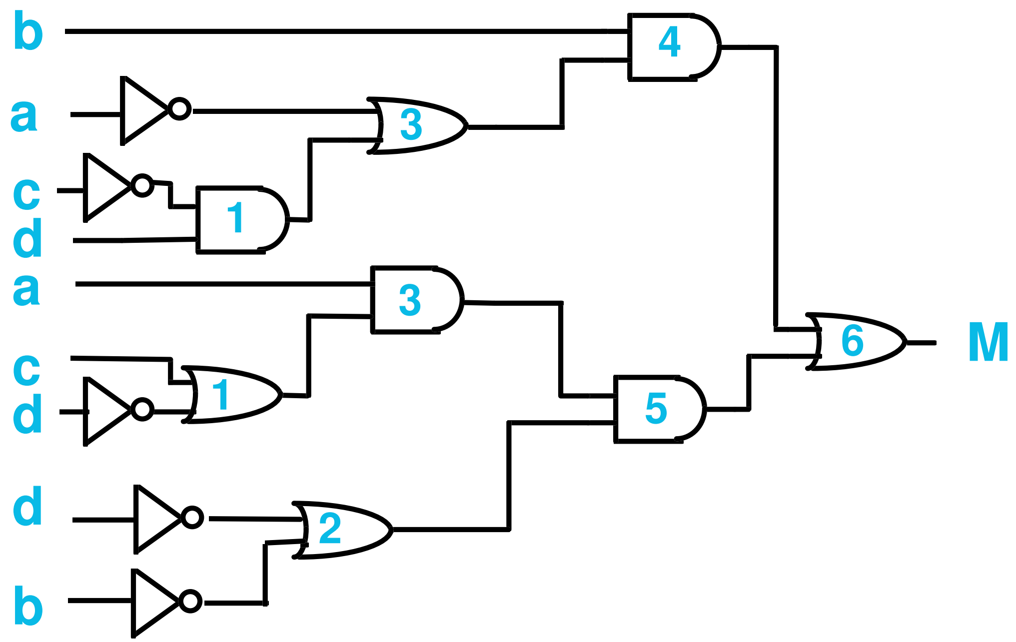
Computing the ENF

Make the circuit fanout-free internally



Computing the ENF - 2

Push inverters to primary inputs



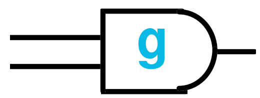
There is a one-to-one correspondence between paths in above circuit and original circuit.

– Compute ENF by “flattening” circuit to sum-of-products form without using Boolean identities like $a.a \equiv a$, $a.\overline{a} \equiv 0$, etc.

Rules for ENF Computation

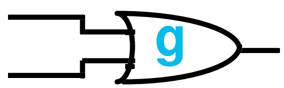
Primary inputs' ENF $\equiv$ primary input literal

a_A b_B



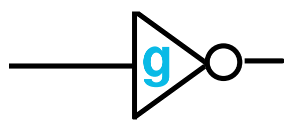
$a_{A,g} \bullet b_{B,g}$

a_A b_B



$a_{A,g} + b_{B,g}$

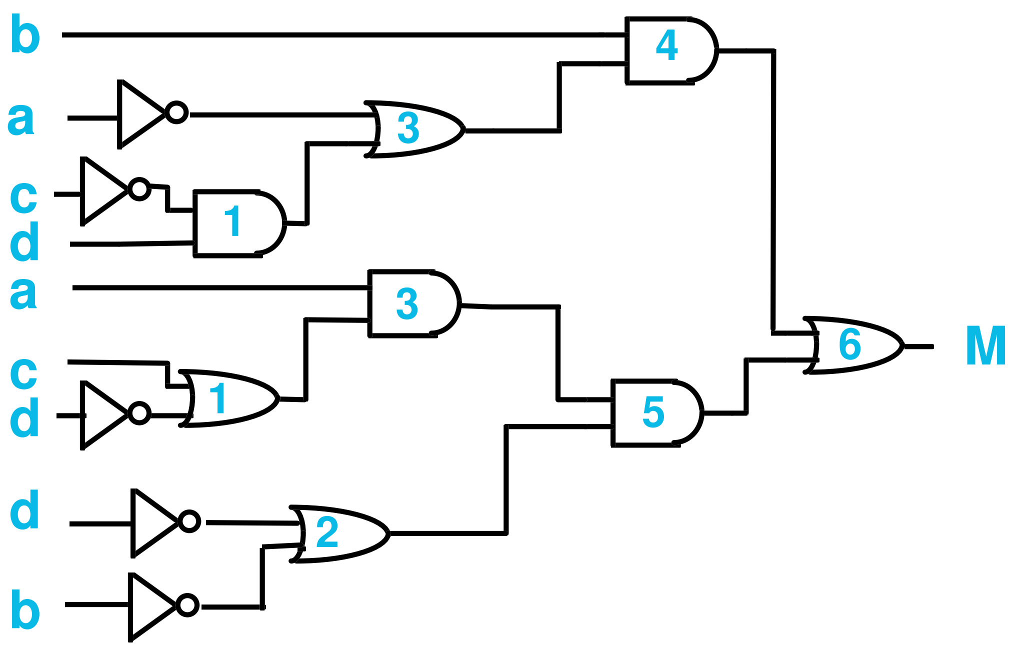
a_A



$\bar{a}_{A,g}$

Do not use Boolean identities

ENF Example



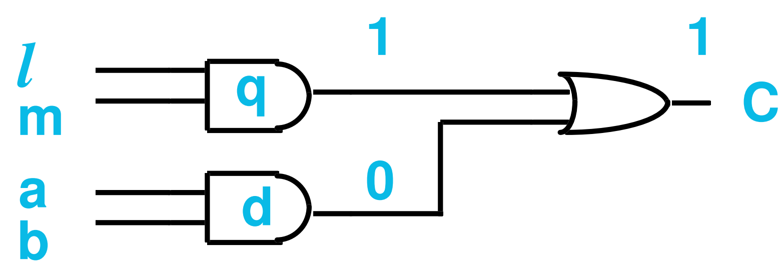
$$E_M = b_{4,6}\,\overline{a}_{3,4,6} + b_{4,6}\,\overline{c}_{1,3,4,6}\,d_{1,3,4,6}$$

$$+\ a_{3,5,6}\,c_{1,3,5,6}\,\overline{d}_{2,5,6} + a_{3,5,6}\,c_{1,3,5,6}\,\overline{b}_{2,5,6}$$

$$+\ a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{d}_{3,5,6} + a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{b}_{2,5,6}$$

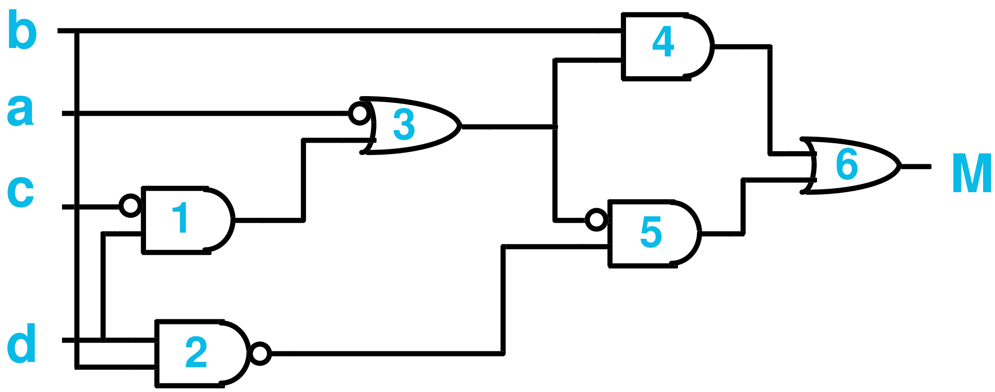
Relatively Essential Vertices (REVs)

In a two-level circuit



Vector which is relatively essential vertex of q was required for robust path delay fault test for path from *l* in q

Paths and Path-Cube-Complexes

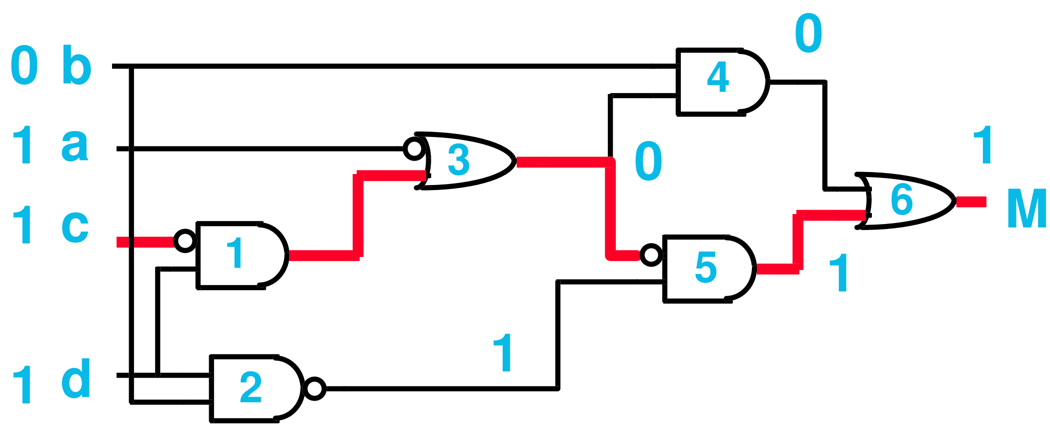


$$E_M = b_{4,6}\,\overline{a}_{3,4,6} + b_{4,6}\,\overline{c}_{1,3,4,6}\,d_{1,3,4,6}$$
$$+ a_{3,5,6}\,c_{1,3,5,6}\,\overline{d}_{2,5,6} + a_{3,5,6}\,c_{1,3,5,6}\,\overline{b}_{2,5,6}$$
$$+ a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{d}_{3,5,6} + a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{b}_{2,5,6}$$

Path a,3,4,6
Path-cube-complex is $b_{4,6}\,\overline{a}_{3,4,6}$

Path b,2,5,6
Path-cube-complex $a_{3,5,6}\,c_{1,3,5,6}\,\overline{b}_{2,5,6} + a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{b}_{2,5,6}$

REVs and Path-Cube-Complexes



$$E_M = b_{4,6}\,\overline{a}_{3,4,6} + b_{4,6}\,\overline{c}_{1,3,4,6}\,d_{1,3,4,6}$$
$$+ a_{3,5,6}\,c_{1,3,5,6}\,\overline{d}_{2,5,6} + a_{3,5,6}\,c_{1,3,5,6}\,\overline{b}_{2,5,6}$$
$$+ a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{d}_{3,5,6} + a_{3,5,6}\,\overline{d}_{1,3,5,6}\,\overline{b}_{2,5,6}$$

R.E.V. of path-cube-complex of path $c_{1,3,5,6}$ is the

R.E.V. of $a_{3,5,6}\,c_{1,3,5,6}\,\overline{d}_{2,5,6} + a_{3,5,6}\,c_{1,3,5,6}\,\overline{b}_{2,5,6}$

$V_2 = 1011$

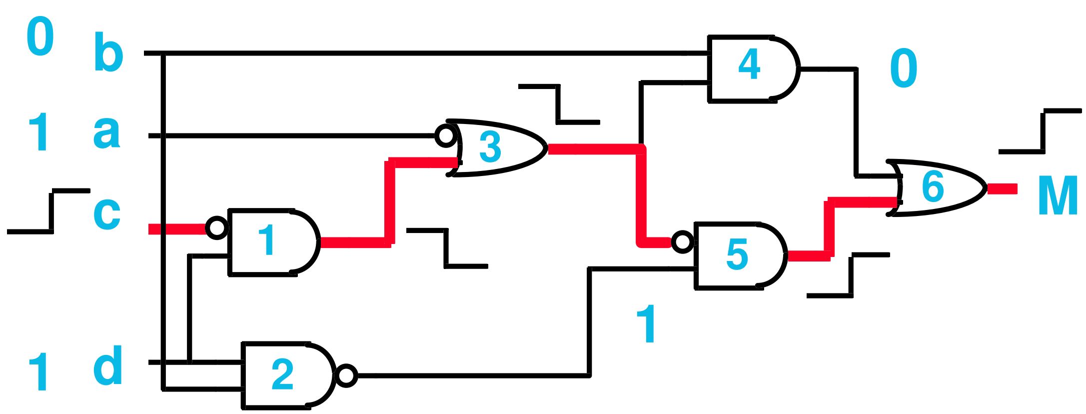
Testability Result

Theorem: A path Π be a path beginning from input l in a multilevel circuit C is testable if and only if there exists a vector pair $<V_1, V_2>$ such that

1) V_2 is a relatively essential vertex of the path-cube-complex of Π
2) Vertex V_1 distance-1 from V_2 in l is in the OFF-set of C.

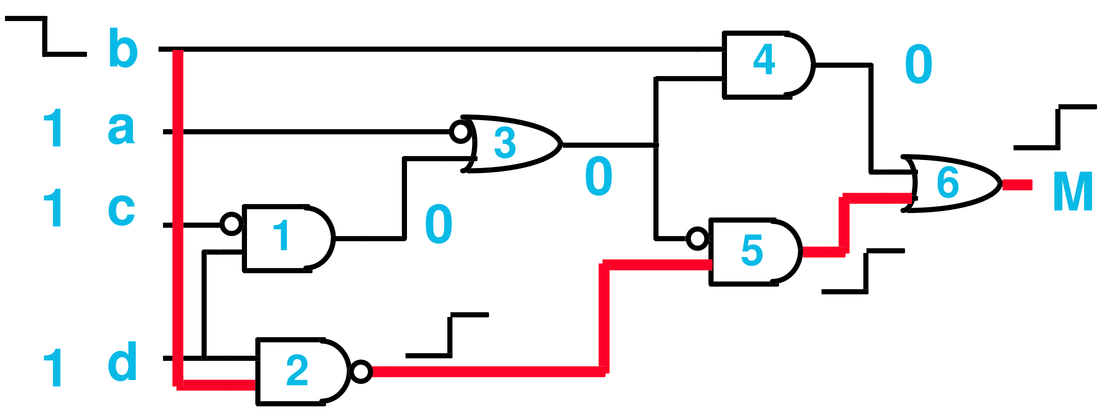
Exactly the same as the two-level case!

Path Delay Fault Tests



$V_1 = 1001$
$V_2 = 1011$

R.E.V. of $c_{1,3,5,6}$

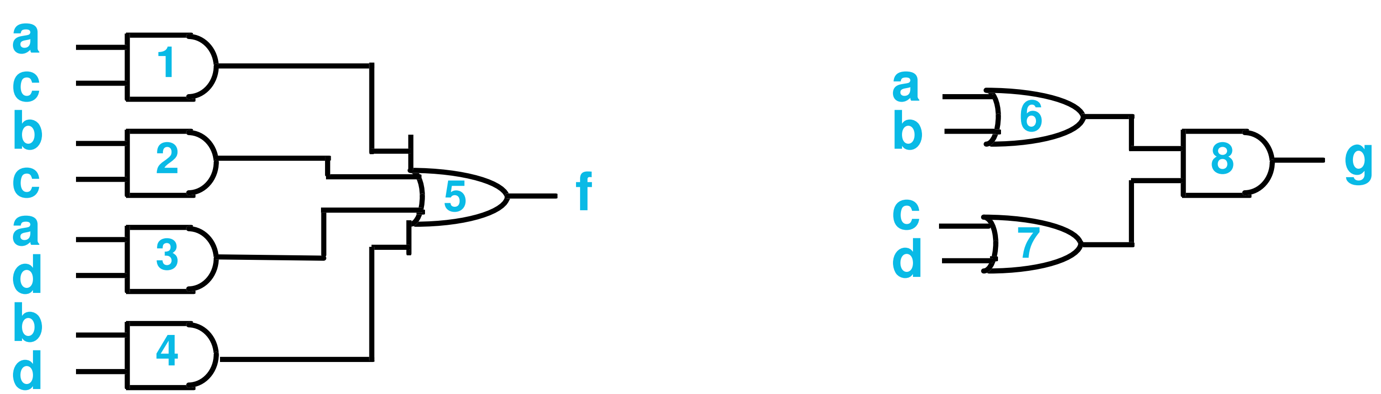


$V_1 = 1111$
$V_2 = 1011$

R.E.V. of $\overline{b}_{2,5,6}$

Algebraic Factorization

ENFs of two-level circuit and algebraically factored multilevel circuit are identical except for a renaming of tags.



$$E_f = a_{1,5}\, c_{1,5} + b_{2,5}\, c_{2,5} + a_{3,5}\, d_{3,5} + b_{4,5}\, d_{4,5}$$

$$E_g = a_{6,8}\, c_{7,8} + b_{6,8}\, c_{7,8} + a_{6,8}\, d_{7,8} + b_{6,8}\, d_{7,8}$$

ENF Reducibility

Not only are ENF's syntactically identical there is a many-to-one mapping of tags from two-level circuit to multilevel circuit

$$E_f = a_{1,5}\, c_{1,5} + b_{2,5}\, c_{2,5} + a_{3,5}\, d_{3,5} + b_{4,5}\, d_{4,5}$$

$$E_g = a_{6,8}\, c_{7,8} + b_{6,8}\, c_{7,8} + a_{6,8}\, d_{7,8} + b_{6,8}\, d_{7,8}$$

$$\{a_{1,5},\ a_{3,5}\} \rightarrow a_{6,8}$$

$$\{b_{2,5},\ b_{4,5}\} \rightarrow b_{6,8}$$

etc.

ENF Reducibility Implications

In two-level circuit each path-cube-complex consists of exactly one cube

In multilevel circuit each path-cube-complex can have more than one cube

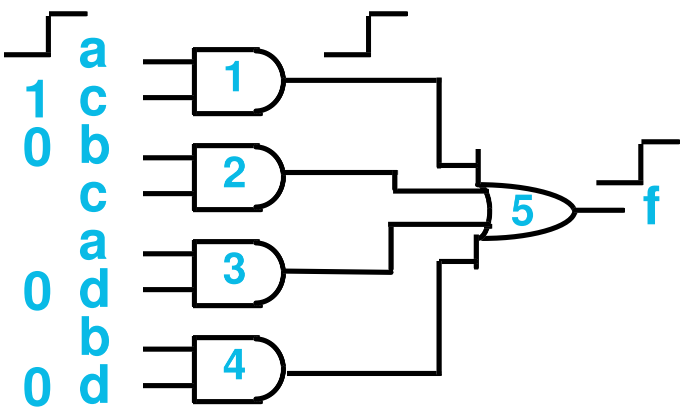
OFF-sets of circuits are the same, and relatively essential vertices of cubes stay the same.

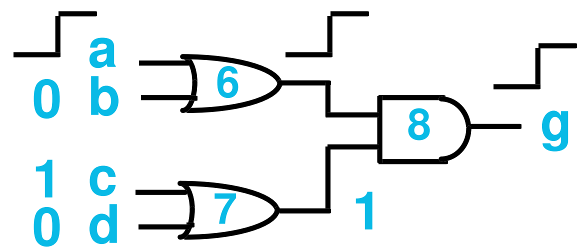
Therefore, testability and test vector sets are maintained.

Synthesis Procedures

If two-level circuit has full path-delay fault testability, algebraically factored circuit will have full testability.

Same vectors can be applied.





Similar result for multifaults.

Multifault Equivalence