LEAP Shared Memories: Automating the Construction of FPGA Coherent Memories

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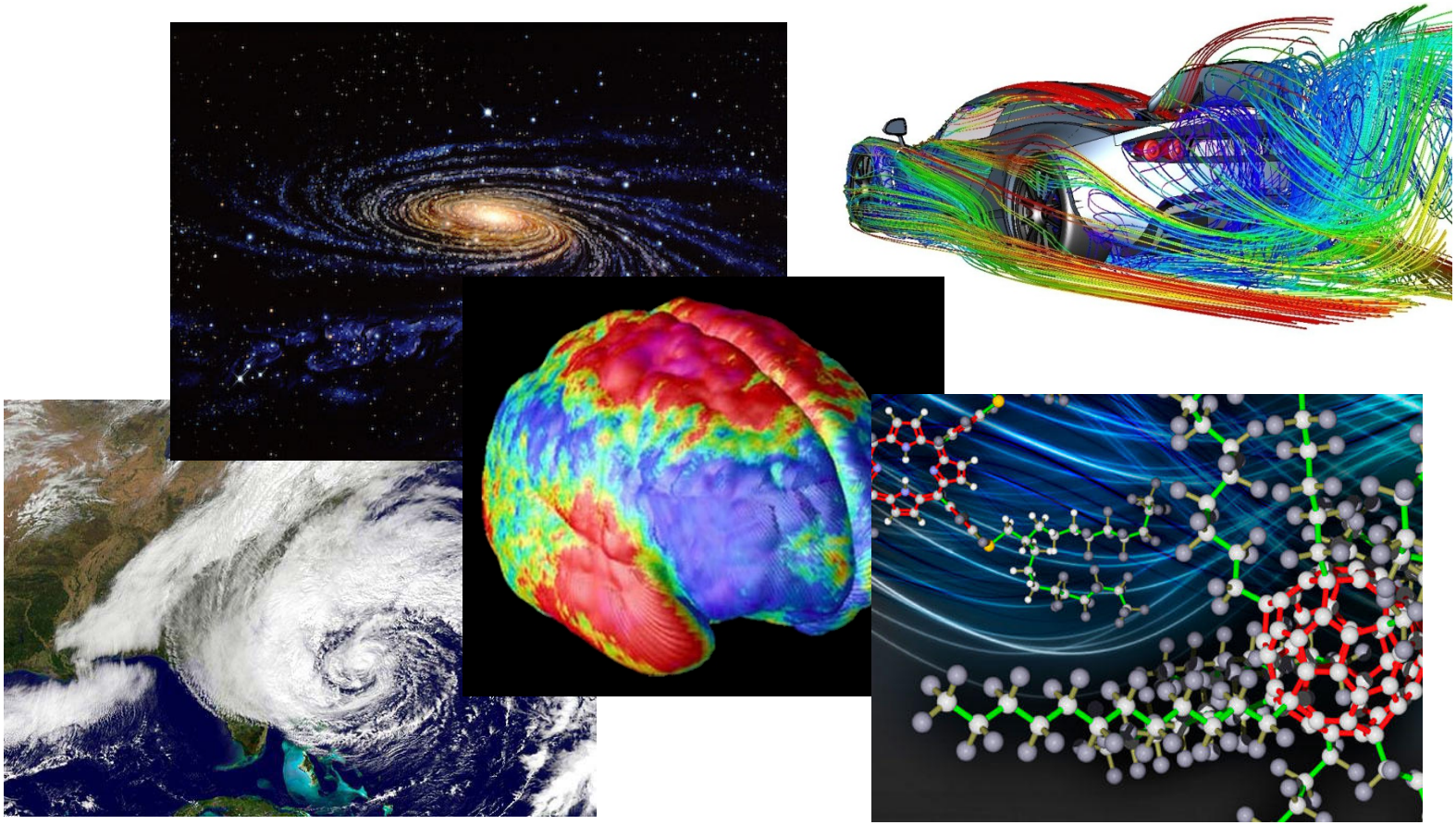
[†] Massachusetts Institute of Technology
[‡] Intel Corporation

May 12th, FCCM 2014

Motivation

- **Goal: simplifying parallel programming on FPGAs**



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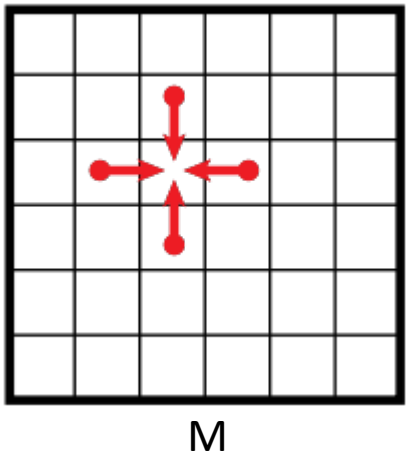
- **Goal: simplifying parallel programming on FPGAs**
- **2D Heat Transfer Equation**



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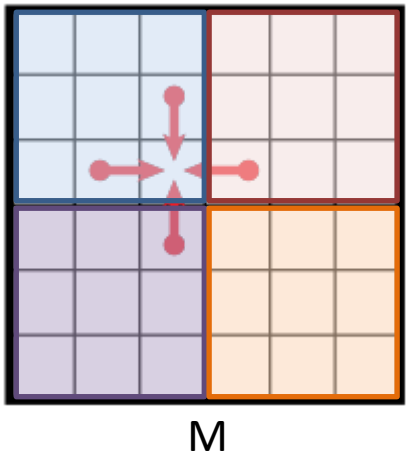


```
for(int t = 0; t < T; t++){
  #pragma omp parallel num_threads(4){
    int thread_id = omp_get_thread_num();
    int bid_x = thread_id%2;
    int bid_y = thread_id/2;
    for (int y = bid_y*(N/2); y < (1+bid_y)*(N/2); y++)
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        U[t+1,x,y] = C0*U[t,x,y]
                   + Cx*(U[t,x-1,y]+U[t,x+1,y])
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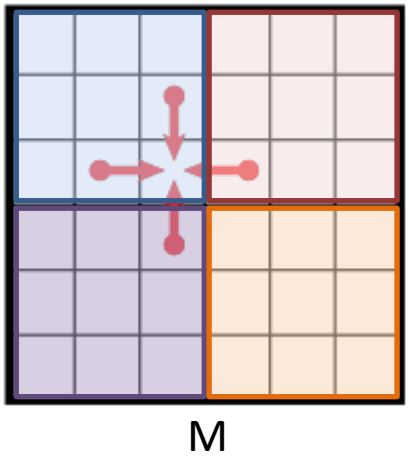


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operation on the shared array

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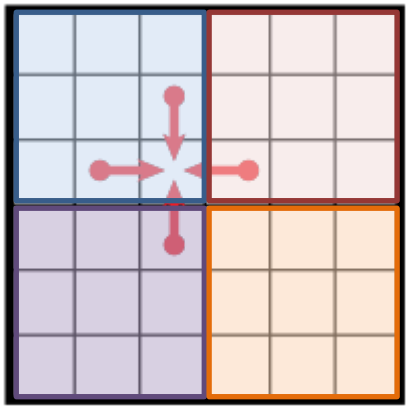


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operation on the shared array

implicit barrier synchronization

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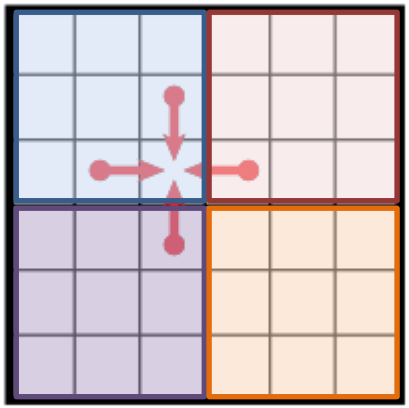


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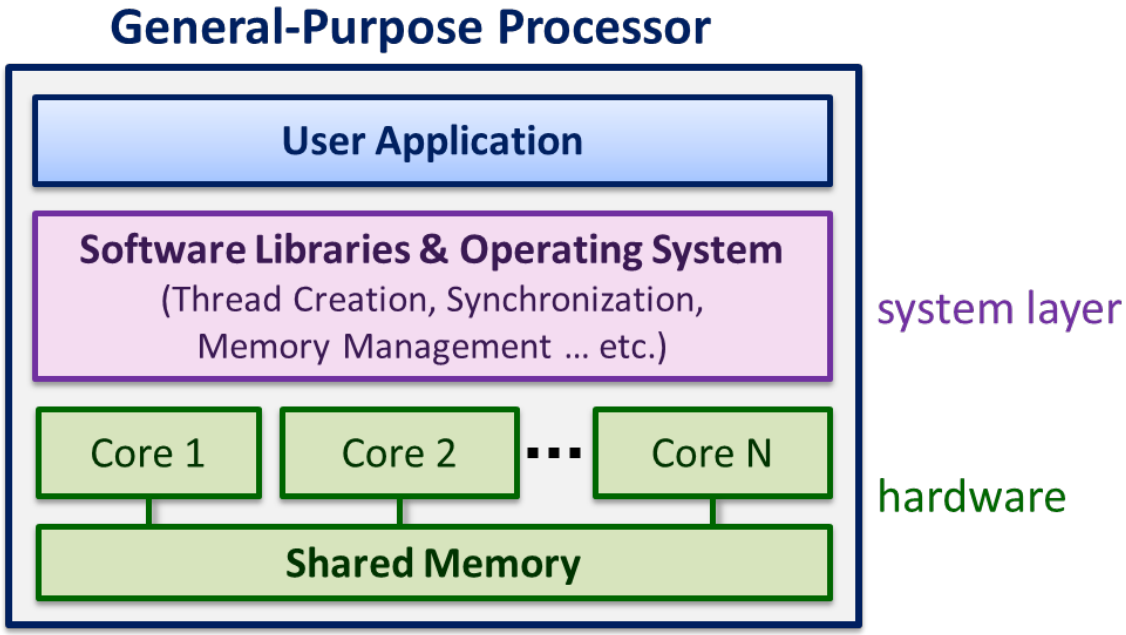

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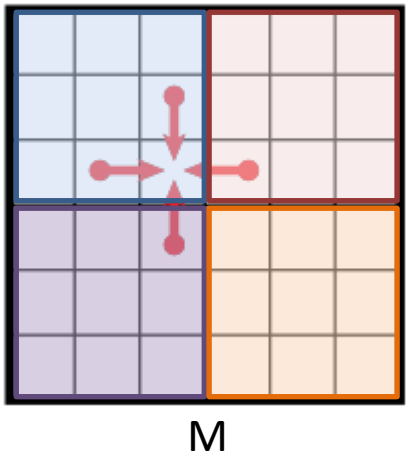
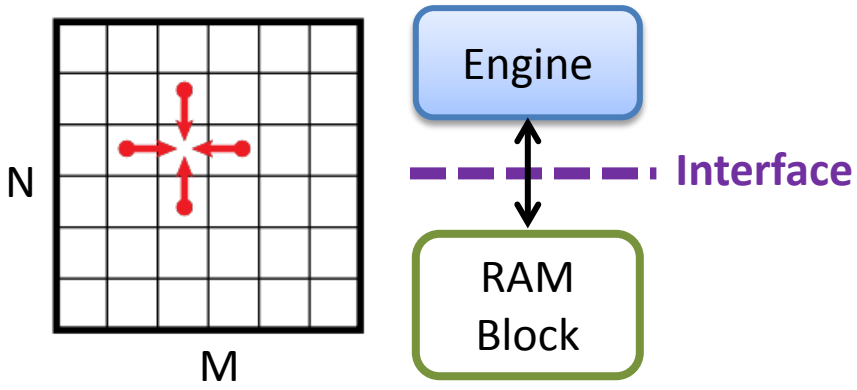


How to implement on FPGAs?

Programming on FPGA

- **2D Heat Transfer Equation (using FPGA Block RAM)**

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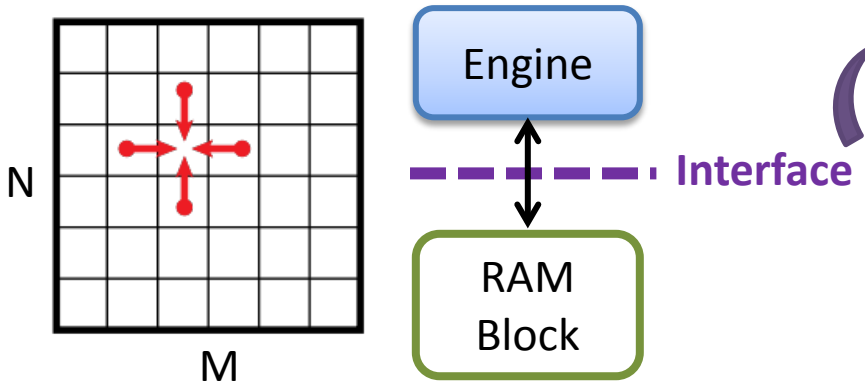


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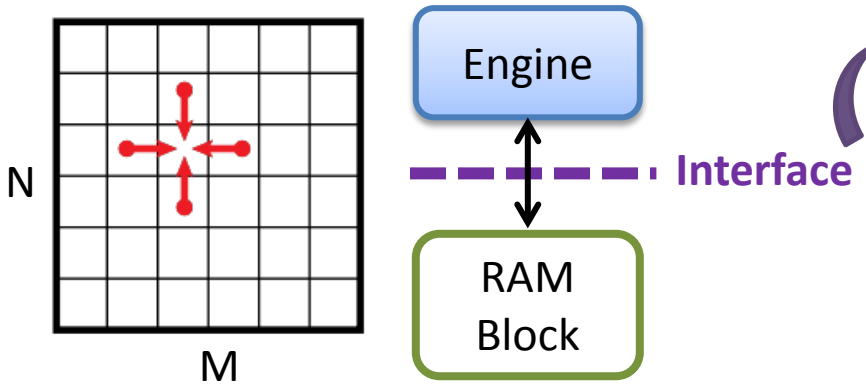


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```

```
MEM_IFC#(Bit#(5), Bit#(32)) memory <- mkBRAM();
....
memory.readReq(a1);
Bit#(32) d1 <- memory.readResp();
memory.write(a2, d2);
....
```

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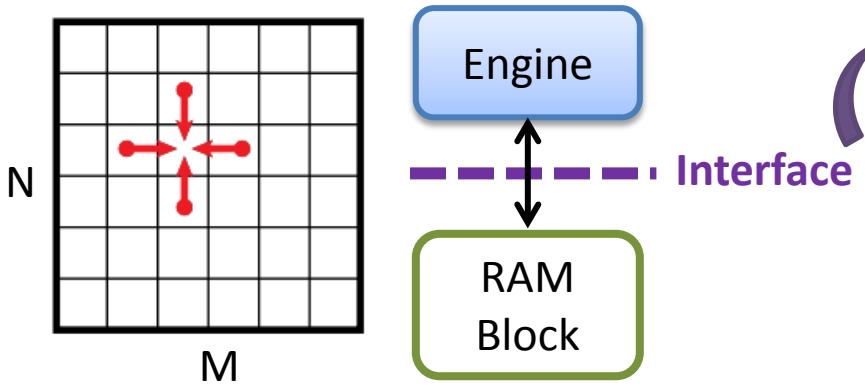


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memory.readReq(a1);
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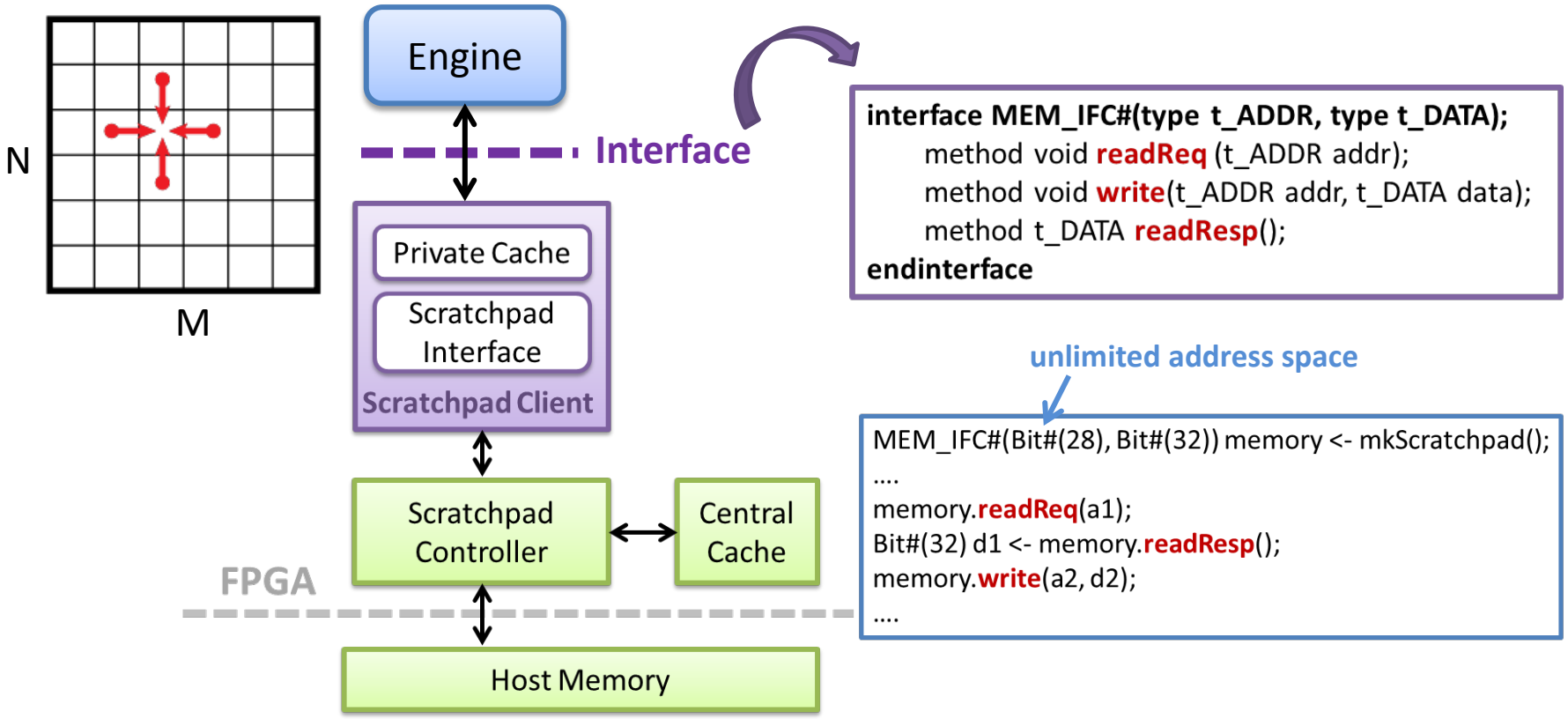
....
```

Difficulty:

- Problem size cannot fit in RAM block

Programming on FPGA

- **2D Heat Transfer Equation (using LEAP Scratchpad)**



M. Adler *et al.*, "LEAP Scratchpads," in FPGA, 2011.

Programming on FPGA

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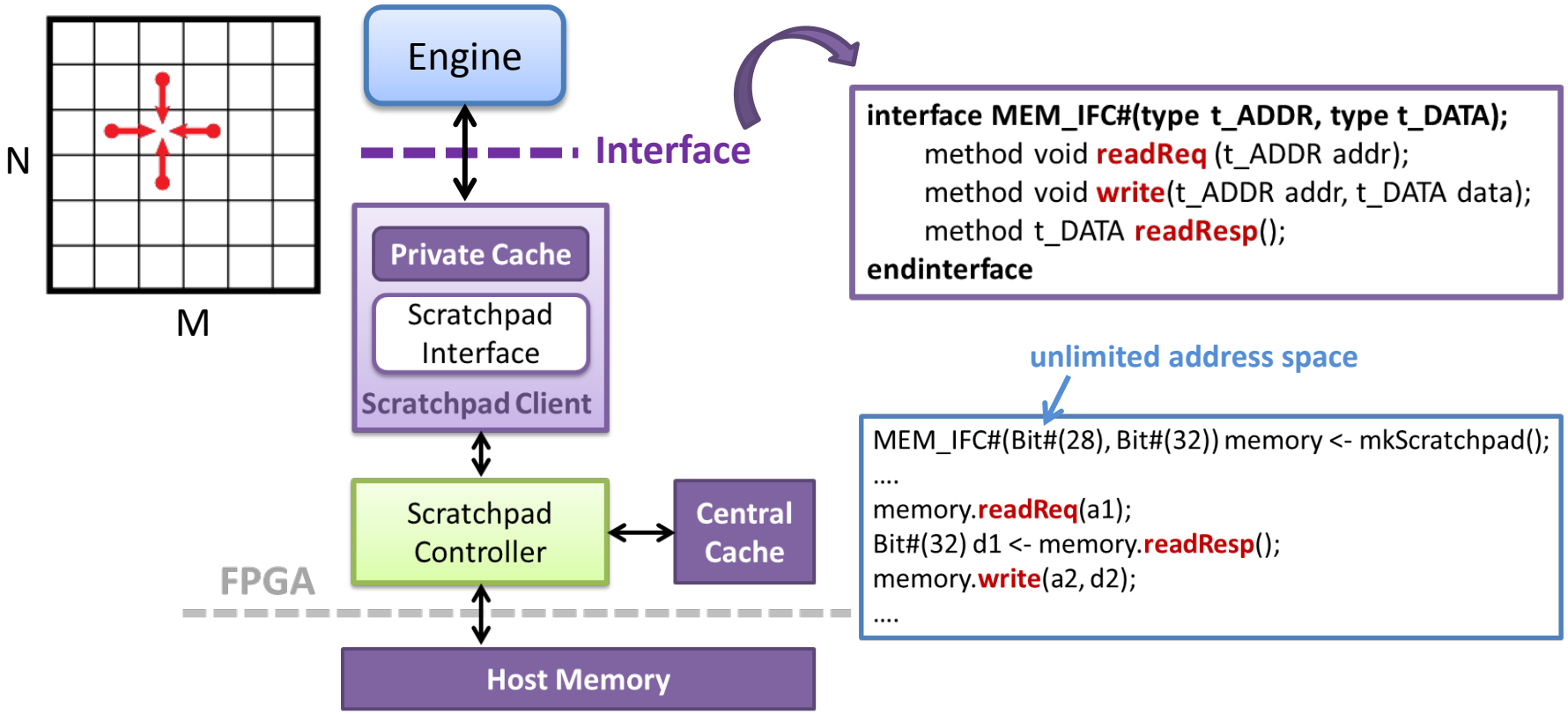

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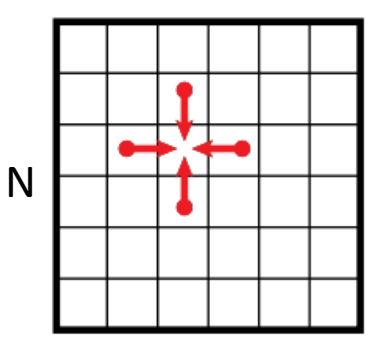
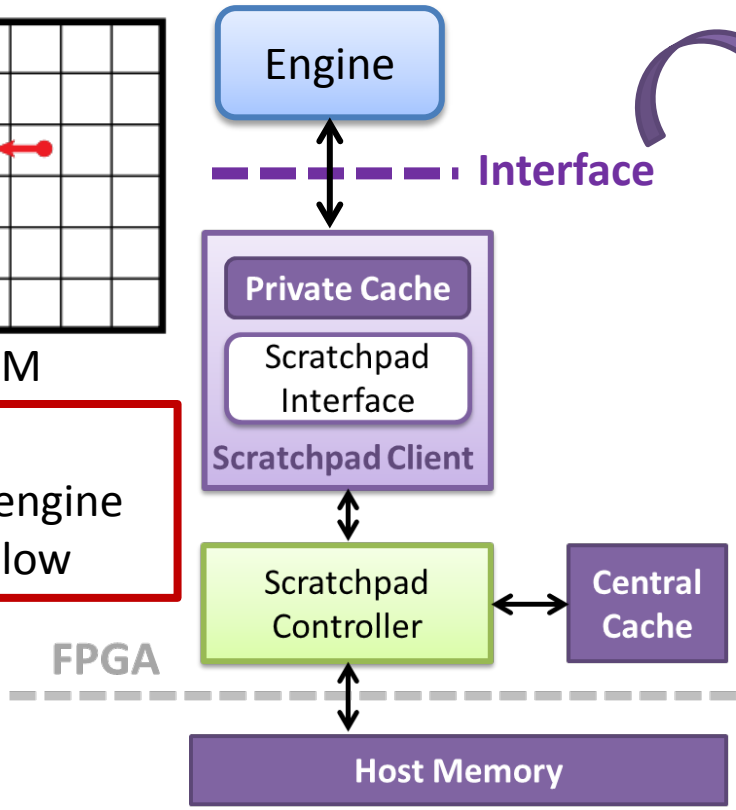


Difficulty:
- Single engine is too slow

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    method t_DATA readResp();
endinterface
```

unlimited address space

```
MEM_IFC#(Bit#(28), Bit#(32)) memory <- mkScratchpad();
....
memory.readReq(a1);
Bit#(32) d1 <- memory.readResp();
memory.write(a2, d2);
....
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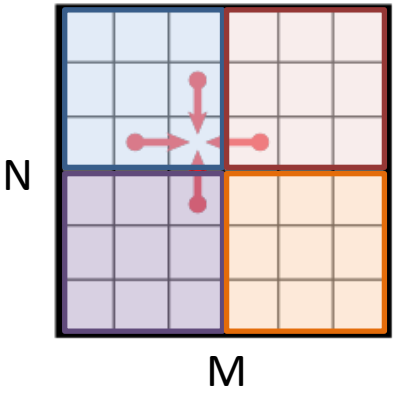
Parallel Programming on FPGA

- **2D Heat Transfer Equation**

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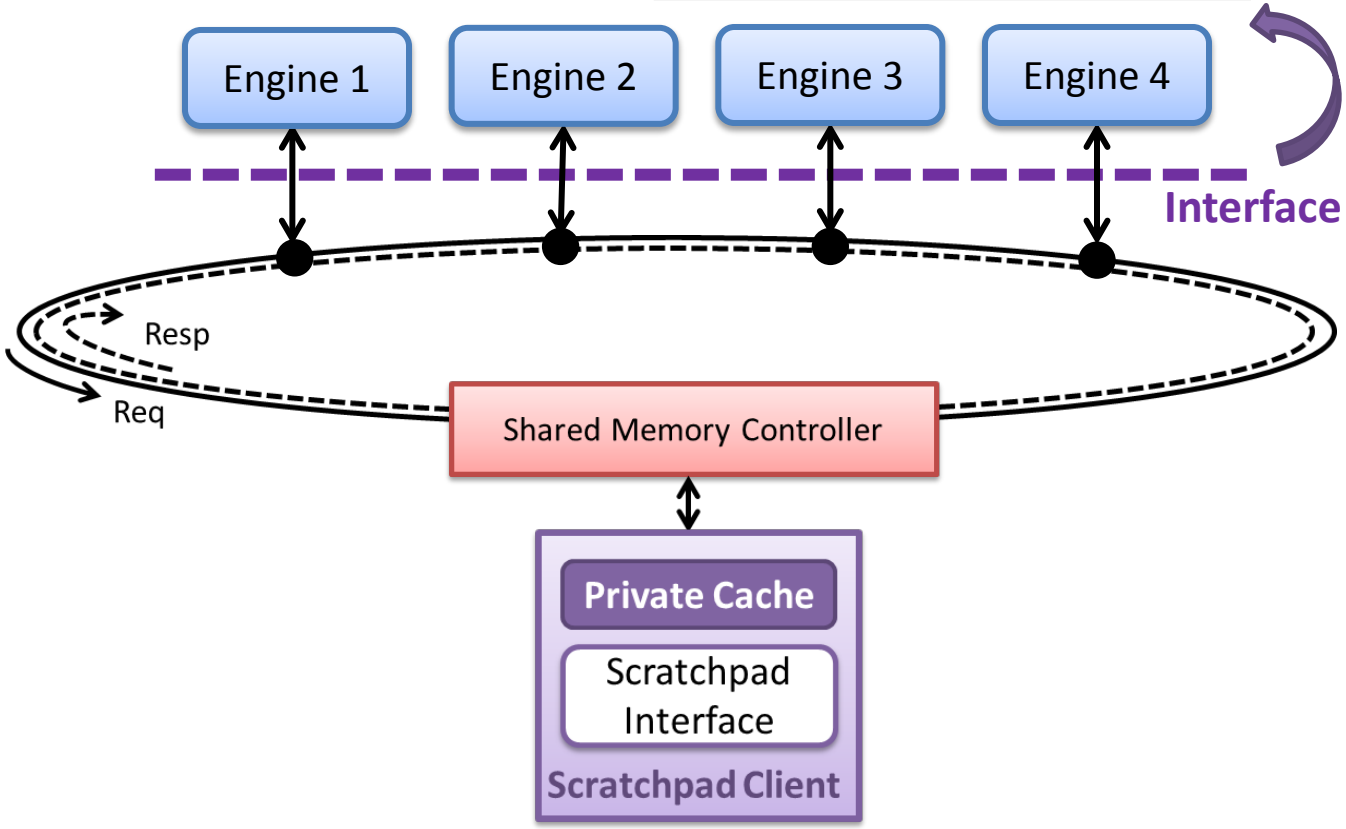

Parallel Programming on FPGA

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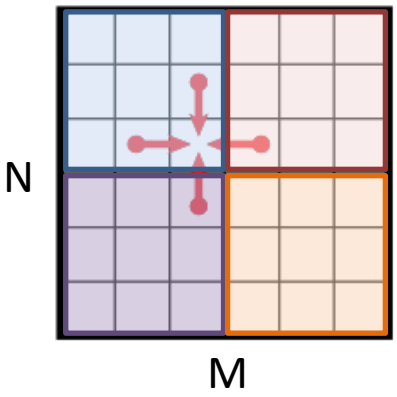


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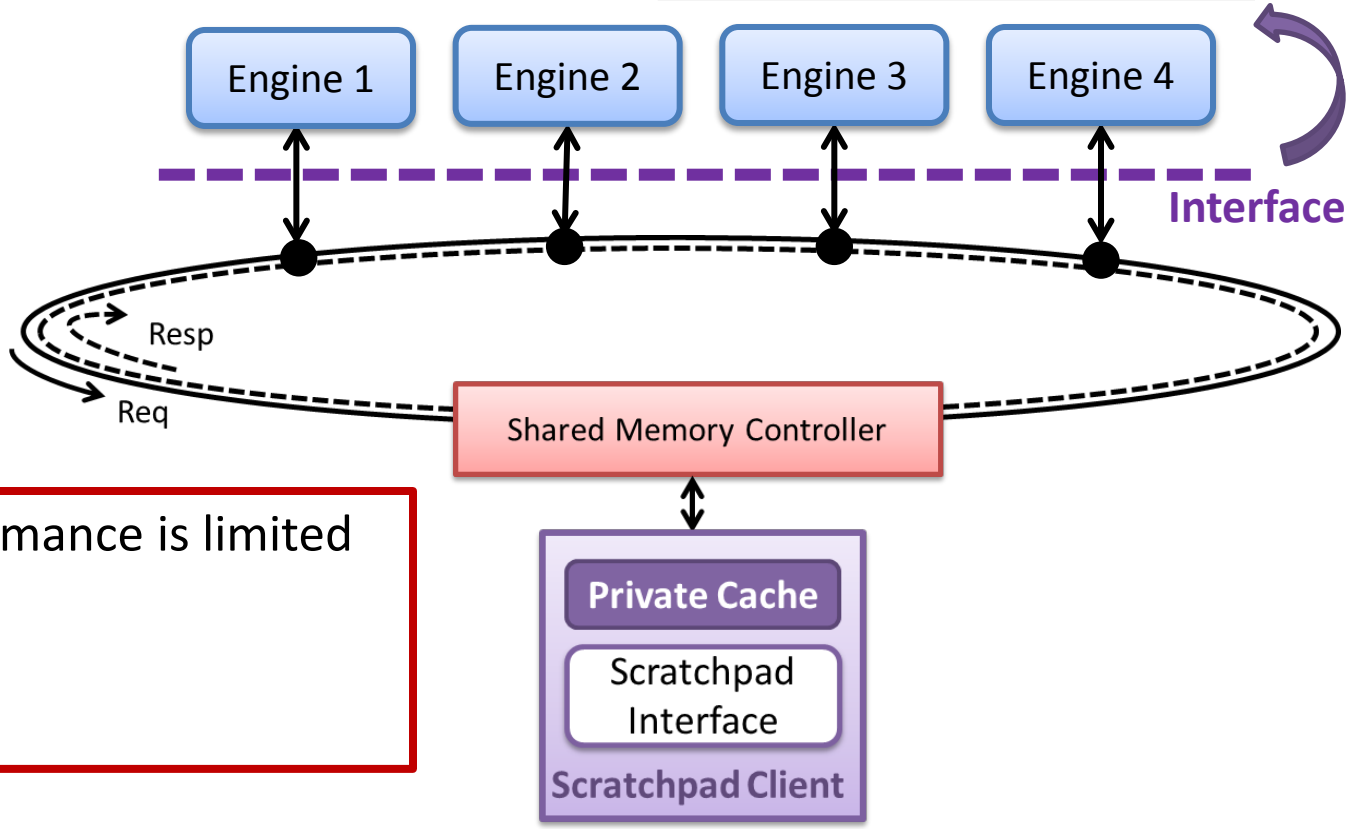

Difficulty: Performance is limited

Parallel Programming on FPGA

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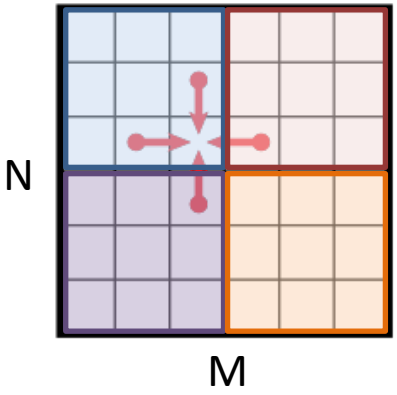


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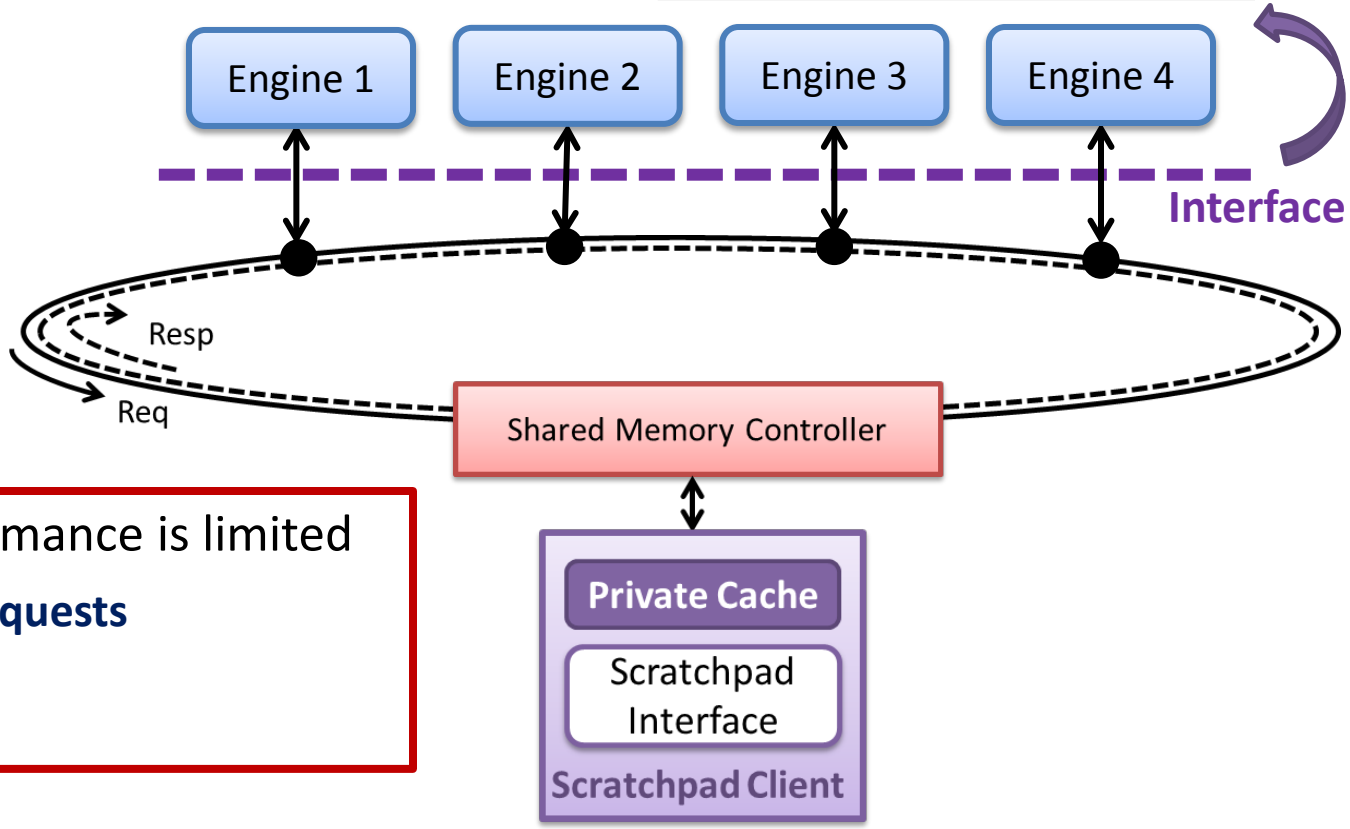

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☹ **Serialized requests**

Parallel Programming on FPGA

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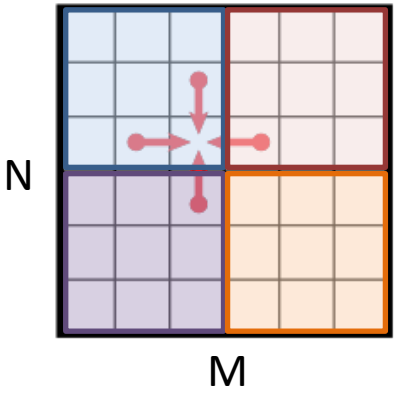


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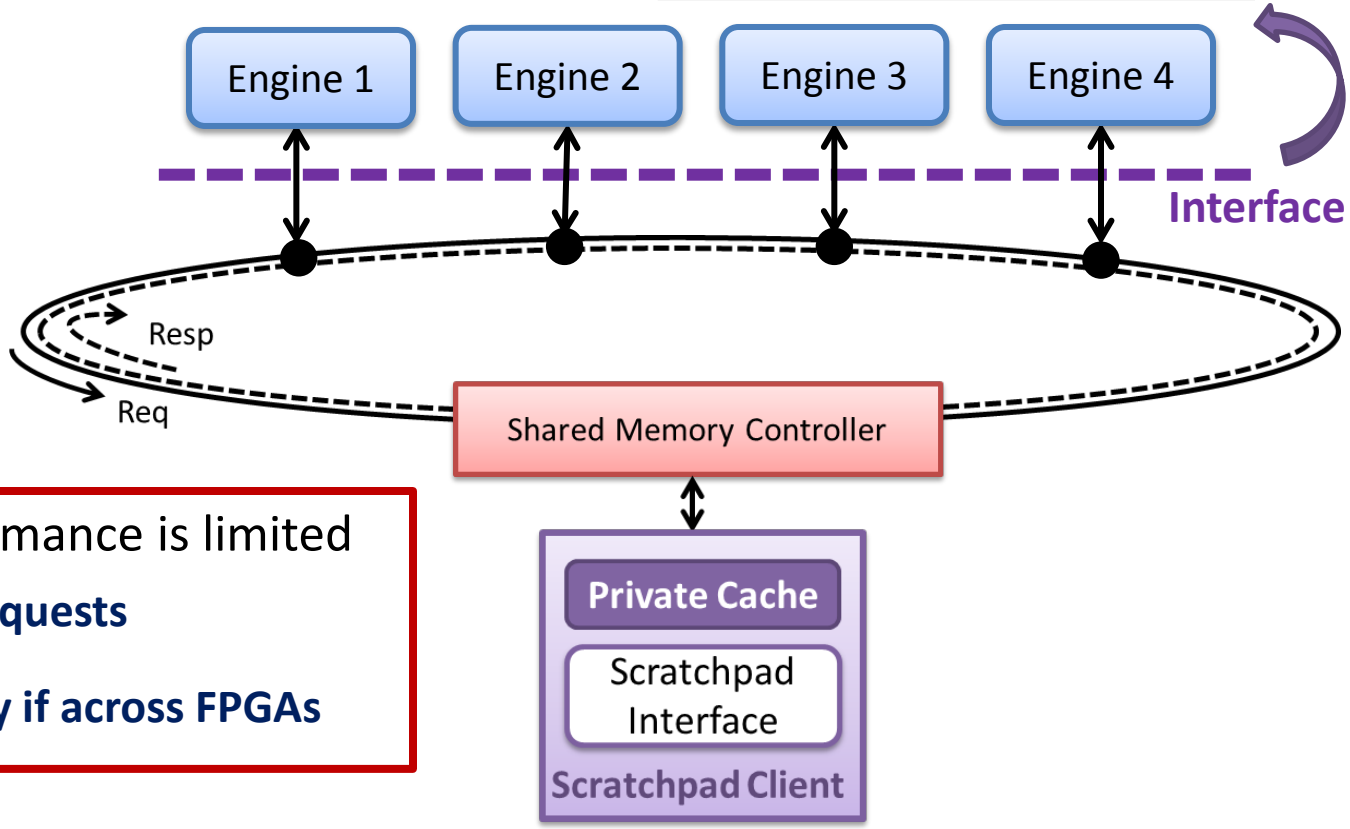
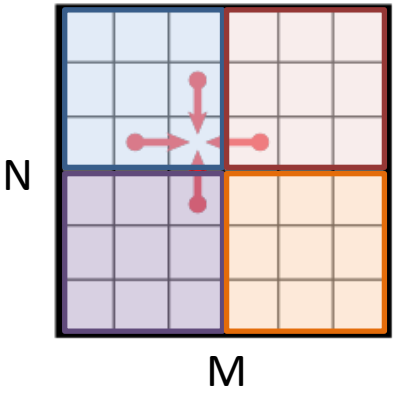


Difficulty: Performance is limited

- **Serialized requests**
- **Long latency if across FPGAs**

Parallel Programming on FPGA

- **2D Heat Transfer Equation**

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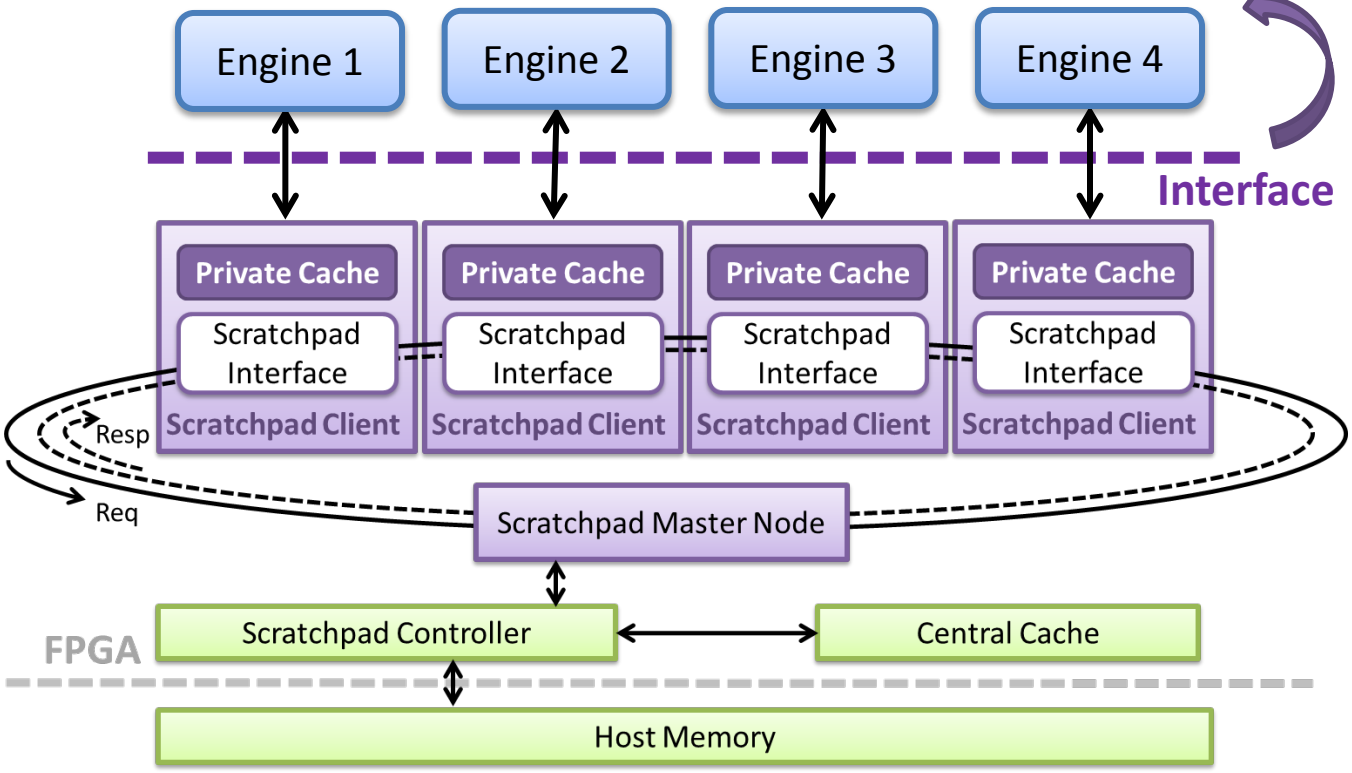

Parallel Programming on FPGA

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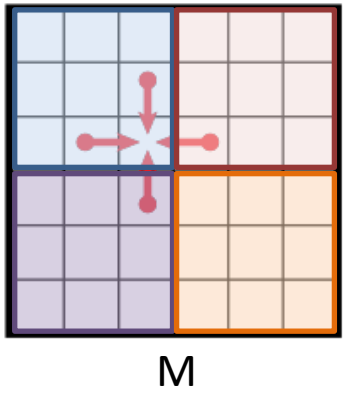

Difficulty:
- Edge pixels are shared

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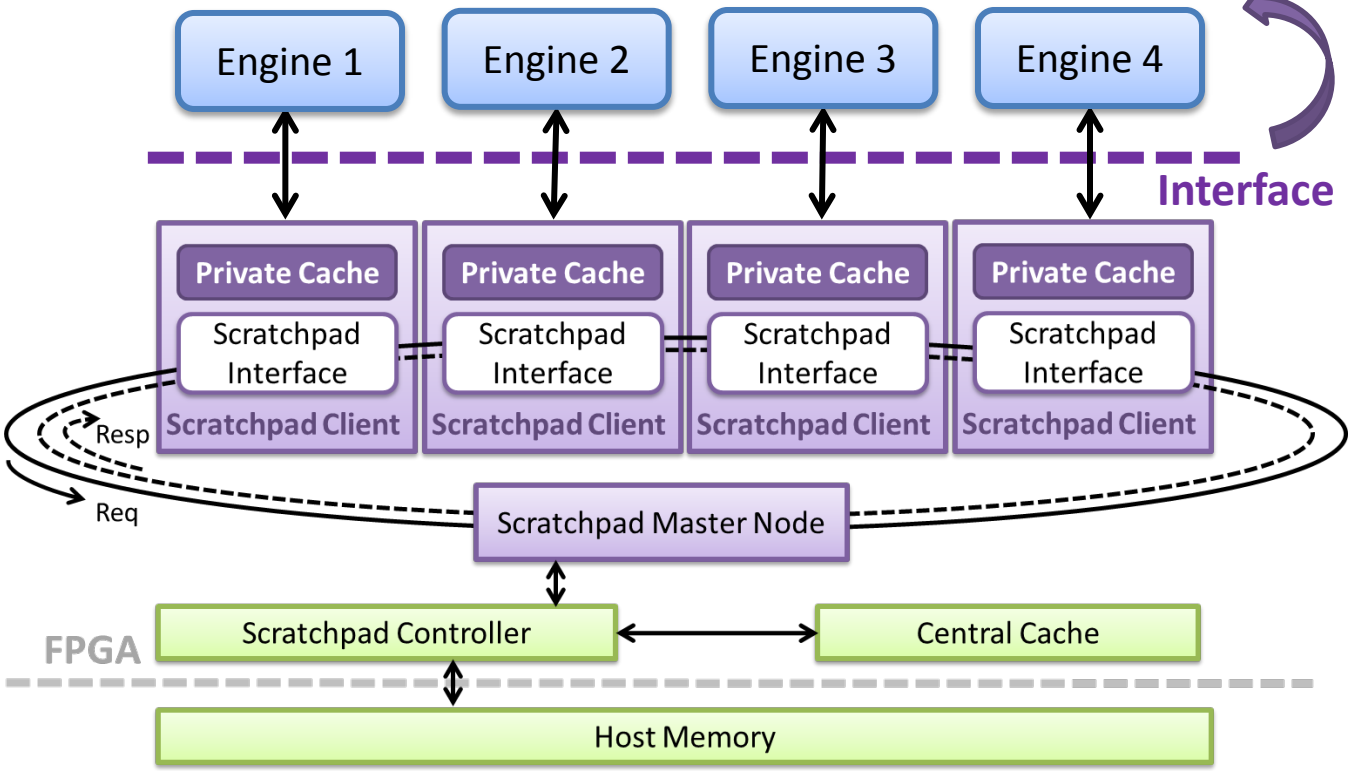

Parallel Programming on FPGA

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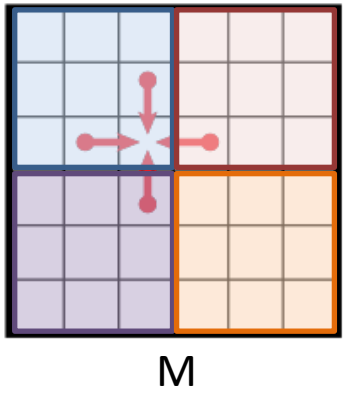


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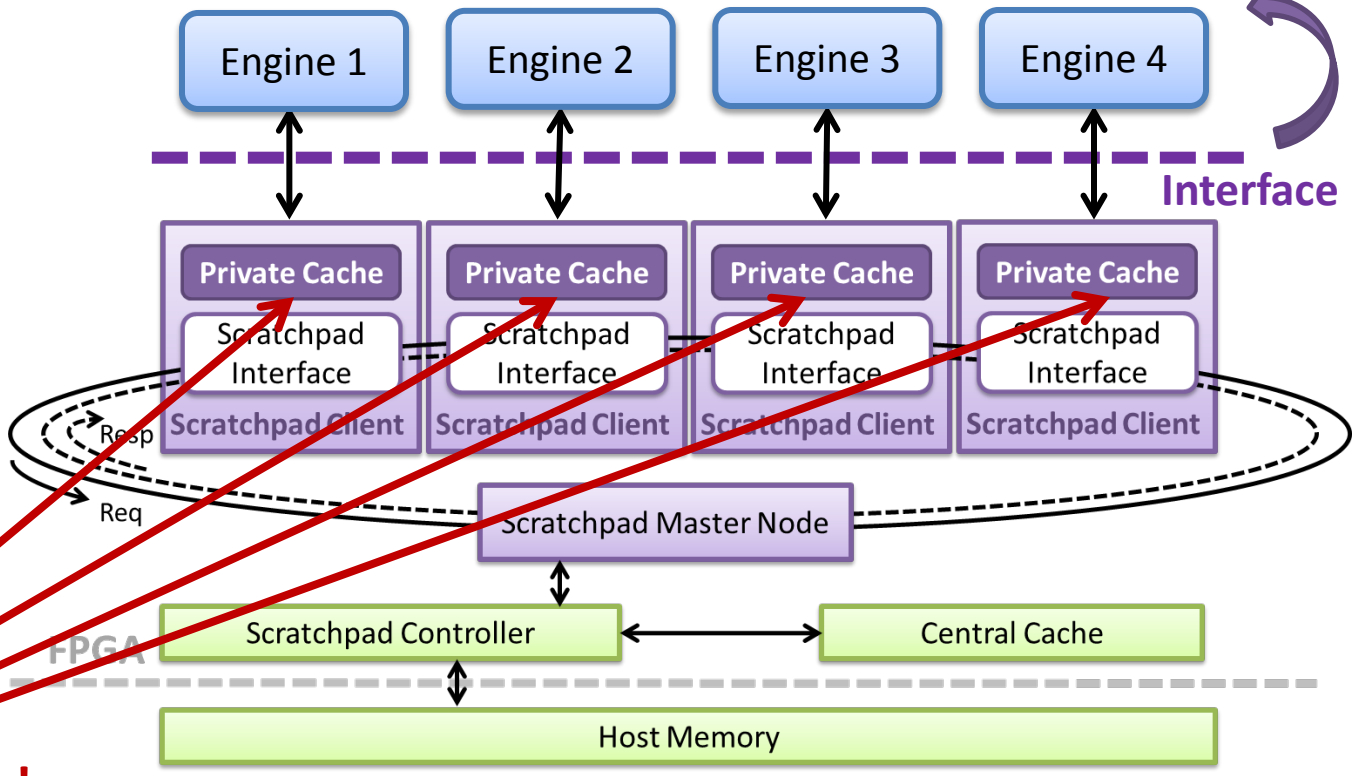
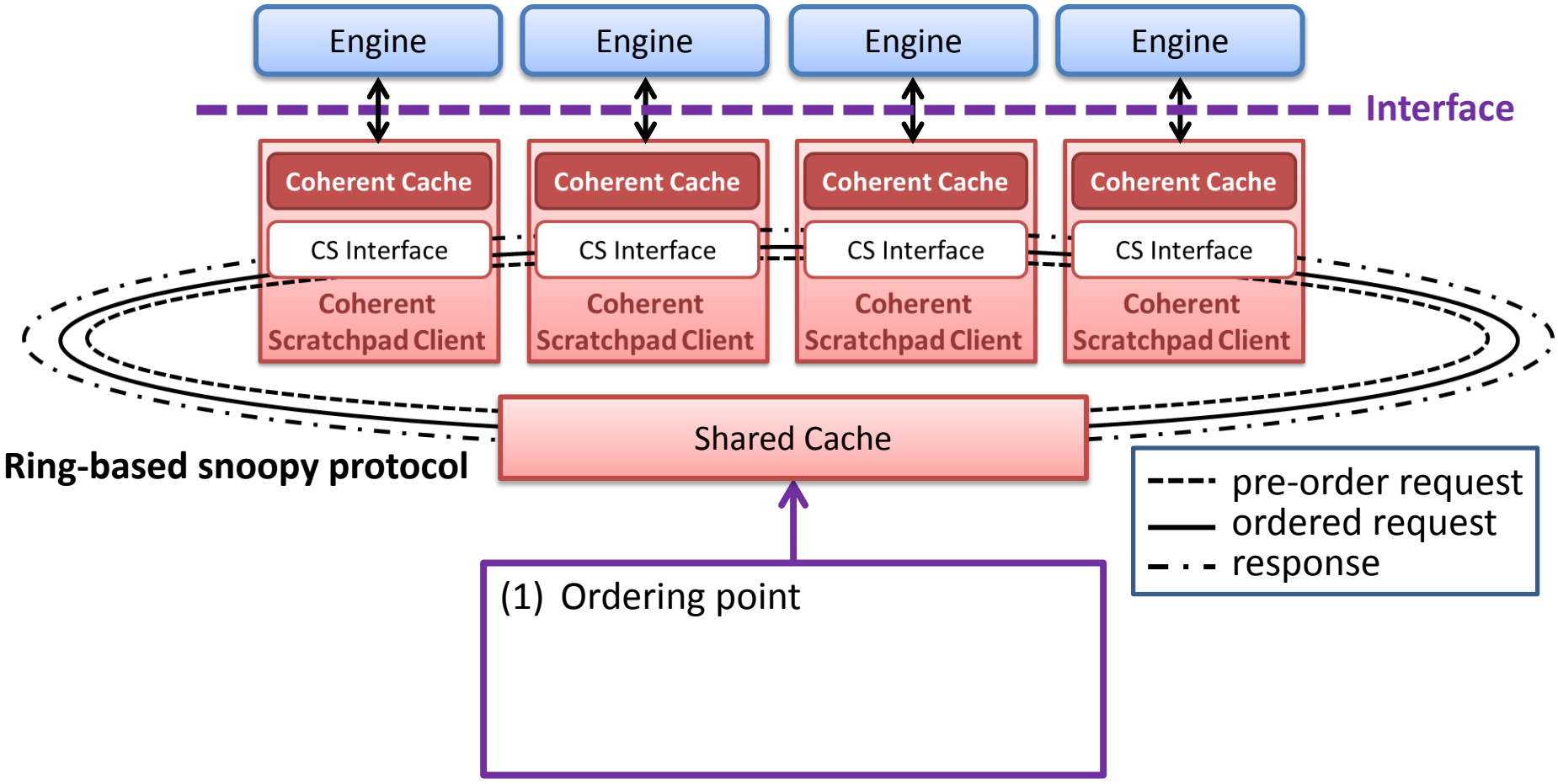


Difficulty:

- Edge pixels are shared

Need cache coherence!

Shared Memory Services: Coherent Scratchpad (CS)



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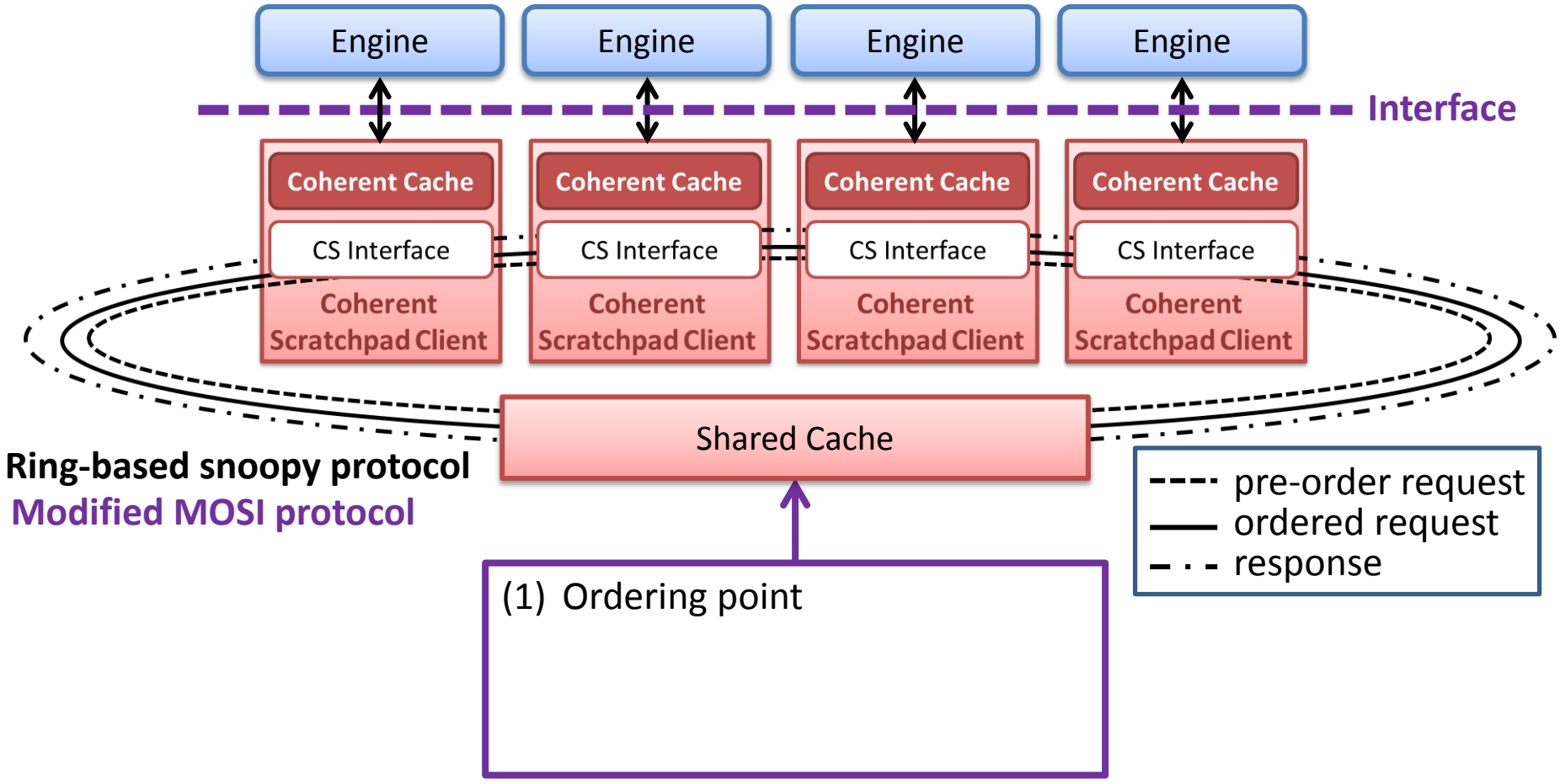

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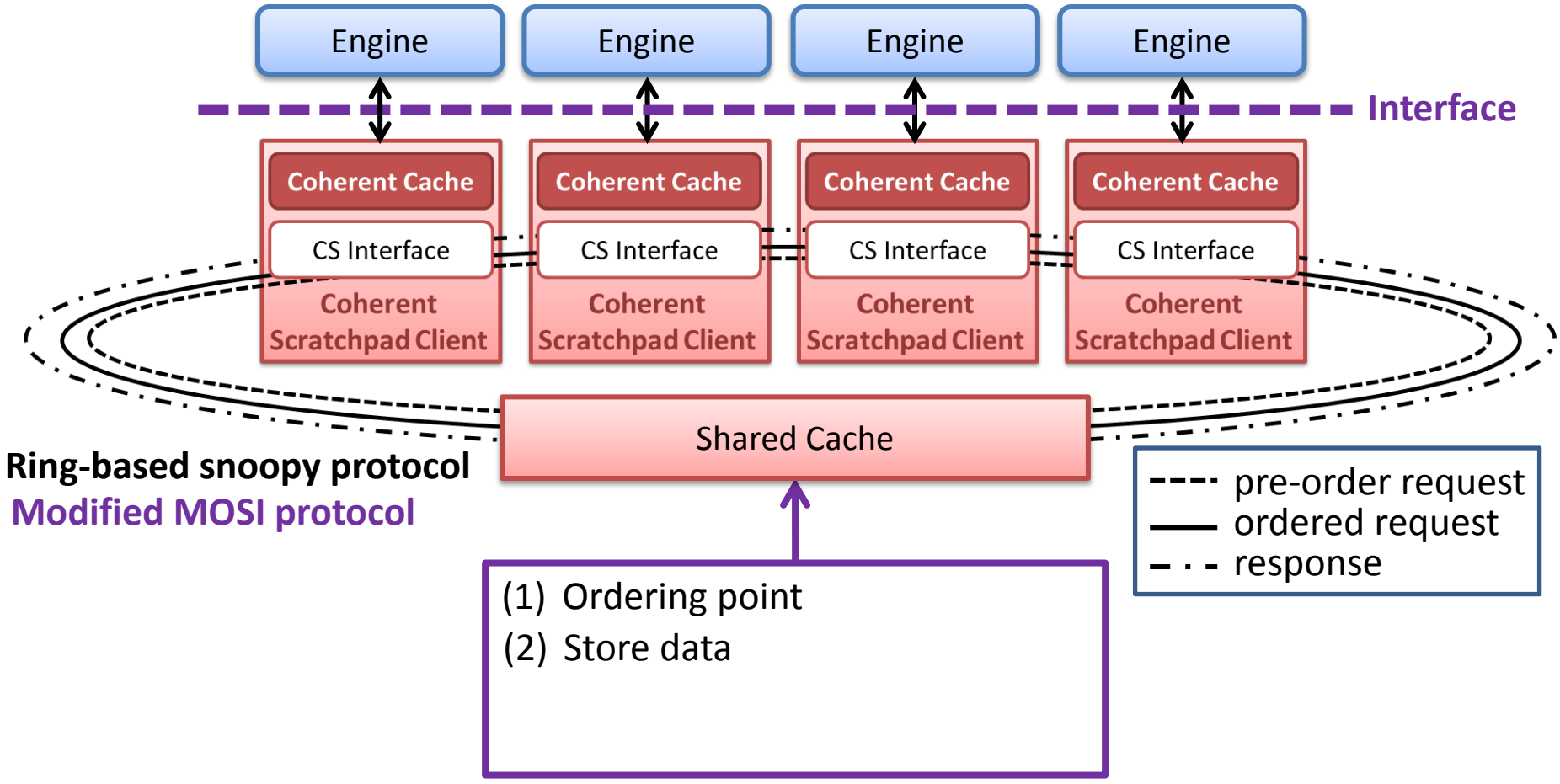

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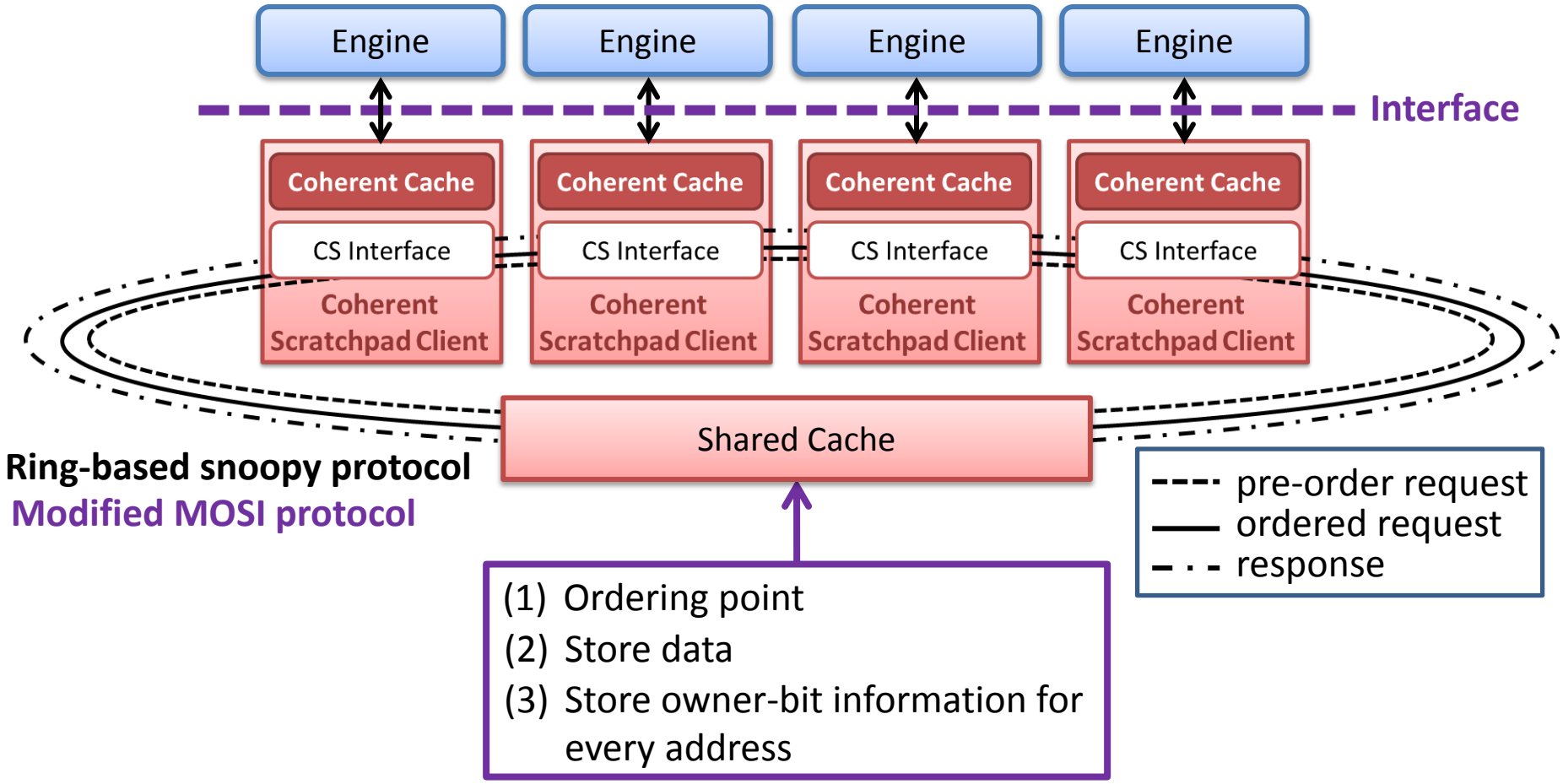

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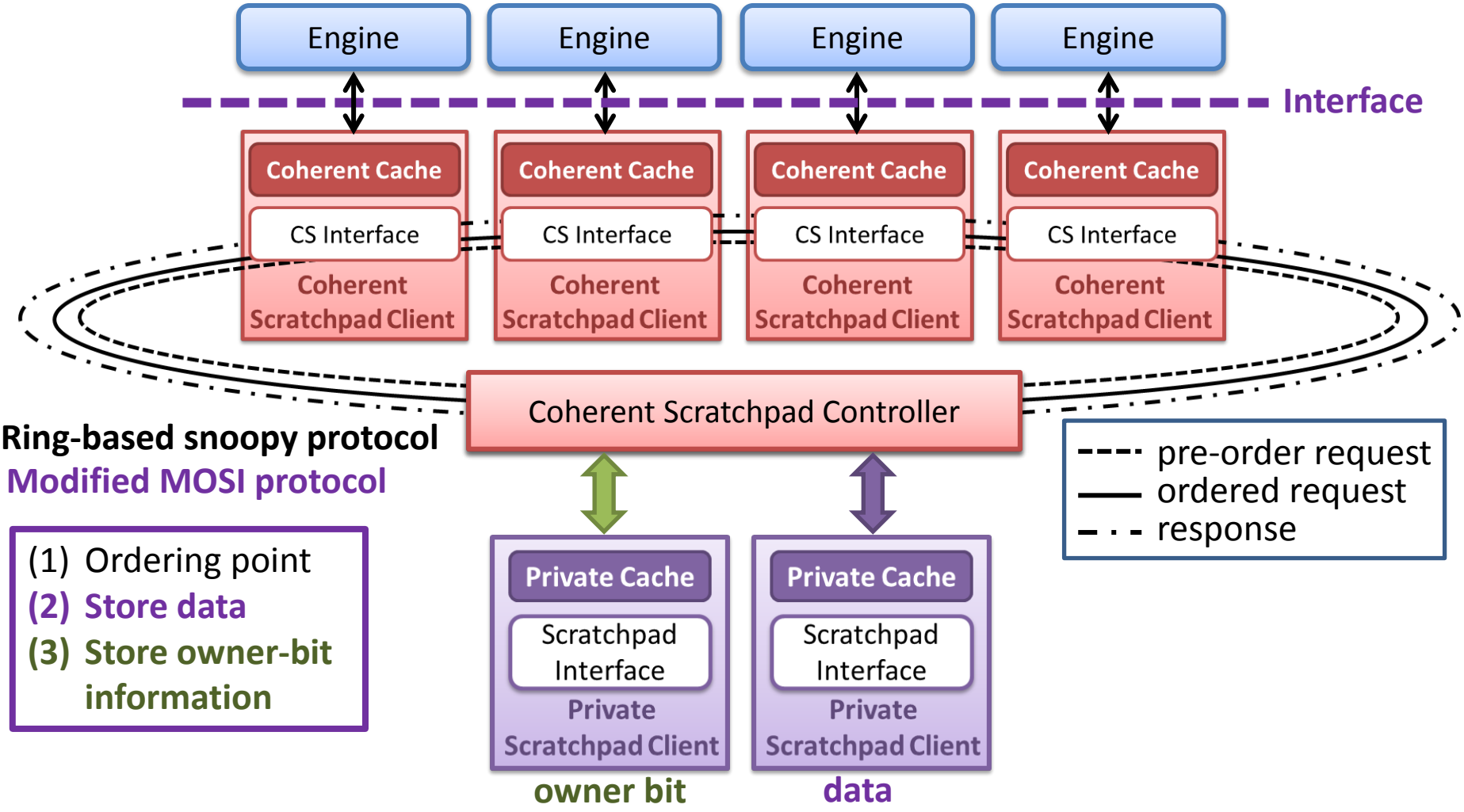

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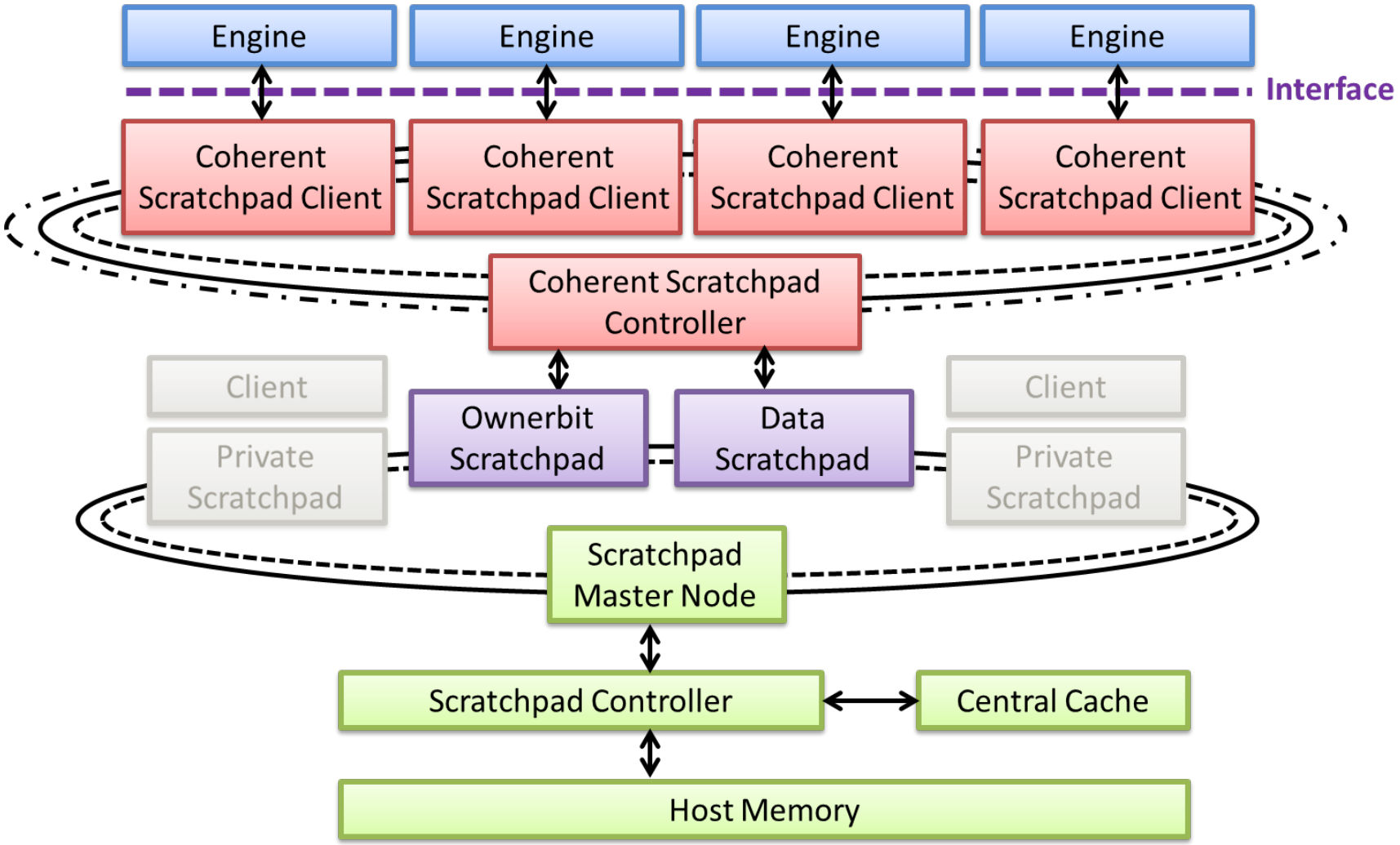

Parallel Programming on FPGA

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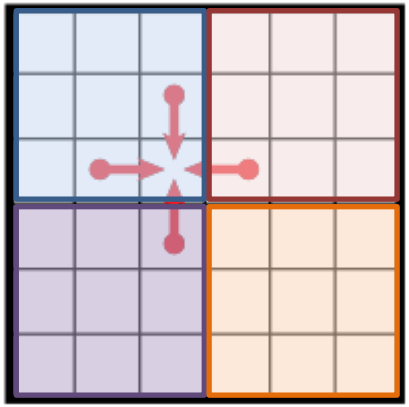


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        U[t+1,x,y] = C0*U[t,x,y]
                   + Cx*(U[t,x-1,y]+U[t,x+1,y])
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  }
}
```
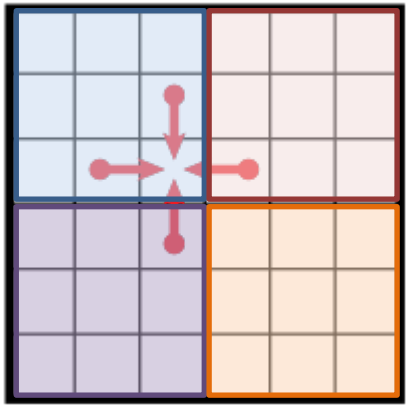

implicit barrier synchronization

Parallel Programming on FPGA

- **2D Heat Transfer Equation**

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operation on the shared array

implicit barrier synchronization

Parallel Programming on FPGA

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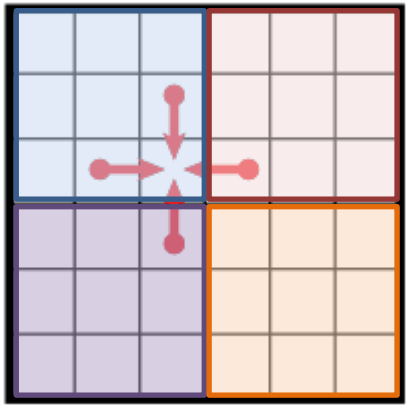


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- Finish the inner loop operations
  - ✓ Computations complete
  - ✓ Memory operations complete
- Wait until all threads are finished

Shared Memory Services: Memory Consistency

- **Block RAM/Private Scratchpad Interface**

```
interface MEM_IFC#(type t_ADDR, type t_DATA);
    method void readReq (t_ADDR addr);
    method void write(t_ADDR addr, t_DATA data);
    method t_DATA readResp();
endinterface
```

- **Coherent Scratchpad Interface**

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    method Bool requestPending(t_REQ r);
endinterface
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Shared Memory Services: Memory Consistency

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Fence support (memory consistency)

Parallel Programming on FPGA

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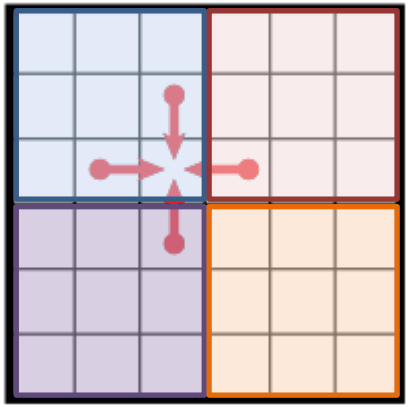


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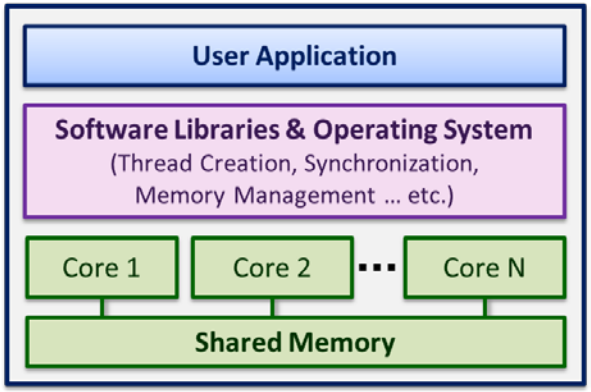
Synchronization Services: Memory Barrier

- **In Processor: software through-memory barriers**
  - via shared memory & locks




```
void barrier(num_threads_const, lock_addr, eflag_addr,
             lflag_addr, ecounter_addr, lcounter_addr)
{
    while (*eflag_addr);
    lock(lock_addr);
    (*ecounter_addr)++;
    if ((*ecounter_addr) == num_thread_const){
        (*eflag_addr) = 0;
        (*lflag_addr) = 1;
    }
    unlock(lock_addr);
    while (*lflag_addr);
    lock(lock_addr);
    (*lcounter_addr)++;
    if ((*lcounter_addr) == num_thread_const){
        (*lcounter_addr) = 0;
        (*ecounter_addr) = 0;
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    unlock(lock_addr);
}
```

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Synchronization Services: Memory Barrier

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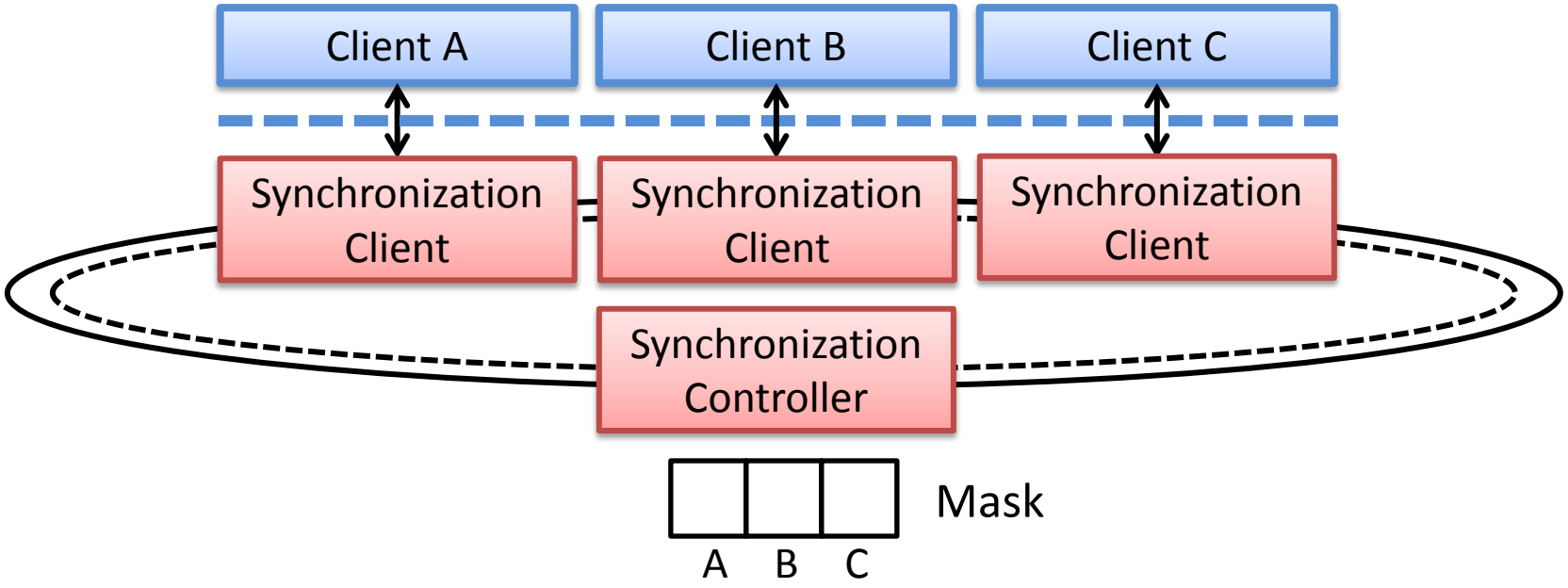
Suppose clients A & B need to synchronize



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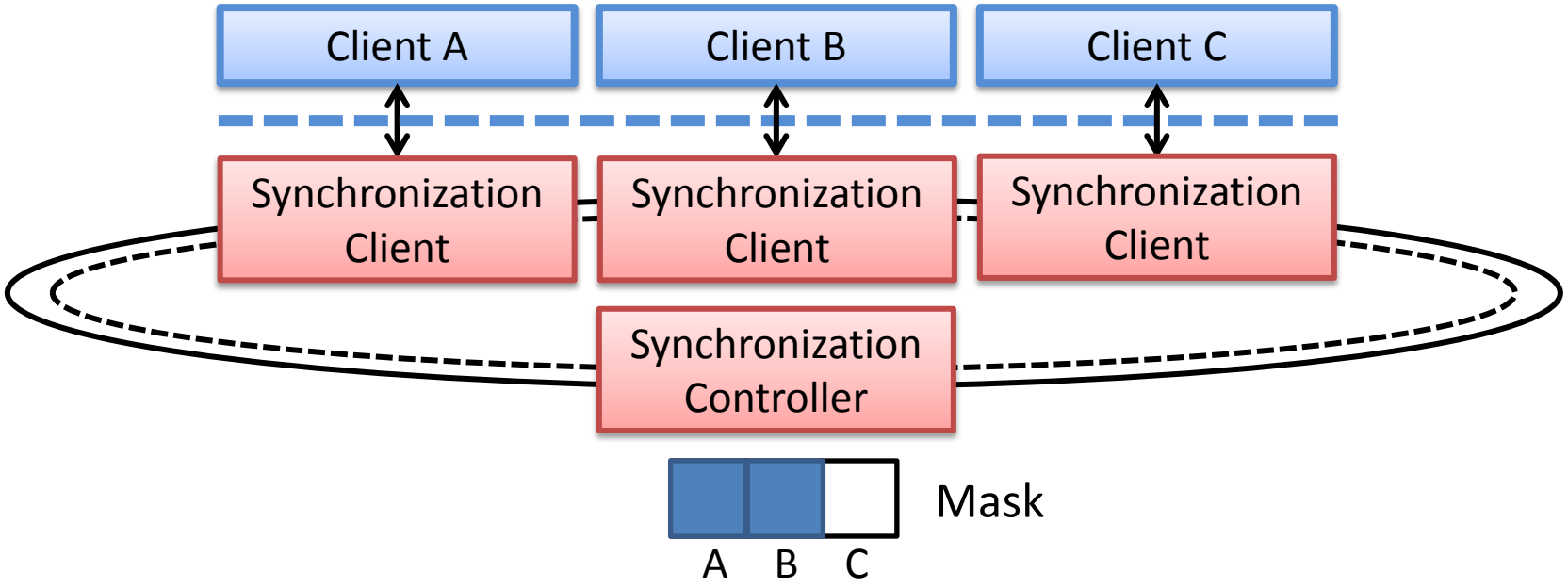

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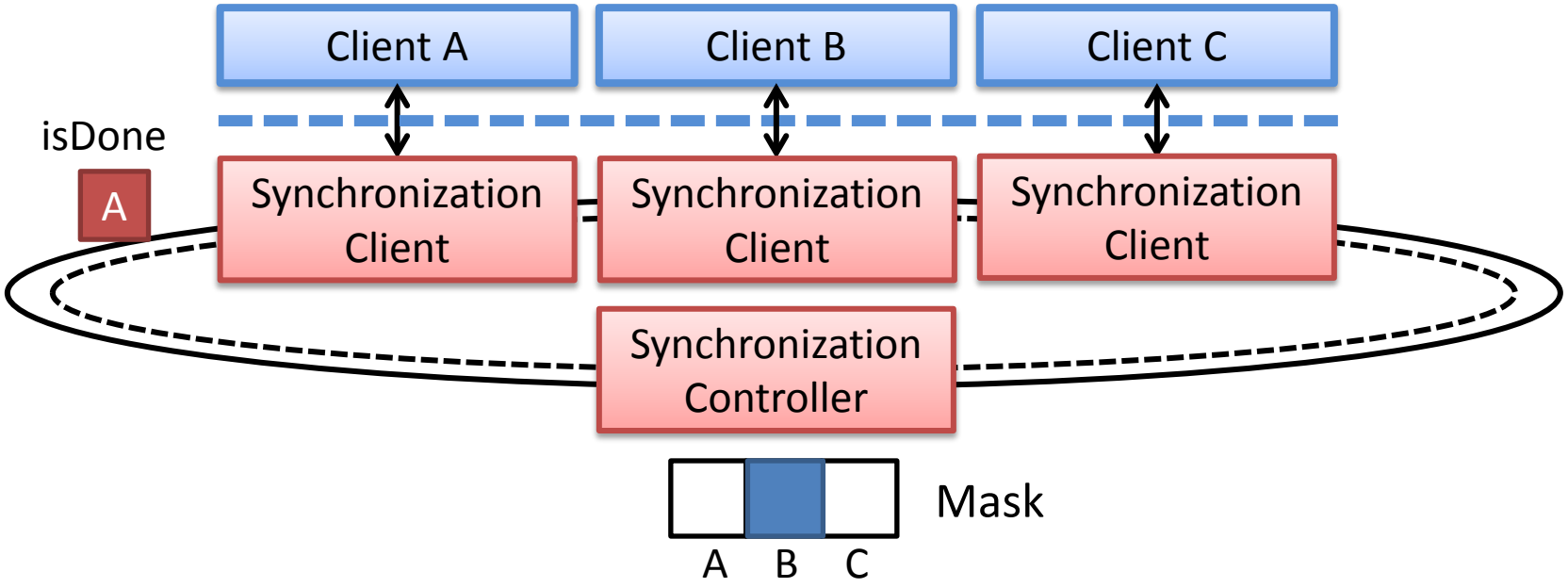

Synchronization Services: Memory Barrier

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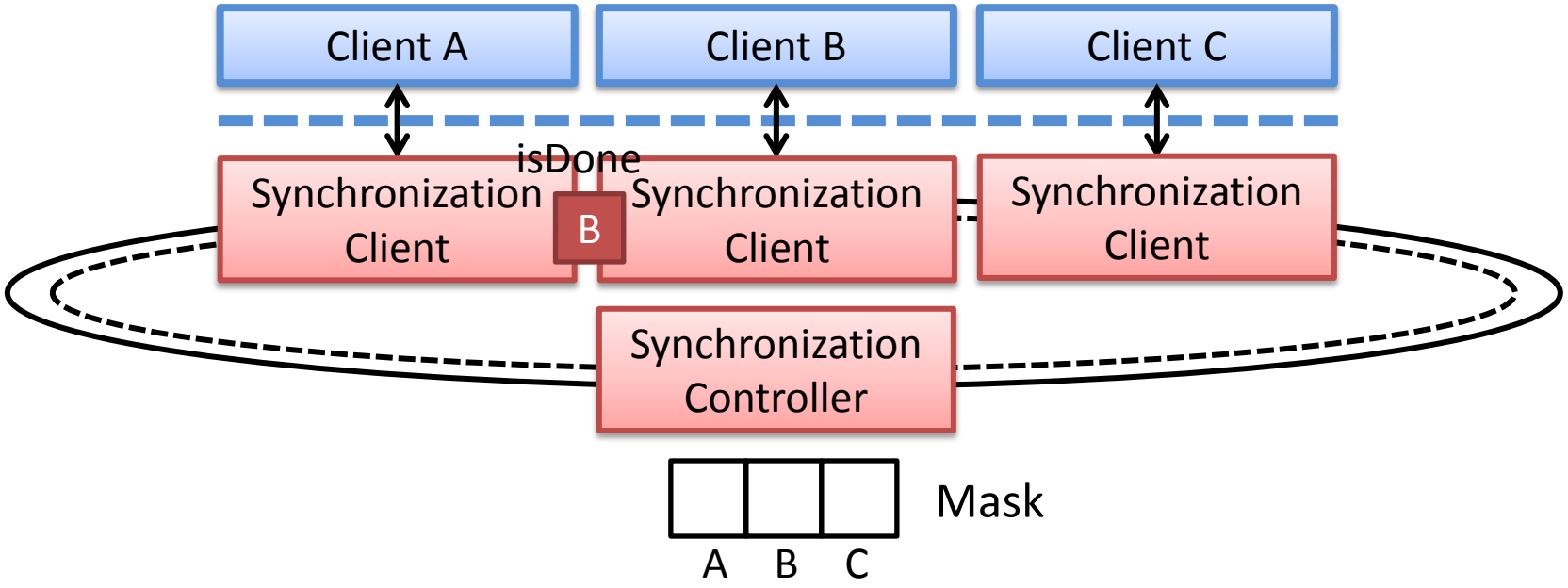

Synchronization Services: Memory Barrier

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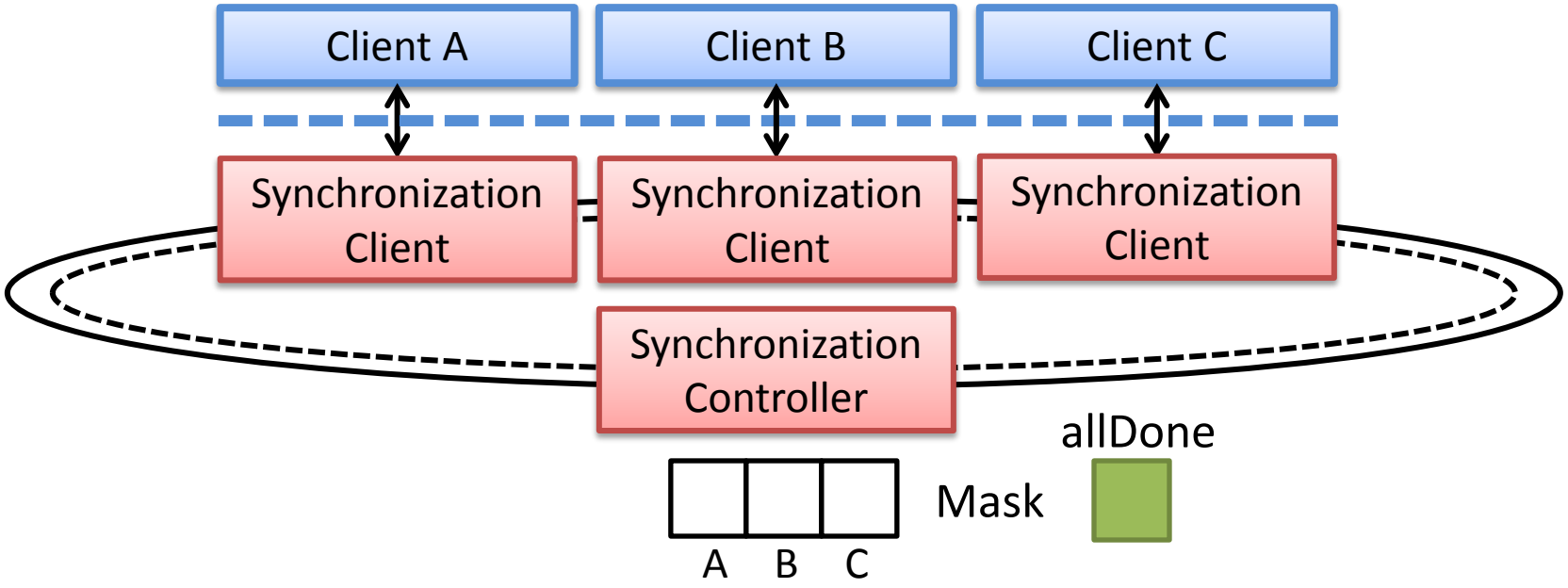
Suppose clients A & B need to synchronize

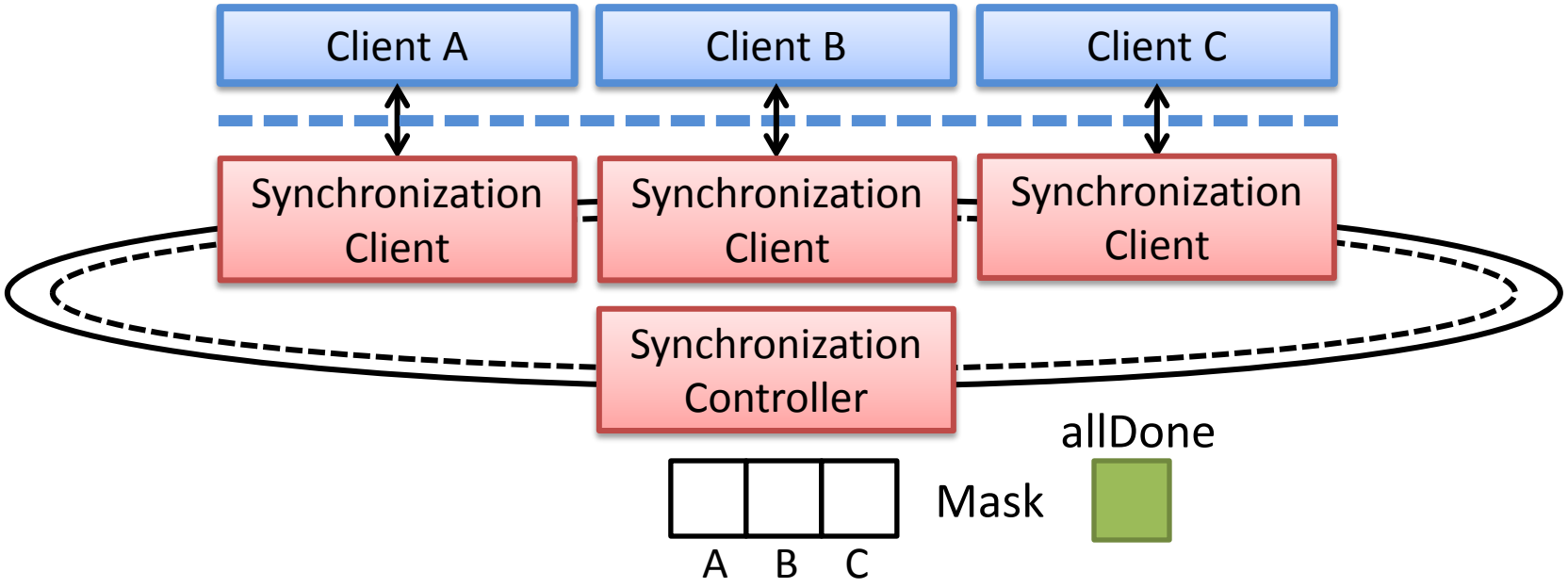


Synchronization Services: Memory Barrier

- **In Processor: software through-memory barriers**
  - via shared memory & locks
- **In FPGA:**

```
void barrier()
{
  send(isDone);
  while (receive(allDone));
}
```

Suppose clients A & B need to synchronize



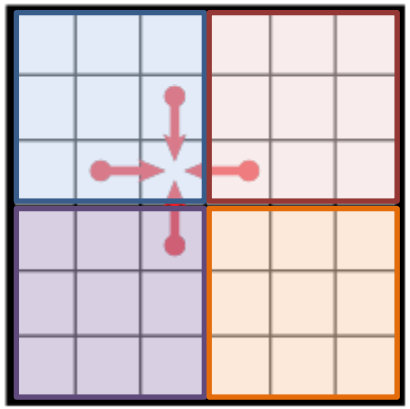
Synchronization Services: Memory Barrier

- **In Processor: software through-memory barriers**
  - via shared memory & locks
- **In FPGA:**
  - outside of shared memory
- **Performance Comparison:**

System	Barriers per Second	Normalized Throughput
LEAP Barrier Service	7352076	342
Hardware Lock Barrier via Coherent Scratchpad	85088	4
Spin-Lock Mutex-Enabled Cache*	21510	1

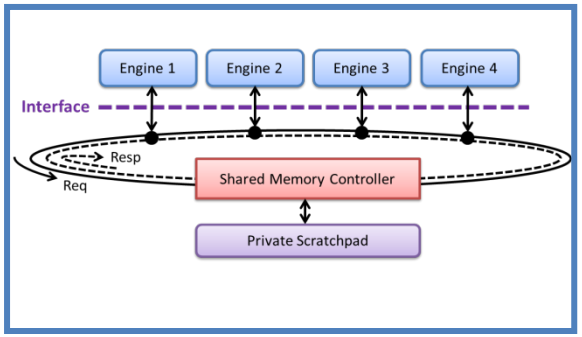
* V. Mirian and P. Chow, "Managing mutex variables in a cache-coherent shared-memory system for FPGAs," in *FPT*, 2012.

Performance on 2D Heat Transfer

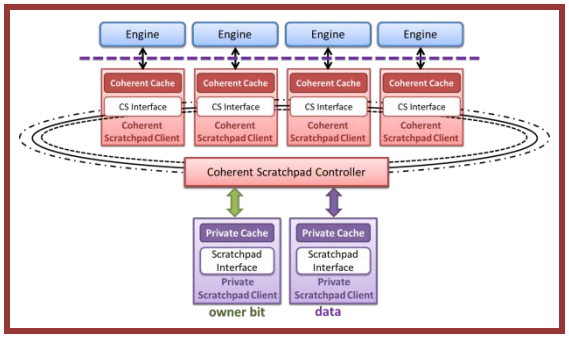


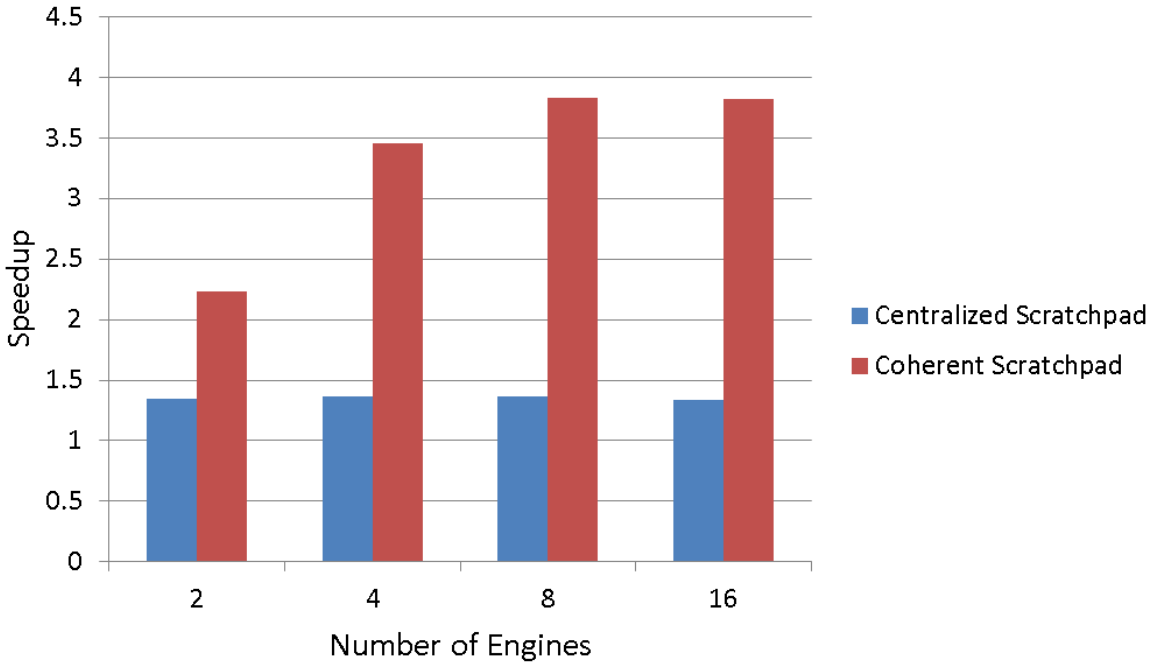
FPGA: Xilinx VC707
Frame Size: 512x512
Coherent Cache Size: 8KB
Pixel Size: 8bit

Centralized Scratchpad

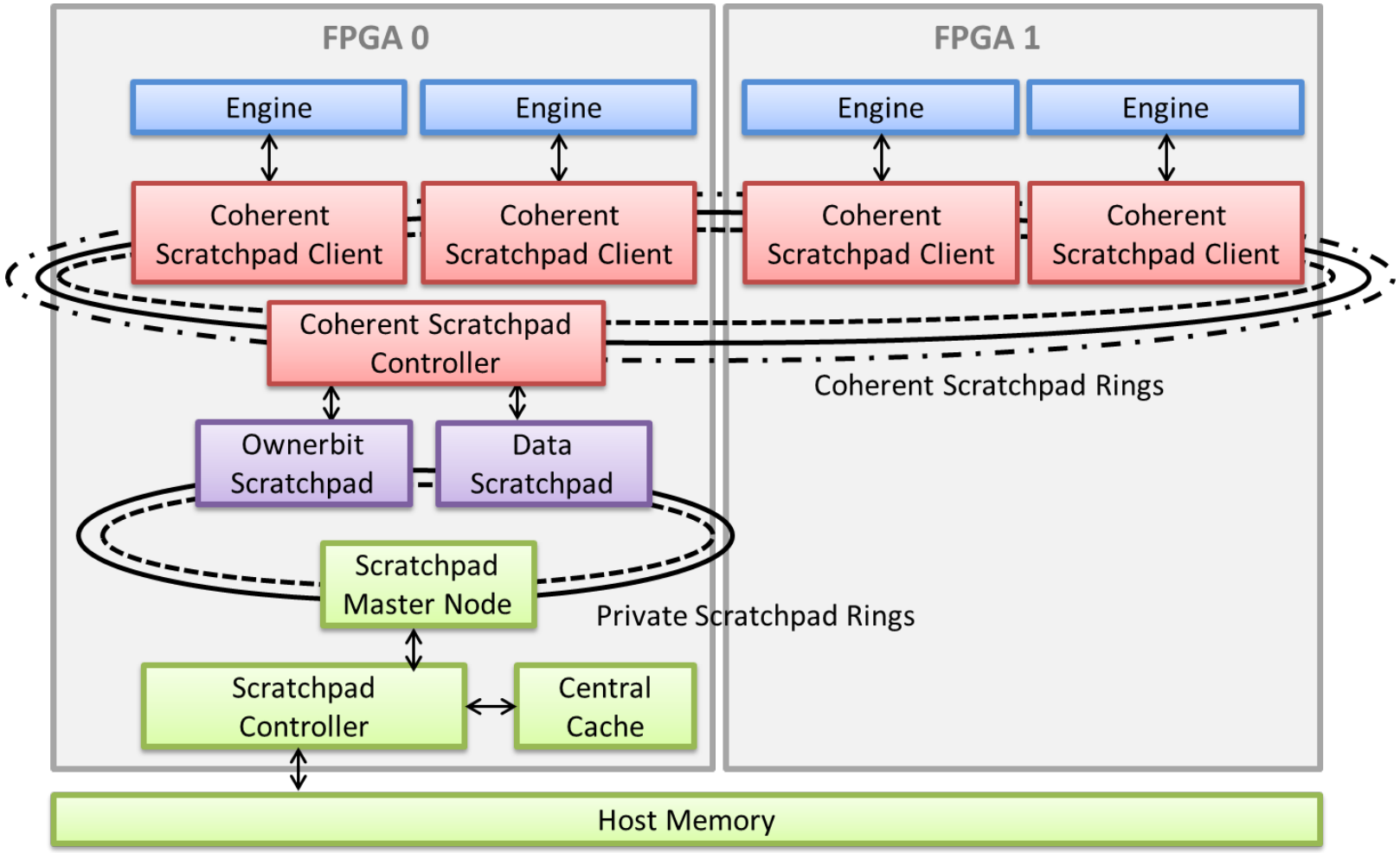


Coherent Scratchpad





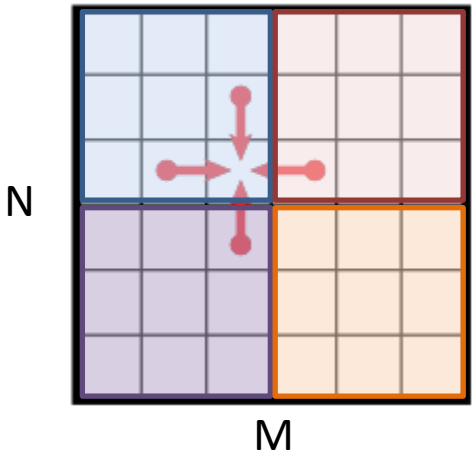
Coherent Scratchpads on Multiple FPGAs



K. Fleming *et al.*, "Leveraging latency-insensitivity to ease multiple FPGA design," in FPGA, 2012.

Performance of Dual FPGA

- **2D Heat Transfer Equation**



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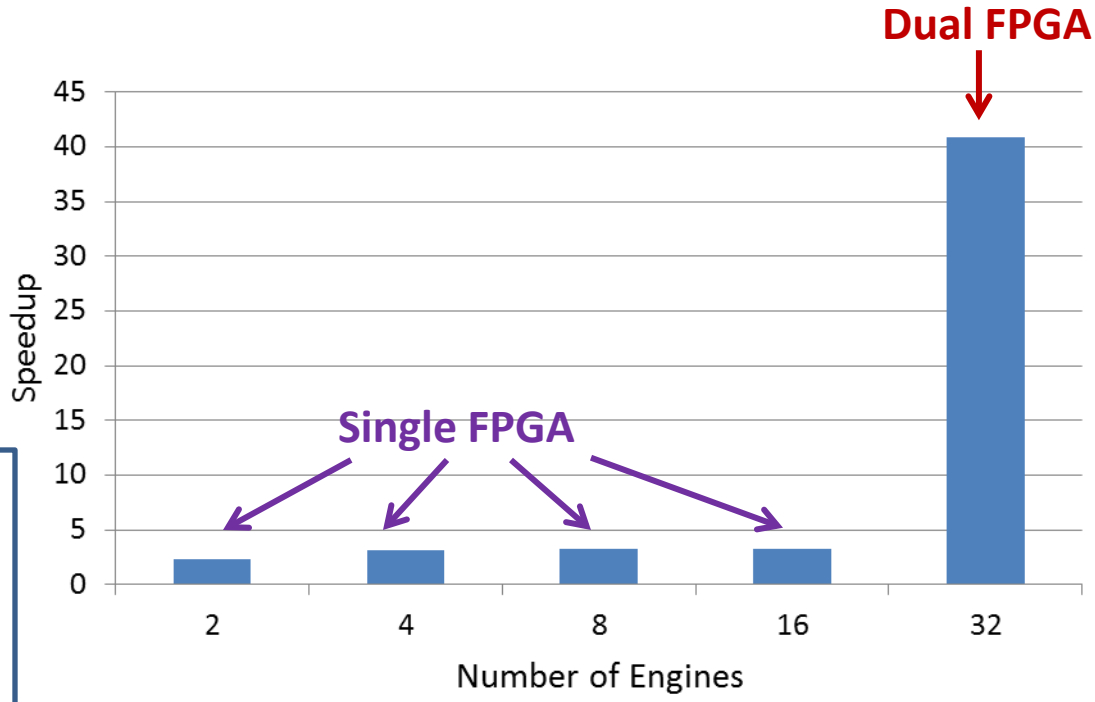

Conclusion

- Programming on FPGA is difficult due to the lack of useful abstractions
- We provide a set of FPGA-based shared memory primitives:
  - Coherent scratchpads: manage multiple coherent caches
  - Synchronization primitives
- We improve programming efficiency
  - Common interface:
    Block RAM -> multi-FPGA coherent memory
  - It took only a few hours to write the 2D heat transfer equation

Thank You