ASIC SA-27E Databook, Part II
Macros

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Revision History

Date	Page	Description
6/4/2001	31–42	Added "Compilable Extended Voltage Register Arrays"
6/4/2001	145	Updated "Valid SRAM1R Configurations" table
4/2/2001	160	Updated SRAM1RN usage restrictions
4/2/2001	170	Updated BIST1RN usage restrictions
4/2/2001	183, 205	Updated SRAM2B and SRAM4G "Address Collisions"
3/1/2001	146	Updated SRAM1R "Usage Limitations"
3/1/2001	165, 167	Updated BIST1R "Usage Requirements", and pin definitions
3/1/2001	206, 207	Updated large SRAM4G delay definitions, added small SRAM4G delay definitions
3/1/2001	216	Updated BIST4G scan latches and clock cycles
3/1/2001	279–322	Updated Phase-Locked Loop (miscellaneous changes throughout)
01/29/2001	n/a	Deleted SRAM1LR (has been removed from menu)
01/29/2001	229, 242	Updated ROMEH/ROMLH and ROMEP/ROMLP personality file format
01/10/2001	209, 210	Updated SRAM4G footprint and “SRAM4G Access Time, Internal Capacitance, and Physical Area Examples”
01/10/2001	223, 236	Updated ROMEH/ROMLH and ROMEP/ROMLP array clocked read timing diagram
01/10/2001	237	Added ROMEP/ROMLP ARYSEL timing data
10/11/2000	19	Added multiport compilable register arrays minimum voltage
10/11/2000	152–153, 156	Updated SRAM1R delay tables, "SRAM1R Access Time, Internal Capacitance, and Physical Area Examples"
10/11/2000	206, 209, 211, 211	Updated SRAM4G delay definitions, and "SRAM4G Access Time, Internal Capacitance, and Physical Area Examples". Added SER paragraph

Date	Page	Description
10/11/2000	212	Updated BIST4G macro dimensions and area
10/11/2000	231, 237	Updated ROMLP/ROMEP "Non-Power-of-Two NWORD Counts" paragraph and delay definitions
10/11/2000	264–265, 272	Added CAMB delay definitions, SER paragraph
10/11/2000	297, 313–314, 320–322	Updated "PLL Tuning Bit Recommended Default Settings", physical placement restrictions, and "Guidelines to Minimize Jitter"
9/20/2000	22, 28	Updated "Multiport Compilable Register Arrays" symbol naming conventions, timing modes descriptions
9/20/2000	81, 101, 117, 138, 143, 164, 171, 175, 190, 195, 212, 217, 230, 244, 273	Added SRAM and BIST supported V_{dd} range
9/20/2000	96–100	Added SRAM1A—Compilable One-Port SRAM for Low Voltage
9/20/2000	105–120	Added "SRAM1LR—Compilable Low Power One-Port SRAM with Fuse Redundancy"
9/20/2000	146	Added SRAM1R "Usage Limitations"
9/20/2000	159–163	Added "SRAM1RN—Compilable High Density One-Port SRAM without Fuse Redundancy"
9/20/2000	165, 167	Updated BIST1R fuse redundancy paragraph and SCANOUT pin description
9/20/2000	169–170	Added "BIST1RN—BIST Controller for SRAM1RN without Fuse Redundancy"
9/20/2000	184–185, 188	Added SRAM2B delay data, updated "SRAM2B Access Time, Internal Capacitance, and Physical Area Examples"
9/20/2000	206, 209, 211, 211	Updated SRAM4G footprint, "SRAM4G Access Time, Internal Capacitance, and Physical Area Examples", and LSSD latch counts
9/20/2000	212	Updated BIST4G macro dimensions and area

Date	Page	Description
9/20/2000	227–228	Updated “ROMEH Access Time, Internal Capacitance, and Physical Area Examples” and “ROMLH Access Time, Internal Capacitance, and Physical Area Examples”
9/20/2000	240–241	Updated "ROMEP Access Time, Internal Capacitance, and Physical Area Examples" and "ROMLP Access Time, Internal Capacitance, and Physical Area Examples"
9/20/2000	266,269, 271–272	Added CAMB "Area, Timing, and Power Estimates", "Combining Arrays". Updated “CAMBPE Timings, Internal Capacitance, and Physical Area Examples” and “CAMBML Timings, Internal Capacitance, and Physical Area Examples”
7/26/2000	53–73	Updated Embedded DRAM to include x 292 configuration, miscellaneous other pages
7/26/2000	135	Updated SRAM2G footprint
7/26/2000	145	Updated SRAM1R “Valid SRAM1R Configurations”
7/26/2000	166, 167	Updated BIST1R POR and SCANOUT pin descriptions
7/26/2000	188	Updated "SRAM2B Access Time, Internal Capacitance, and Physical Area Examples"
7/26/2000	195–216	Added SRAM4G and BIST4G
7/26/2000	221, 234	Updated BCLK pin definition in ROMEH, ROMLH, ROMEP, ROMLP
7/26/2000	227–228, 240–241	Updated "ROMEH Access Time, Internal Capacitance, and Physical Area Examples", "ROMLH Access Time, Internal Capacitance, and Physical Area Examples", "ROMEP Access Time, Internal Capacitance, and Physical Area Examples", "ROMLP Access Time, Internal Capacitance, and Physical Area Examples"
7/26/2000	271–272	Updated "CAMBPE Timings, Internal Capacitance, and Physical Area Examples", "CAMBML Timings, Internal Capacitance, and Physical Area Examples"
7/26/2000	323–327	Added Generic Fat Wire I/Os
4/25/2000	53	Embedded DRAM: changed “1.8V $\pm$ 10% operation” to “1.8V $\pm$ 0.15V” operation; updated signal/power connections
4/25/2000	72	Updated embedded DRAM signal/power connections
4/25/2000	63	Updated embedded DRAM "AC Parameters"
4/25/2000	55	Added embedded DRAM "Naming Conventions"
4/25/2000	75–77	Added embedded DRAM fat wire I/Os

Date	Page	Description
4/25/2000	95, 116, 137, 189, 158	Added soft error sensitivity to SRAM1G, SRAM1LG, SRAM2G, SRAM2B, and SRAM1R
4/25/2000	138	Updated BISTG global porosity
4/25/2000	175–189	Miscellaneous changes to SRAM2B
4/25/2000	190–194	Miscellaneous changes to BIST2B
4/25/2000	164	Updated BIST1R global porosity
4/25/2000	172	Updated "Fuse Naming Conventions and Dimensions"
4/25/2000	243–276	Added CAMB and CAMBBIST
4/25/2000	280, 312–313	Updated PLL area
2/11/2000	285, 287	Removed PLLOUTC pin from PLL7SFLIBEDV and PLL7SFLIBIDV drawings

Contents

Multiport Compilable Register Arrays

Multiport Compilable Register Arrays

Overview

The SA-27E compilable register array is a dense register file with asynchronous write and read functions. The register arrays were designed to provide a physically dense solution, as well as a high-performance solution for small multiport arrays by avoiding the overhead of array built-in self-test (ABIST). The storage cell used is a scannable LSSD latch and is fully compliant with IBM's LSSD test methodology. As a result, no macro isolation or additional I/Os for test purposes[1] are required. Note that the minimum V_{dd} supported by SA-27E compilable register arrays is 1.20V.

System Features

The maximum logical size is limited by the total number of bits in the array. As a result, it is possible to have large data widths with a small number of words, or a large number of words with a small data width. The register array system can deliver data bus widths ranging from 2 to 82 bits in increments of a single bit and word depths ranging from 8 to 256 words or 8 to 512 words, depending on the number of ports in the register array and the decode options supported for that configuration. Refer to Table 1 and Table 2 for a list of supported logical configurations, including supported decodes (see "Column Multiplexing ("Decode")" on page 20). Note that the word depth range in Table 1 includes support for arrays with non-power-of-two word depths.

Table 1. Valid Compilable Register Array Configurations

Decode Option[1]	Word Depth		Word Depth Granularity[2]	Bit Width	
	Min	Max		Min	Max
2	8	128	8	2	82
4	16	256	16	2	40
8	32	512	32	2	20

1. Decode option 8 is available for 2-port register arrays only.
2. Word depth granularity indicates the valid non-power-of-two word depths. For example, a register array with a decode of 2 can be compiled with 8, 16, 24, …, 128 words; a register array with a decode of 4 can be compiled with 16, 32, 48, …, 256 words; and a register array with decode 8 can be compiled with 32, 64, 96, …, 512 words.

1. With the exception of the QW pin. See "Quick Write" on page 21.

Multiport Configurations

Multiple port configurations are supported in the register array system. Each port has independent address and data pins. In the case of multiple write ports, each port also has independent bit write enable inputs. Refer to Table 2 for a list of the supported multiport configurations.

Table 2. Supported Multiport Configurations

Number of Ports	Number of Write Ports	Number of Read Ports	Decode Options Available
2	1	1	2, 4, 8
3	1	2	2, 4
4	2	2	2, 4

Column Multiplexing (“Decode”)

The array consists physically of rows and columns, with corresponding decoding. The column decoding requires 1, 2, or 3 address inputs, corresponding to a decode of 2, 4, or 8, respectively. Table 6 on page 27 defines which address bits are used for column decoding.

Decode options give rise to different physical implementations of the same logical array. If a register array is available with different decode values, the larger the decode, the physically taller and thinner the array will be.

Non-2^n Word Depths

The compilable register array system supports non-power-of-two word depths. When non-power-of-two arrays are requested, the physical array grows to exactly match the logical configuration. Note that data writes to addresses not in the logical (or physical) memory space will be lost. Reads to addresses not contained in the logical (or physical) memory domain will be mapped to the same address in the lower half of the memory domain. In other words, if a 24-word register array is used in a design and a read operation is performed on address 28, the register array reads address 12.

Bit Write Control

The register arrays have a bit write enable feature that allows the user to selectively enable specific bits during a write cycle. Each data bit on each write port has an associated bit write enable line. During a write cycle, if the bit enable line to a single bit or group of bits is held low, that bit or those bits, respectively, will not be written. Unused bit write pins should be tied high.

Quick Write

The register arrays have a quick write (QW) feature. The large number of latches contained in a register array can make the chip scan chains very long, and increase test time. To help manage this, the register arrays have a feature built into the architecture that allows four words within the array to be written at the same time. This feature has been designed for test purposes only. The register array QW pin must be driven by a test I/O, although this net can also be shared by other appropriate signals. For more detailed information concerning this feature, please contact your IBM representative.

Symbol Naming Conventions

The naming strategy for the register arrays is defined such that unique instance names can be created for each possible compiled configuration. The first group of characters in the name defines the generic array type, to which fields are appended for defining the various compilable options. The names adhere to the following convention:

RA**wwwXbbDdPxWyRzMm**

where:

RA	=	Type of macro (register array)
w	=	Total number of words: 3 digits
b	=	Data width in bits: 2 digits
d	=	Decode option: 1 digit (2, 4, 8)
x	=	Total number of ports (2, 3, 4)
y	=	Number of write ports (1 or 2)
z	=	Number of read ports (1, 2)
m	=	RA simulation mode

1	READ_WRITE
2	DATA_WRITE_THROUGH
3	CLOCKED_WRITE_THROUGH
4-7	(Reserved for future use)
8	ACTEST
9	SCAN

Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. Here is an example:

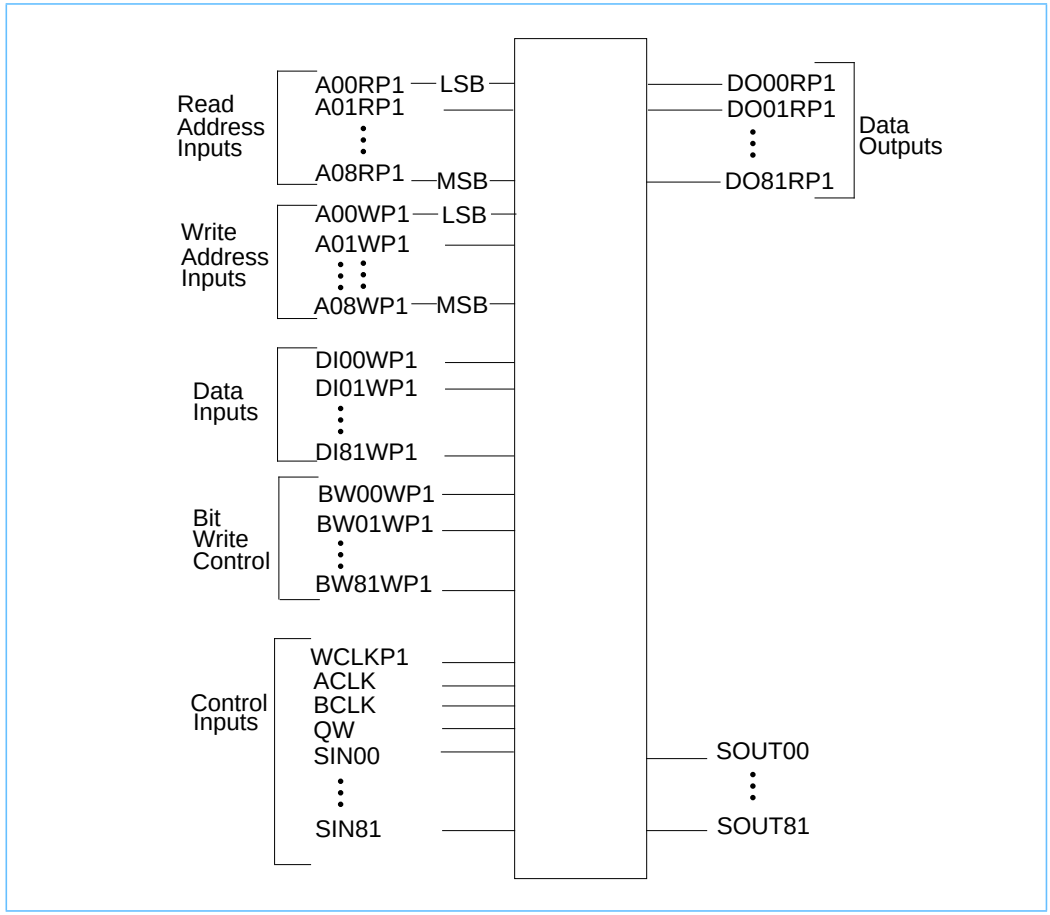
RA064X08D4P3W1R2M1	A 64-word x 8-bit register array, with a decode of 4 and three ports: one write port and two read ports. The simulation mode is normal read/write.

Logical Description

Logical Symbol

A symbolic representation of the compilable register array is shown in Figure 1.

Figure 1. Register Array Logic Symbol (2 port shown)



Symbolic View

Pin Definitions

Table 3 summarizes the function and proper usage of the macro pins shown in Figure 1 on page 23. The control and input pins must be stable before the write clock initiates a write access of the array. Pin timing relationships are described later.

Table 3. Register Array Pin Definitions

Pin	Definition
A00WPx–A0mWPx/ A00RPy–A0mRPy	Address pins are defined starting with A00, the least significant bit. The most significant bit address pin name, parameter “m” can be determined from the equation: $Words \leq 2^{m+1}$ Table 6 on page 27 defines which address bits are used for column decoding. The “WPx” stands for write port x, where x can be 1 or 2. The “RPy” stands for read port y, where y can also be 1 or 2.
DI00WPx–DInnWPx	The number of data input pins is dependent on the data bit count of the array selected. Pin names are assigned starting with DI00. The maximum value of “nn” is 81. As with the address ports, “WPx” stands for write port x, where x can be 1 or 2.
BW00WPx– BWnnWPx	A bit write enable pin is allocated for every data input pin in the array. The bit write (enable) control inputs are active high. If the input is held high during a write cycle, the corresponding data input bit is written into the array. If the pin is held low during a write cycle, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pin names are assigned starting with BW00WPx. The maximum value of “nn” is 81. If the bit write control feature is not used, the bit write pins should be tied high. As with the address ports, “WPx” stands for write port x, where x can be 1 or 2.
SIN00–SINnn	The SIN (scan-in) pins are allocated for scanning in data to the register array’s latches via the scan clocks (ACLK, BCLK) during test operation. The register array can be placed in a scan path with other elements on a chip. The SINnn pin must be used to conform to LSSD test requirements. There is one scan chain per bit in the register array. The scan chains are noninverting from input to output (SOUTnn). However, the scan-in signal is inverted internally to the register array and is reinverted just prior to exiting the register array (SOUTnn).
SOUT00–SOUTnn	The SOUT (scan-out) pins are allocated for scanning out data from the register array’s latches via the scan clocks (ACLK, BCLK) during test operation. SOUTnn is associated with SINnn for each “nn.”

Table 3. Register Array Pin Definitions (Continued)

Pin	Definition
QW	For improved chip-level test speeds, this signal allows four words to be written at the same time. The QW input pin must be connected to a chip-level scan gate in order to be used by the tester. This feature only affects write port 1 on the four-port (two write port) configurations. This signal must be held low (inactive) during functional operation. This signal must also be driven by a test I/O, though this net may also be shared.
ACLK	The ACLK (master scan clock) pin is used only during test operation of the register array. This pin must originate from a primary input, but can be common with other A clocks on the chip. This signal must be held low (inactive) during functional operation.
BCLK	The BCLK (slave scan clock) pin is used only during test operation of the register array. This pin must originate from a primary input, but can be common with other B clocks on the chip. This signal must be held low (inactive) during functional operation.
WCLKPx	When WCLKPx (write clock) is high, the storage element is transparent. This signal is identical to the LSSD C clock and must follow all rules that apply to a C clock. The “Px” implies that this write clock is for write port x, where x can be either a 1 or 2.
DO00RPy–DOnnRPy	The data output pins have the same polarity and pin count as the data input pins. Pin names begin with DO00RPy. The maximum value of “nn” is 81. Read operations do not involve a clock (are “static”). The results of a read remain on the data output pins until the read address inputs change, or, if read and write addresses are equal and if the write clock is active, the data inputs change (this is the “write-through” mode). Read operations from one port are unaffected by reads from other ports. As with the address ports, “RPx” stands for read port y, where y can be 1 or 2.

Scan Chain Length

Each of the “nn” scan chains (one chain per bit of the data word) has a length equal to half the maximum addressable word depth (words/2).

Timing Diagrams

Write Cycle

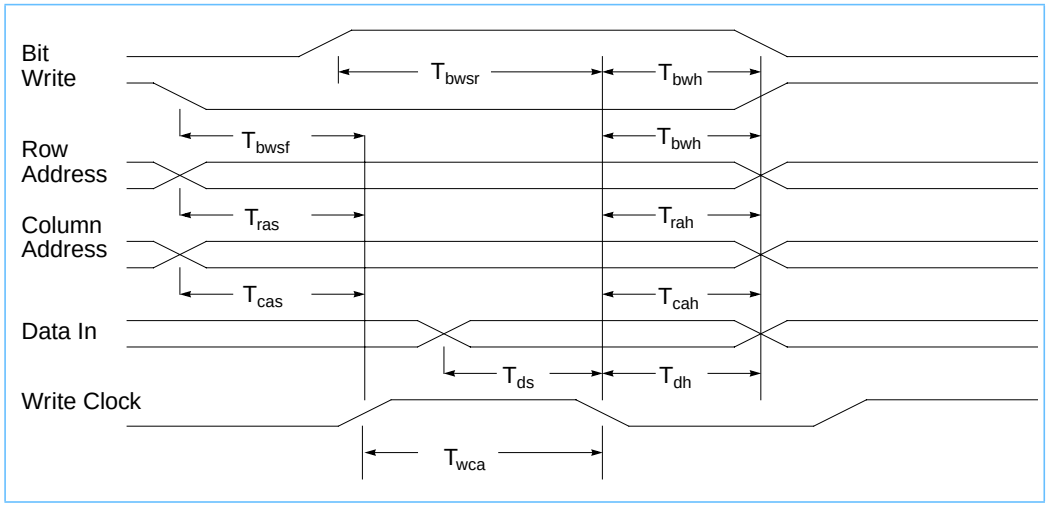


Table 4. Write Cycle Timing Parameters

Abbreviation	Parameter
T_{cas}, T_{cah}	Column address setup and hold time
T_{ras}, T_{rah}	Row address setup and hold time
$T_{bws(f,r)}$, T_{bwh}	Bit write enable setup and hold time
T_{ds}, T_{dh}	Data setup and hold time
T_{wca}	Write clock active (pulse width)

Write operations are initiated by and timed from the write clock(s) (WCLKP1, WCLKP2). Data, write address (split into column and row address), and bit write signals have timing requirements specified against both the rising and falling edges of the write clock(s). As with all level-sensitive latches, data timing requirements are specified against the falling edge of the write clock(s). Simultaneous, synchronous, and asynchronous write operations are permitted with one restriction: the write ports cannot have identical addresses during the same active write cycle. There is no circuitry to prevent a simultaneous write

to the same address. If this happens, the storage cell will be left in an unknown state. The simulation models will produce an unknown state for such an event as well.

Read Cycle

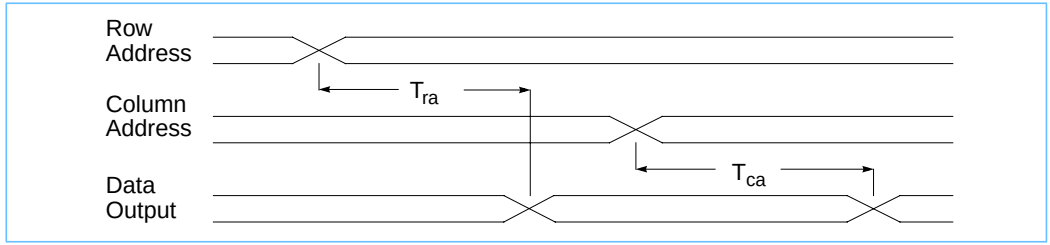


Table 5. Read Cycle Timing Parameters

Abbreviation	Parameter
T_{ca}	Column address access time
T_{ra}	Row address access time

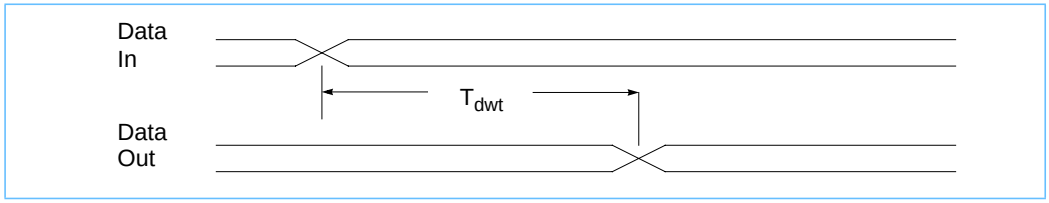
Read operations are performed through a process of address decoding and multiplexer selection. Read operations are not clocked. A read access is initiated by a change in the read address and is timed against the last valid read address to arrive at the register array. As with the write port, the read address signals are broken up into two categories: row address and column address.

The row address varies from two to six bits wide and is decoded into WORDS/DECODE unique row addresses. The row address pin assignments for each port begin with the first unused pin after the column address pin requirement is satisfied. Refer to Table 6 for more information.

Table 6. Row and Column Address by Decode

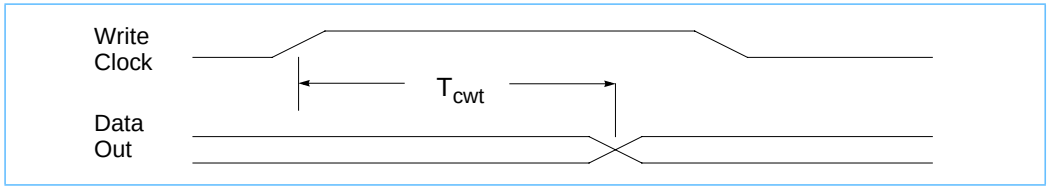
Register Array Decode	Read/Write Address	
	Row Address Range	Column Address Range
2	A06–A01	A00
4	A07–A02	A01–A00
8	A08–A03	A02–A00

Data Write-Through



The delay path, data in to data out (T_{dwt}), occurs when the write clock is active, the bit write signals are held active and the write address equals the read address.

Clocked Write-Through



The delay path, write clock rising to data out (T_{cwt}), occurs when the read address equals the write address, bit write signals are held active, and the data-in signals are assumed to be stable before the write clock activates (rises).

Timing Modes

READ_WRITE mode includes timings for all the timing parameters defined in Table 4 on page 26 and Table 5 on page 27. Use of READ_WRITE mode assumes that no write-through conditions (defined below) will occur, where the user is responsible for ensuring that such conditions are prevented by the chip-level logic design.

DATA_WRITE_THROUGH mode includes all the timings defined in READ_WRITE mode, plus the assumption that write-through conditions are permitted. A write-through condition is defined as an equivalence of logic states between the read address of a given read port and the write address of a given write port when the given write port's WCLK is active (high). However, if all bit write signals are disabled for the given write port, no write-through paths from that write port will exist. When a bit write signal is low, a write

operation to the bit (implicitly denoted within the bit write's pin name—see Table 3 on page 24) is blocked.

Two write-through propagation delay timings are possible in DATA_WRITE_THROUGH mode:

1. From data-in to data-out
2. From WCLK to data-out

Note that since the data-in setup requirements are the same as in READ_WRITE mode, either the data-in or the WCLK may be the latent signal triggering a subsequent change in state for data-out when a write-through condition occurs.

CLOCKED_WRITE_THROUGH mode includes all the timings defined in READ_WRITE mode, with the exception of a modified data-in setup test, and with the assumption that write-through conditions are permitted. In CLOCKED_ WRITE_THROUGH mode, a data-in setup check is made with respect to the clock's rising edge instead of the falling edge (as in READ_WRITE mode); therefore, the data-in signals must be stable before the WCLK goes high.

As a result of this restriction, the only write-through propagation delay possible in CLOCKED_WRITE_THROUGH mode is WCLK to data-out (the clocked write-through delay path). Thus, write-through delays in this mode are always forced to be timed with respect to the WCLK's rising edge.

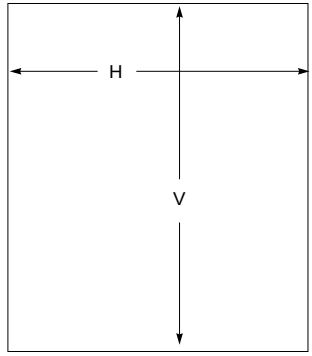
Example Timings

Table 7. Example Timings for a Two-Port, 16-Bit Register Array

Words	Decode	T_{ra}	T_{ca}	T_{ras}	T_{cas}	T_{bws}	T_{ds}	T_{rah}	T_{cah}	T_{bwh}	T_{dh}	Twca
16	2	0.74	0.50	0.12	0.01	0.02	0.21	0.08	0.16	0.18	0.21	0.43
128	4	1.01	0.64	0.16	0.09	0.15	0.27	0.18	0.12	0.21	0.23	0.44
256	8	1.14	1.01	0.05	0.02	-0.01	0.17	0.34	0.22	0.40	0.39	0.58

Note: All timings (in ns) for nominal process, 1.8V V_{dd}, 85˚C, input transition of 0.2 ns, and 0.5 pF load

Area Calculations



The approximate sizes for the register arrays are given by the following equations. The dimensions are in cells.

$$H = \left[\left(\left(\frac{Words}{Decode}\right) \times h1\right) + h2\right]$$

$$V = \left\lceil \frac{(Bits \times v1 \times Decode) + v2}{12} \right\rceil$$

Table 8. Definition of Variables

Variable	Definition
Words	Number of words (8, 12, 16, …, 512)
Bits	Data width (number of bits per word)
Decode	Decode option (2, 4, or 8)

Table 9. Physical Size Parameters

Number of Ports	h1	h2 (by Decode)			v1	v2
		D = 2	D = 4	D = 8		
2	7	56	67	72	14	119
3	10	64	84	n/a	14	155
4	12.5	78	103	n/a	16	200

Compilable Extended Voltage Register Arrays

Overview

The SA-27E compilable extended voltage register array (RAEV) is a supplement to the pre-existing SA-27E compilable register array (RA). The RAEV supports a voltage range beyond that supported by the RA. Refer to Table 10 for a voltage range comparison between the RA and RAEV.

Table 10. RA/RAEV V_{dd} Range

Macro Type	Maximum V_{dd}	Minimum V_{dd}
Register array (RA)	1.95V	1.20V
Register array, extended voltage (RAEV)	1.95V	0.90V

The RAEV is equivalent to the RA in terms of function and behavior. However, the RAEV's internal circuit architecture is distinct from that of the RA, so characteristics such as size, timing, and soft-error rate (SER)[1], etc. is different between the two designs. In addition, the SA-27E RAEV is a limited offering of only 2-port, decode 2, configurations.

System Features

The maximum logical size is limited by the total number of bits in the array. As a result, it is possible to have large data widths with a small number of words, or a large number of words with a small data width. The RAEV compilable system can deliver data bus widths ranging from 2 to 82 bits in increments of a single bit and word depths ranging from 8 to 128 words. Refer to Table 11 on page 32 for a list of supported logical configurations. Note that the word depth range in Table 11 includes support for arrays with non-power-of-two word depths.

1. Contact your IBM representative for more information regarding SER.

Table 11. Valid Compilable RAEV Configurations

Number of Ports	Number of Write Ports	Number of Read Ports	Decode Option	Word Depth		Word Depth Granularity[1]	Bit Width	
				Min	Max		Min	Max
2	1	1	2	8	128	8	2	82

3. Word depth granularity indicates the valid non-power-of-two word depths. For example, an RAEV can be compiled with 8, 16, 24, …, 128 words.

Column Decoding/Multiplexing (“Decode”)

The RAEV’s embedded latch array physically consists of rows and columns. The read address and write address decoders and multiplexers are each split into designated “row” and “column” subcirucuts. For a decode 2 option (the only option for SA-27E RAEVs), the column portion of the write address decoder is a 1 x 2 decoder, and the column portion of the read address multiplexer is a 2 x 1 multiplexer. The row decoders and multiplexers handle routing for the remaining address pins. Table 15 on page 39 defines the address bits used for column decoding.

Non-2^n Word Depths

The compilable RAEV supports non-power-of-two word depths. When non-power-of-two arrays are requested, the physical array grows to exactly match the logical configuration. Note that data writes to addresses not in the logical (or physical) memory space will be lost. Reads to addresses not contained in the logical (or physical) memory domain will be mapped to the same address in the lower half of the memory domain. In other words, if a 24-word register array is used in a design and a read operation is performed on address 28, the register array reads address 12.

Soft Error Rate

Other than extended-voltage operation, a significant difference between the RA and RAEV designs is the SER specification. The RAEV designs have a much lower FIT/kbit[1] value across each of the SER components (for example, cosmic, package, solder bump,

1. A “FIT” is defined as 1 fail/10^9 hours.

etc.). Consequently, the RAEV is the recommended choice over the RA for SER-sensitive applications. For quantitative estimates and more details regarding SER, contact your IBM representative.

Bit Write Control

The RAEVs have a bit write enable feature that allows the user to selectively enable specific bits during a write cycle. Each data bit has an associated bit write enable line. During a write cycle, if the bit enable line to a single bit or group of bits is held low, that bit or those bits, respectively, will not be written. Unused bit write pins should be tied high.

Quick Write

Like the register arrays, the RAEVs have a quick write (QW) feature. The large number of latches contained in an RAEV can make the chip scan chains very long, and increase test time. To help manage this, the RAEVs have a feature built into the architecture that allows four words within the array to be written at the same time. This feature has been designed for test purposes only. The RAEV QW pin must be driven by a test I/O, although this net can also be shared by other appropriate signals. For more information concerning this feature, please contact your IBM representative.

Symbol Naming Conventions

The naming strategy for the RAEVs is defined such that unique instance names can be created for each possible compiled configuration. The first group of characters in the name defines the generic array type, to which fields are appended for defining the various compilable options. The names adhere to the following convention:

RAEV**wwwXbbDdPxWyRzMm**

where:

RAEV	=	Type of macro (register array)
w	=	Total number of words: 3 digits
b	=	Data width in bits: 2 digits
d	=	Decode option: 1 digit (2)
x	=	Total number of ports (2)
y	=	Number of write ports (1)
z	=	Number of read ports (1)
m	=	RAEV simulation mode

1	READ_WRITE
2	DATA_WRITE_THROUGH
3	CLOCKED_WRITE_THROUGH
4-7	(Reserved for future use)
8	ACTEST
9	SCAN

Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. An example is shown below.

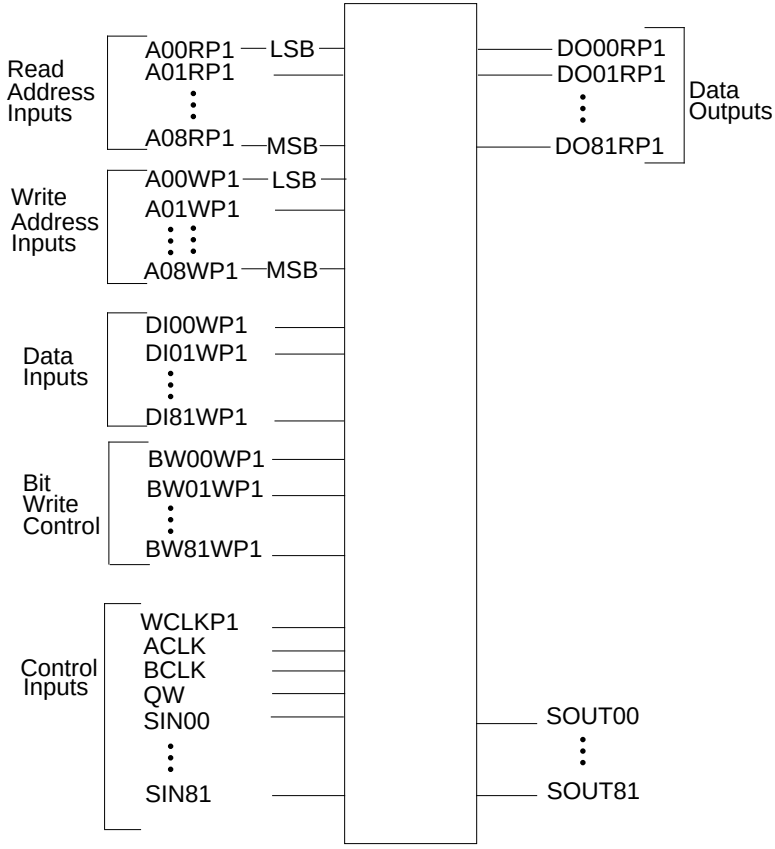
RAEV064X08D2P2W1R1M1	A 64-word x 8-bit RAEV, with a decode of 2 and two ports: one write port and one read port. The simulation mode is READ_WRITE.

Logical Description

Logical Symbol

A symbolic representation of the compilable RAEV is shown in Figure 2.

Figure 2. RAEV Logic Symbol (2-port shown)



Symbolic View

Pin Definitions

Table 12 summarizes the function and proper usage of the macro pins shown in Figure 2 on page 35. The control and input pins must be stable before the write clock initiates a write access of the array. Pin timing relationships are described later. Pin naming conventions for the RAEVs are consistent with those used for SA-27E RAs.

Table 12. RAEV Pin Definitions

Pin	Definition
A00WPx–A0mWPx/ A00RPy–A0mRPy	Address pins are defined starting with A00, the least significant bit. The most significant bit address pin name, parameter “m” can be determined from the equation: $$Words \leq 2^{m+1}$$ Table 15 on page 39 defines which address bits are used for column decoding. The “WPx” stands for write port x, where x can only be 1. The “RPy” stands for read port y, where y can also only be 1.
DI00WPx–DInnWPx	The number of data input pins is dependent on the data bit count of the array selected. Pin names are assigned starting with DI00. The maximum value of “nn” is 81. As with the address ports, “WPx” stands for write port x, where x can only be 1.
BW00WPx– BWnnWPx	A bit write enable pin is allocated for every data input pin in the array. The bit write (enable) control inputs are active high. If the input is held high during a write cycle, the corresponding data input bit is written into the array. If the pin is held low during a write cycle, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pin names are assigned starting with BW00WPx. The maximum value of “nn” is 81. If the bit write control feature is not used, the bit write pins should be tied high. As with the address ports, “WPx” stands for write port x, where x can only be 1.
SIN00–SINnn	The SIN (scan-in) pins are allocated for scanning in data to the RAEV’s latches via the scan clocks (ACLK, BCLK) during test operation. The RAEV can be placed in a scan path with other elements on a chip. The SINnn pin must be used to conform to LSSD test requirements. There is one scan chain per bit in the RAEV. The scan chains are noninverting from input to output (SOUTnn). However, the scan-in signal is inverted internally to the RAEV and is reinverted just prior to exiting the RAEV via the scan-out pin.
SOUT00–SOUTnn	The SOUT (scan-out) pins are allocated for scanning out data from the RAEV’s latches via the scan clocks (ACLK, BCLK) during test operation. SOUTnn is associated with SINnn for each “nn.”

Table 12. RAEV Pin Definitions (Continued)

Pin	Definition
QW	For improved chip-level test speeds, this signal allows four words to be written at the same time. The QW input pin must be connected to a chip-level scan gate in order to be used by the tester. This signal must be held low (inactive) during functional operation. This signal must also be driven by a test I/O, though this net may also be shared.
ACLK	The ACLK (master scan clock) pin is used only during test operation of the RAEV. This pin must originate from a primary input, but can be common with other A clocks on the chip. This signal must be held low (inactive) during functional operation.
BCLK	The BCLK (slave scan clock) pin is used only during test operation of the RAEV. This pin must originate from a primary input, but can be common with other B clocks on the chip. This signal must be held low (inactive) during functional operation.
WCLKPx	When WCLKPx (write clock) is high, the storage element is transparent. This signal is identical to the LSSD C clock and must follow all rules that apply to a C clock. The “Px” implies that this write clock is for write port x, where x can only be 1.
DO00RPy–DOnnRPy	The data output pins have the same polarity and pin count as the data input pins. Pin names begin with DO00RPy. The maximum value of “nn” is 81. Read operations do not involve a clock (are “static”). The results of a read remain on the data output pins until the read address inputs change, or, if read and write addresses are equal and if the write clock is active, the data inputs change (this is a “write-through” mode). Read operations from one port are unaffected by reads from other ports. As with the address ports, “RPx” stands for read port y, where y can only be 1.

Scan Chain Length

Each of the “nn” scan chains (one chain per bit of the data word) has a length equal to half the maximum addressable word depth (words/2).

Timing Diagrams

Write Cycle

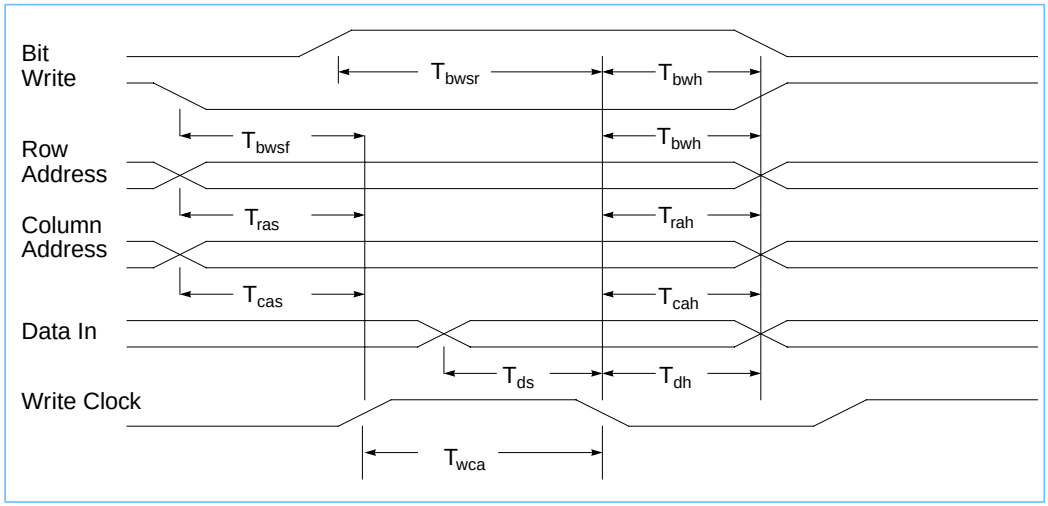


Table 13. Write Cycle Timing Parameters

Abbreviation	Parameter
T_{cas}, T_{cah}	Column address setup and hold time
T_{ras}, T_{rah}	Row address setup and hold time
$T_{bws\ (f,\ r)}$, T_{bwh}	Bit write enable setup and hold time
T_{ds}, T_{dh}	Data setup and hold time
T_{wca}	Write clock active (pulse width)

Write operations are initiated by and timed from the write clock, WCLKP1. Data, write address (split into column and row address), and bit write signals have timing requirements specified against both the rising and falling edges of the write clock. As with all level-sensitive latches, data timing requirements are specified against the falling edge of the write clock.

Read Cycle

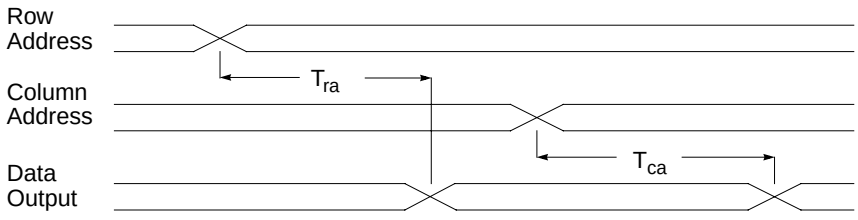


Table 14. Read Cycle Timing Parameters

Abbreviation	Parameter
T_{ca}	Column address access time
T_{ra}	Row address access time

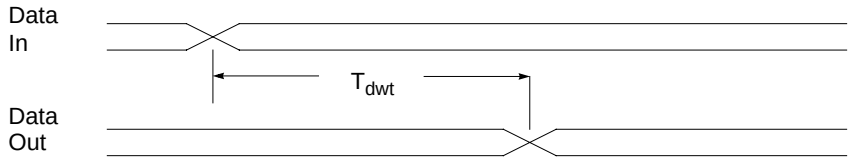
Read operations are performed through a process of address decoding and multiplexer selection. Read operations are not clocked. A read access is initiated by a change in the read address and is timed against the last valid read address to arrive at the RAEV. As with the write port, the read address signals are broken up into two categories: row address and column address.

The row address varies from two to six bits wide and is decoded into WORDS/DECODE unique row addresses. The row address pin assignments for each port begin with the first unused pin after the column address pin requirement is satisfied. Refer to Table 15 for more information.

Table 15. Row and Column Address Pins

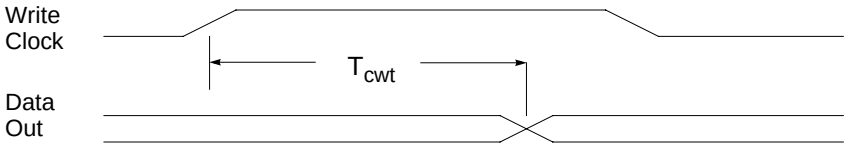
Decode	Read/Write Address	
	Row Address Pin Range	Column Address Pin Range
2	A06–A01	A00

Data Write-Through



The delay path, data in to data out (T_{dwt}), occurs when the write clock is active, the bit write signals are held active, and the write address equals the read address.

Clocked Write-Through



The delay path, write clock rising to data out (T_{cwt}), occurs when the read address equals the write address, bit write signals are held active, and the data in signals are assumed to be stable before the write clock activates (rises).

Timing Modes

READ_WRITE mode includes timings for all the timing parameters defined in Table 13 on page 38 and Table 14 on page 39. Use of READ_WRITE mode assumes that no write-through conditions (defined below) will occur, where the user is responsible for ensuring that such conditions are prevented by the chip-level logic design.

DATA_WRITE_THROUGH mode includes all the timings defined in READ_WRITE mode, with the added assumption that write-through conditions are permitted. A write-through condition is defined as an equivalence of logic states between the read address and the write address when WCLKP1 is active (high). However, if all bit write signals are disabled, no write-through paths will exist. When a bit write signal is low, a write operation to the bit (implicitly denoted within the bit write's pin name—see Table 12 on page 36) is blocked.

Two write-through propagation delay timings are possible in DATA_WRITE_THROUGH mode:

1. From data-in to data-out
2. From WCLKP1 to data-out

Note that since the data-in setup requirements are the same as in READ_WRITE mode, either the data-in or the WCLKP1 may be the latent signal triggering a subsequent change in state for data-out when a write-through condition occurs.

CLOCKED_WRITE_THROUGH mode includes all the timings defined in READ_WRITE mode, with the exception of a modified data-in setup test, and with the assumption that write-through conditions are permitted. In CLOCKED_WRITE_THROUGH mode, a data-in setup check is made with respect to the clock's rising edge instead of the falling edge (as in READ_WRITE mode); therefore, the data-in signals must be stable before WCLKP1 goes high.

As a result of this restriction, the only write-through propagation delay possible in CLOCKED_WRITE_THROUGH mode is WCLKP1 to data-out (the clocked write-through delay path). Consequently, write-through delays in this mode are always forced to be timed with respect to the WCLKP1's rising edge.

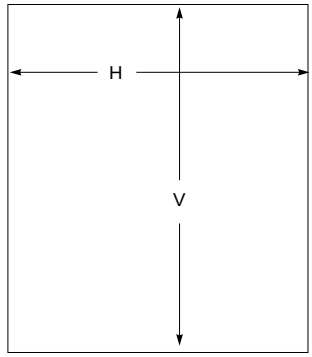
Example Timings

Table 16. Example Timings for a Two-Port, 16-Bit RAEV

Words	Decode	T_{ra}	T_{ca}	T_{ras}	T_{cas}	T_{bws}	T_{ds}	T_{rah}	T_{cah}	T_{bwh}	T_{dh}	Twca
16	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
128	2	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD

Note: All timings (in ns) for nominal process, 1.8V V_{dd}, 85˚C, input transition of 0.2 ns, and 0.5 pF load

Area Calculations



The approximate sizes for the RAEVs are given by the following equations. The dimensions are in cells.

$$H = \left\lceil \left(\left(\frac{Words}{2} \right) \times h1 \right) + h2 \right\rceil$$

$$V = \left\lceil \frac{(Bits \times v1 \times 2) + v2}{12} \right\rceil$$

Table 17. Definition of Variables

Variable	Definition
Words	Number of words (8, 12, 16, …, 128)
Bits	Data width (number of bits per word)

Table 18. RAEV Physical Size Parameters

h1	h2	v1	v2
7.25	56 + X[1]	14	119

1. X = 0; for WORDS/DECODE = 4, 8, 12, 16, 20, or 24
   X = 3; for WORDS/DECODE = 28, 32, 36, 40, 44, or 48
   X = 6; for WORDS/DECODE = 52, 56, 60, or 64

Electronic Chip Identification

Electronic Chip Identification (ECID)

Overview

The SA-27E ECID macro is an 80 bit latch string which stores a unique binary string per packaged module. The ECID information is programmed into laser fuses inside the macro after wafer final test. This chip information can be sensed into fuse latches whose contents can be either scanned out or read out of the macro in parallel. The fuse latches are scannable LSSD latches and are fully compliant with IBM's LSSD test methodology.

Naming Convention

ECID names adhere to the following conventions:

ECID_xyyzz

where:

x	=	Number of levels of metal for the image
yy	=	Last level of metal: LM, MT, or MZ
zz	=	Image type: C4 or WB (for wire bond)

Modes of Operation

Input Truth Table

Table 19. Mode Selection Table as a Function of Inputs

Inputs						Mode
TESTM3	POR	CCLK	ACLK	BCLK	SCANIN	
0	1-to-0	1	0	1	X	Fuse latch sense operation
0	0	X	0	X	X	Functional mode
1	X	X	X	X	X	Logic test

Fuse Latch Sense Operation: The ECID fuse states are read into the fuse latches (i.e., sensed) when CCLK is high and POR switches from high to low, where POR is the latent signal for sensing the fuses. TESTM3 and ACLK must be low during fuse latch sense. BCLK must be high for the fuse values to be propagated to the FUSEnn output pins. Fuse latch sense needs to occur at least once on chip power-up and also after logic test where the fuse latches are scanned (via ACLK/BCLK scan cycles). Fuse latch sense refreshes the fuse latches with the ECID's fuse data.

Functional Mode: Functional mode is a typical ECID state after fuse latch sense, where the fuse data remain available on the FUSEnn output pins when BCLK is held high. POR, TESTM3, and ACLK must be held low.

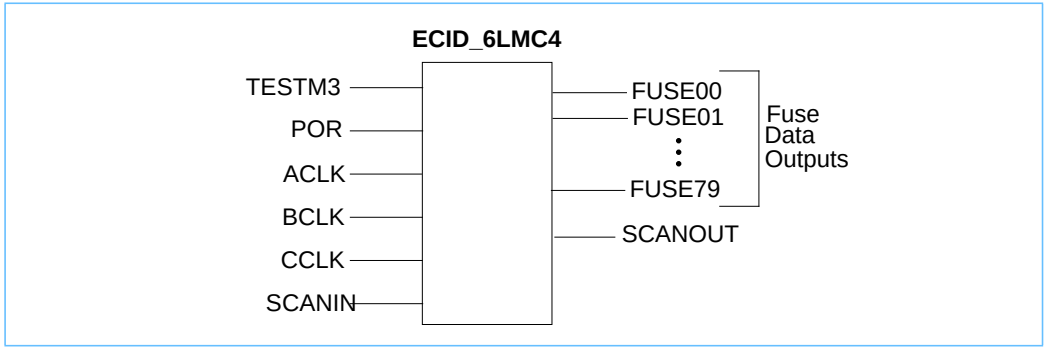
Logic Test: TESTM3, which gates POR and CCLK, must be held high during logic test.

Logical Description

Logical Symbol

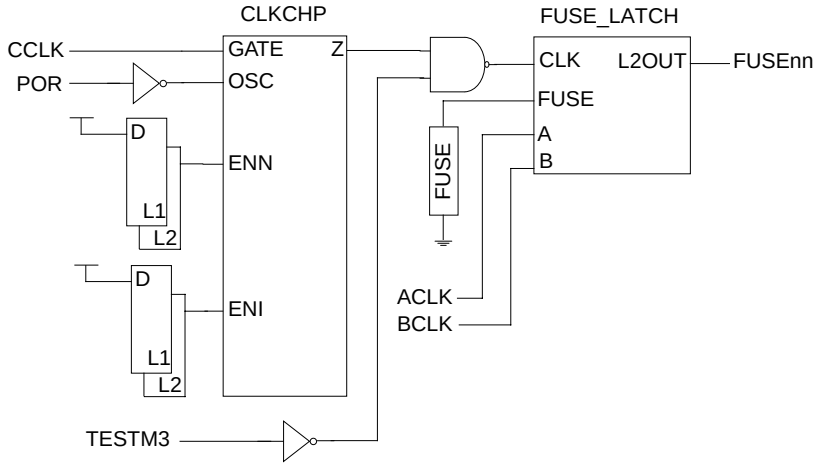
A symbolic representation of the ECID is shown in Figure 3.

Figure 3. ECID Logic Symbol



Block Diagram

Figure 4. ECID Block Diagram Showing Functional Input Circuitry



ECID Pin Definitions

Table 20 describes the function and proper usage of the macro pins shown above.

Table 20. ECID Pin Definitions

Pin	Definition
TESTM3	Inhibits the fuse from being sensed during logic test.
POR	Power-on reset. Enables the customer to sense the fuses and read the ECID contents. The POR pin is used only during the fuse sense latch operation, during which it must transition from 1 to 0.
ACLK	The ACLK (master scan clock) pin is used only during test operations. During functional operation this pin should be held low. This pin must originate from a primary input, but may be common with other A clocks on the chip.
BCLK	The BCLK (slave scan clock) pin is used during the fuse sense latch operation, during which it must be held high if the fuse latch data is to be propagated to the FUSEnn output pins. This pin is also used during test operations and must originate from a primary input, but may be common with other B clocks on the chip.

Table 20. ECID Pin Definitions (Continued)

Pin	Definition
CCLK	The CCLK pin is used only during the fuse sense latch operation, during which it must be held high.
SCANIN	The SCANIN pin is used to scan through data in previous latches through the ECID to a primary output.
FUSE00 - FUSE79	FUSEnn is the L2 output for each fuse latch. Once the fuse value is sensed and captured in the latch the values can be read at these outputs without scanning (using A and B clocks). If these outputs are not used, they should be left floating; these pins should never be tied to a fixed voltage.
SCANOUT	The SCANOUT pin is used to scan ECID and other test data through the ECID macro to a primary output.

Scan Chain Ordering

On entry to the ECID, the SCANIN signal is first sent to a small chain of three L1-L2 latches. The first L1-L2 latch is the ENN latch, whose SCANOUT signal feeds the SCANIN of the ENI latch. Both the ENN and ENI latches are pictured in Figure 3 on page 46, without the detail of the scan chain connections. The SCANOUT of the ENI latch feeds the SCANIN of another L1-L2 latch (not pictured). The SCANOUT from this L1-L2 latch is sent to the internal scan in net for the fuse latch associated with FUSE79 (i.e., fuse latch 79). The internal scan out net of fuse latch 79 feeds the internal scan in net of fuse latch 78, and so on. Finally, the internal scan out net of fuse latch 00 is buffered and sent out of the ECID as the SCANOUT pin. In total, the ECID scan chain winds through a total of 83 latches.

Fuse Contents

Table 21. Breakdown of Fuse String Information.

FUSE#	Data
FUSE00–FUSE 63	Unique binary signature
FUSE64–FUSE79	IBM internal use

Physical Size

Table 22. Physical Size Parameters

ECID Macro	X (in cells)	Y (in cells)	Total (in cells)
ECID_6LMC4	266	72	19152
ECID_6MZC4	266	59	15694
ECID_5MZC4	266	59	15694
ECID_6MTWB	266	59	15694
ECID_5MTWB	266	59	15694
ECID_4MTWB	266	59	15694

Embedded DRAM

Embedded DRAM

Functional Summary

- Two configurations: x 256 or x 292
- 1 Mb to 16 Mb in 1 Mb increments
  - Multiple macros per chip for greater capacity or functional flexibility
  - Additional width for parity
- Data I/O organization:

x 256 configuration	- 256-bit data in with 256-bit write mask - 256-bit data out
x 292 configuration	- 292-bit data in with 292-bit write mask - 292-bit data out

- Broadside addressing
  - Up to 16-bit address
    - Three bit (eight transfer) low-order page addressing
  - Random access and page access modes
- Synchronous or asynchronous operation
- Performance at worst case process and voltage[1]
  - Random access mode: 13 ns access, 50 MHz clock cycle
  - Page access mode: 6.6 ns access, 150 MHz clock cycle
  - 2 pF data out drive

1. The embedded DRAM does not support the full SA-27E ambient operating temperature range, junction temperature range, and storage temperature range at this time. Contact your IBM representative for current specifications.

- 3.2 ms refresh period
  - Distributed refresh, burst refresh, or a combination of distributed and burst refresh are allowed, provided that all word addresses are refreshed within the specified refresh period
- Row and column redundancy
  - Eight data lines can be replaced in every 1 Mb block
  - Eight word lines can be replaced in every 1 Mb block
- 1.8V $\pm$ 0.15V operation
- Full memory BIST
  - Single pass test on logic tester
  - In-macro redundancy calculation
  - *In situ* memory burn-in capability
- Wiring
  - Blocked through M3
  - Signal connections at M1; power connections at M1–M3
  - Signal pins located along one side and repeat on logic cell height pitch
  - Macro can be mirrored horizontally and/or vertically, but not rotated
- VHDL, Verilog, Synopsys, .LEF, and .VIM models provided

Macro Sizes

Table 23. Embedded DRAM Macro Sizes

Macro Capacity (megabits)	x 256 Configuration			x 292 Configuration		
	Macro X (mm)	Macro Y (mm)	Macro Area (mm^2)	Macro X (mm)	Macro Y (mm)	Macro Area (mm^2)
1	1.249	2.654	3.31	1.249	2.930	3.66
2	1.646	2.654	4.37	1.646	2.930	4.82
3	2.089	2.654	5.54	2.089	2.930	6.12
4	2.486	2.654	6.6	2.486	2.930	7.28
5	2.929	2.654	7.77	2.929	2.930	8.58
6	3.326	2.654	8.83	3.326	2.930	9.75
7	3.769	2.654	10.01	3.769	2.930	11.04
8	4.166	2.654	11.06	4.166	2.930	12.21
9	4.609	2.654	12.23	4.609	2.930	13.50
10	5.006	2.654	13.28	5.006	2.930	14.67
11	5.449	2.654	14.46	5.449	2.930	15.97
12	5.846	2.654	15.51	5.846	2.930	17.13
13	6.343	2.654	16.83	6.343	2.930	18.58
14	6.740	2.654	17.89	6.740	2.930	19.75
15	7.183	2.654	19.06	7.183	2.930	21.05
16	7.580	2.654	20.12	7.580	2.930	22.21

Naming Conventions

The naming strategy for the embedded DRAM macro is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the macro type, after which are appended fields to define the configuration options. Leading zeros are used in numerical fields to keep all instance

names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

DRAMwwwwXcXddd

where:

DRAM = DRAM macro

w = total number of word addresses: 4 digits

c = total number of column addresses: 1 digit

d = data width in bits: 3 digits

A representative example would be:

DRAM0512X8X256 A DRAM with 512 row addresses and 8 column addresses, 256 data bits wide.

Pin Descriptions

Table 24. Embedded DRAM Pin Descriptions: x 256 Configuration

Signal	Count	Description	I/O
Control			
MSN[1]	1	Macro select	I
PGN[1]	1	Page mode select	I
WEN[1]	1	Write enable	I
REFN[1]	1	Refresh enable	I
POR	1	Power on reset	I

1. All control input signals are negative active.
2. x is dependent on macro size and varies from 11–15.
3. High level enables write; low level disables write.
4. Analog power supply tester inputs.

Table 24. Embedded DRAM Pin Descriptions: x 256 Configuration (Continued)

Signal	Count	Description	I/O
Address			
A00–A02	3	Column address	I
A03–Ax[2]	9–13	Row address	I
Data			
DI000–DI255	256	Data inputs	I
BW000–BW255[3]	256	Bit write inputs	I
DO000–DO255	256	Data outputs	O
Test			
ACLK	1	LSSD A clock	I
BCLK	1	LSSD B clock	I
CCLK	1	LSSD C clock	I
C2CLK	1	LSSD C clock	I
SI0–SI9	10	Scan in	I
SO0–SO9	10	Scan out	O
OSC	1	Oscillator input	I
EN	1	Oscillator enable	I
TSTN0–TSTN1	2	Test mode enable	I
MSTR0	1	MBIST result (real time)	O
PCNT	1	Pause counter test input	I
TSF0–TSF1	2	Test data save flag	O
DLT	1	I_{ddq} test input	I
VPP[4]	1	Word line high bias	I

1. All control input signals are negative active.
2. x is dependent on macro size and varies from 11–15.
3. High level enables write; low level disables write.
4. Analog power supply tester inputs.

Table 24. Embedded DRAM Pin Descriptions: x 256 Configuration (Continued)

Signal	Count	Description	I/O
VWL[4]	1	Word line low bias	I
VREFX[4]	1	Reference cell bias	I
SYNC	1	Diagnostic trigger	O

1. All control input signals are negative active.
2. x is dependent on macro size and varies from 11–15.
3. High level enables write; low level disables write.
4. Analog power supply tester inputs.

Table 25. Embedded DRAM Pin Descriptions: x 292 Configuration

Signal	Count	Description	I/O
Control			
MSN[1]	1	Macro select	I
PGN[1]	1	Page mode select	I
WEN[1]	1	Write enable	I
REFN[1]	1	Refresh enable	I
POR	1	Power on reset	I
Address			
A00-A02	3	Column address	I
A03-Ax[2]	9–13	Row address	I
Data			
DI000–DI291	292	Data inputs	I
BW000–BW291[3]	292	Bit write inputs	I
DO000–DO291	292	Data outputs	O

1. All control input signals are negative active.
2. x is dependent on macro size and varies from 11–15.
3. High level enables write; low level disables write.
4. Analog power supply tester inputs.

Table 25. Embedded DRAM Pin Descriptions: x 292 Configuration (Continued)

Signal	Count	Description	I/O
Test			
ACLK	1	LSSD A clock	I
BCLK	1	LSSD B clock	I
CCLK	1	LSSD C clock	I
C2CLK	1	LSSD C clock	I
SI0–SI9	10	Scan in	I
SO0–SO9	10	Scan out	O
OSC	1	Oscillator input	I
EN	1	Oscillator enable	I
TSTN0–TSTN1	2	Test mode enable	I
MSTR0	1	MBIST result (real time)	O
PCNT	1	Pause counter test input	I
TSF0–TSF1	2	Test data save flag	O
DLT	1	I_{ddq} test input	I
VPP[4]	1	Word line high bias	I
VWL[4]	1	Word line low bias	I
VREFX[4]	1	Reference cell bias	I
SYNC	1	Diagnostic trigger	O

1. All control input signals are negative active.
2. x is dependent on macro size and varies from 11–15.
3. High level enables write; low level disables write.
4. Analog power supply tester inputs.

Truth Table

Table 26. Embedded DRAM Truth Table

Operation	MSN	PGN	WEN	REFN	Ax	DI	DO	BW
Random read	L	H	H	H	L/H	X	DOUT	X
Random write	L	H	L	H	L/H	L/H	L-R	L/H
Page read	L	L	H	H	L/H	X	DOUT	X
Page write	L	L	L	H	L/H	L/H	L-R	L/H
Refresh	L	H	H	L	X	X	L-R	X

1. X = Valid binary state; don't care if L or H
2. L/H = L or H depending on cycle
3. L-R = Last read data

Logical Description

Figure 5. x 256 Configuration

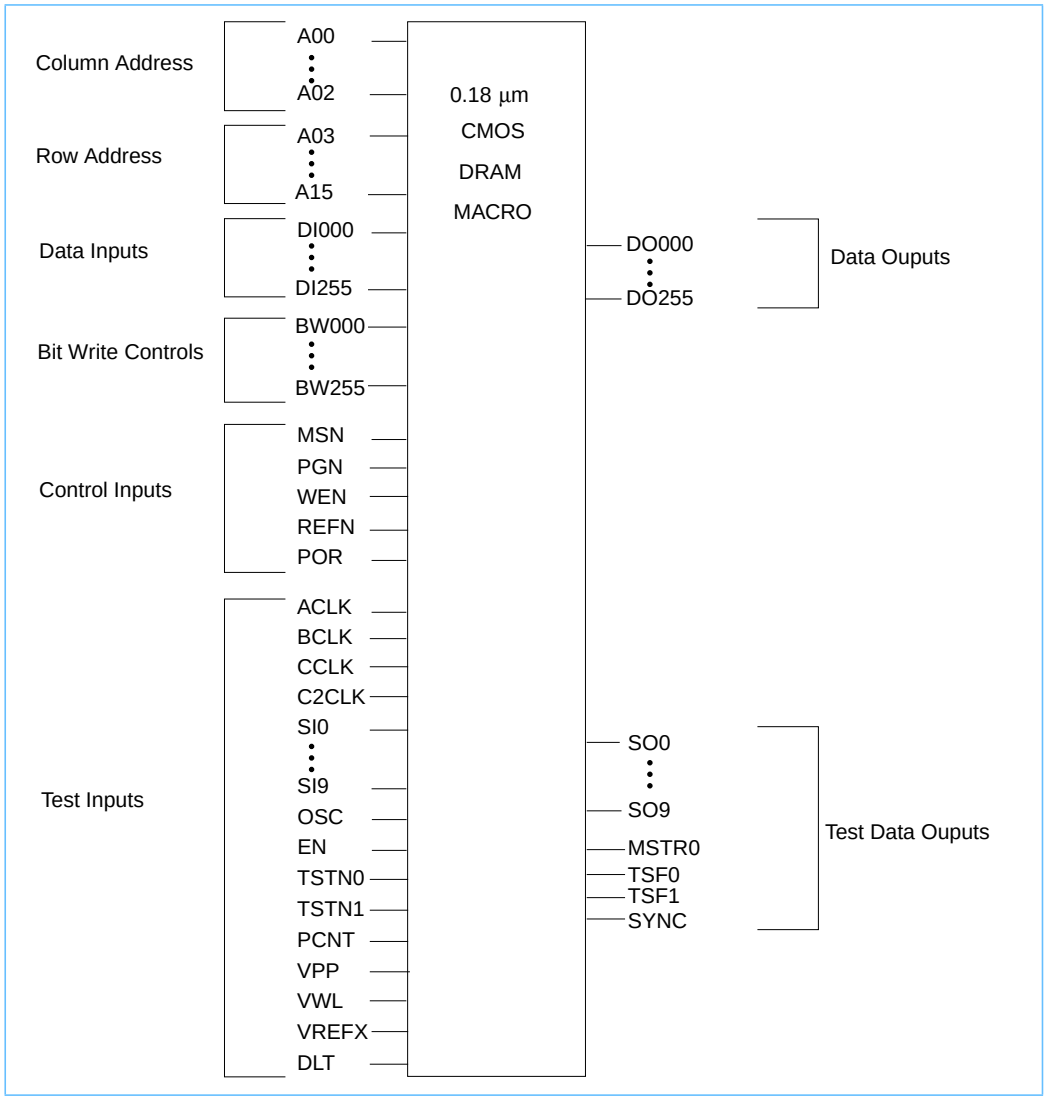
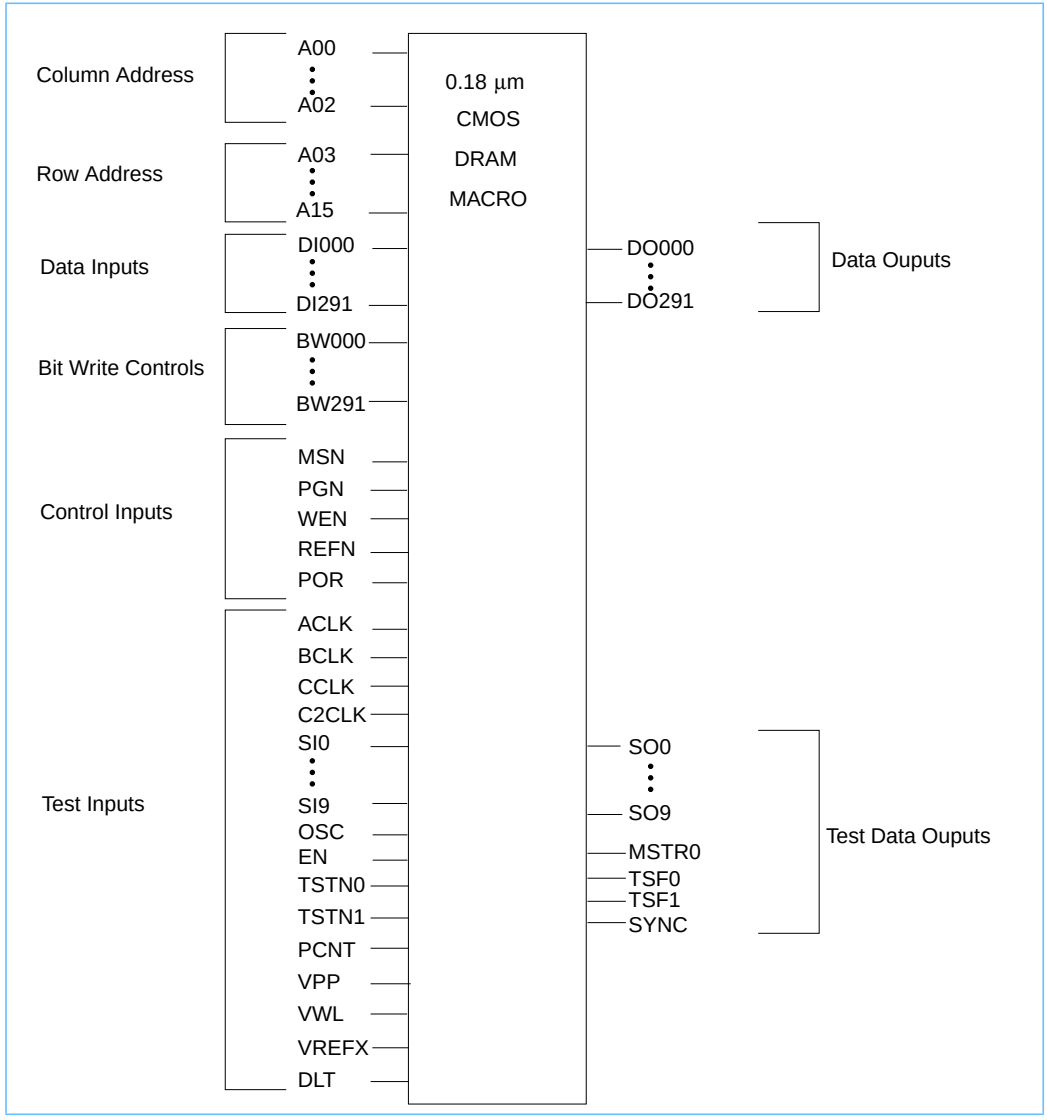


Figure 6. x 292 Configuration



Electrical Characteristics

Table 27. Power Supply Current Characteristics

Condition		x 256 Configuration		x 292 Configuration	
		Active Current[1]	Standby Current	Active Current[1]	Standby Current
Random access	No data changing	60 mA	2 mA	60 mA	2 mA
	All data changing	60 mA + 2.2 mA per Mb		60 mA + 2.5 mA per Mb	
Page access	No data changing	5.5 mA		5.5 mA	
	All data changing	5.5 mA + 7 mA per Mb		5.5 mA + 8.0 mA per Mb	

1. Does not include data out current.
2. Active and standby currents are specified on a per macro basis.

Table 28. AC Parameters

Parameter	Symbol	x 256 Configuration		x 292 Configuration		Units
		Min	Max	Min	Max	
Input setup to MSN/PGN[1]	T_{set}	2	—	2	—	ns
Input hold to MSN/PGN[1]	T_{hld}	3	—	3	—	ns
Random access time	T_{acc}	3.8	13.3	3.8	13.3	ns
MSN active time	T_{act}	13.3	100K	13.3	100K	ns
MSN restore time	T_{res}	6.6	—	6.6	—	ns

1. All input set up and hold times are specified with respect to either MSN (random cycle) or PGN (page cycle).
2. The PGN cycle time and MSN and PGN delay must be chosen to allow a sufficient data output window.
3. The T_{actp} parameter is dependent on the number of page cycles (T_{pcyc}) performed during MSN active time.
4. *W* refresh cycles must be issued within 3.2 ms, where *W* is the total number of word addresses in the macro.
5. A POR cycle must be performed anytime the chip power supply falls below the specified minimum.
6. Signal rise and fall times to the macro are assumed to be ≤ 0.2 ns.

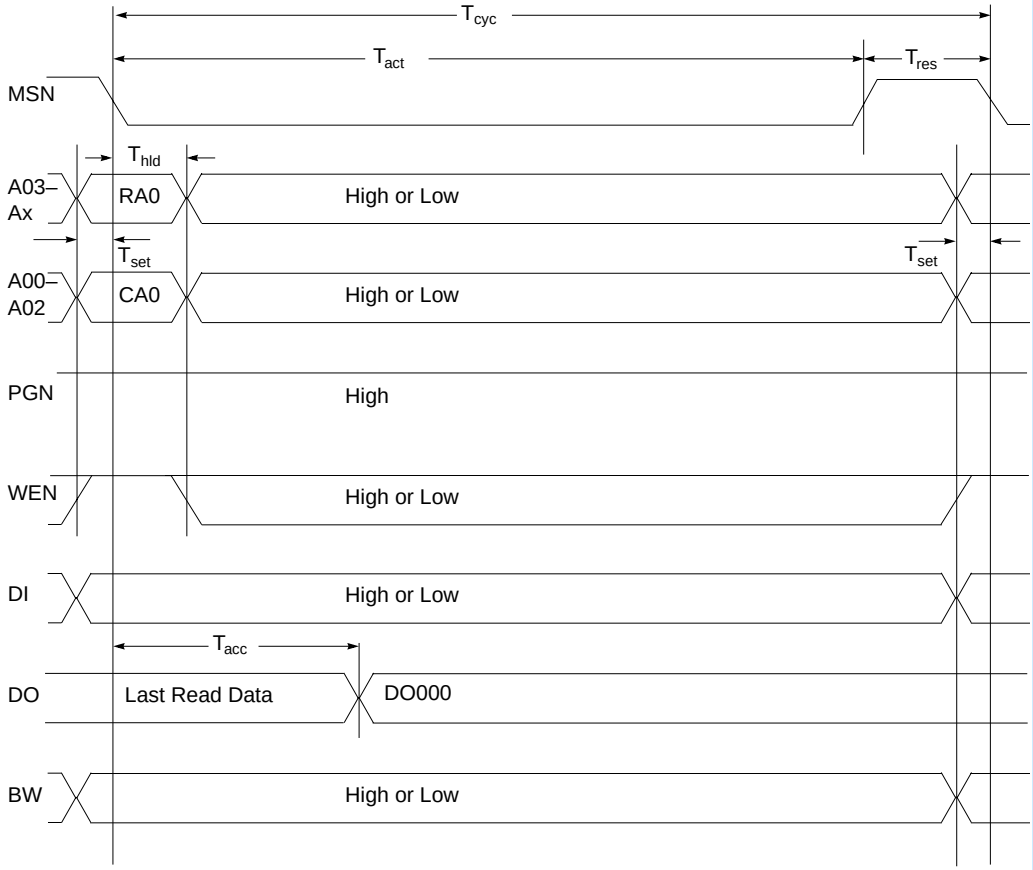
Table 28. AC Parameters (Continued)

Parameter	Symbol	x 256 Configuration		x 292 Configuration		Units
		Min	Max	Min	Max	
Random R/W cycle time	T_{cyc}	20	—	20	—	ns
Page mode access time	T_{accp}	1.4	6.6	1.4	6.6	ns
PGN active time	T_{pa}	3	—	3	—	ns
PGN restore time	T_{pr}	3	—	3	—	ns
PGN cycle time[2]	T_{pcyc}	6.6	—	6.6	—	ns
MSN to PGN delay[2]	T_{mpd}	13	—	13	—	ns
MSN active for page mode[3]	T_{actp}	20	—	20	—	ns
Refresh period[4]	T_{ref}	—	3.2	—	3.2	ms
Page active to MSN restore	T_{pamr}	6.6	—	6.6	—	ns
Page restore to MSN active	T_{prma}	2	—	2	—	ns
Power-on-reset delay[5]	T_{pord}	200	—	200	—	µs
POR to MSN delay[5]	T_{porm}	100	—	100	—	µs
Power-on-reset width[5]	T_{porw}	100	—	100	—	µs

1. All input set up and hold times are specified with respect to either MSN (random cycle) or PGN (page cycle).
2. The PGN cycle time and MSN and PGN delay must be chosen to allow a sufficient data output window.
3. The T_{actp} parameter is dependent on the number of page cycles (T_{pcyc}) performed during MSN active time.
4. *W* refresh cycles must be issued within 3.2 ms, where *W* is the total number of word addresses in the macro.
5. A POR cycle must be performed anytime the chip power supply falls below the specified minimum.
6. Signal rise and fall times to the macro are assumed to be ≤ 0.2 ns.

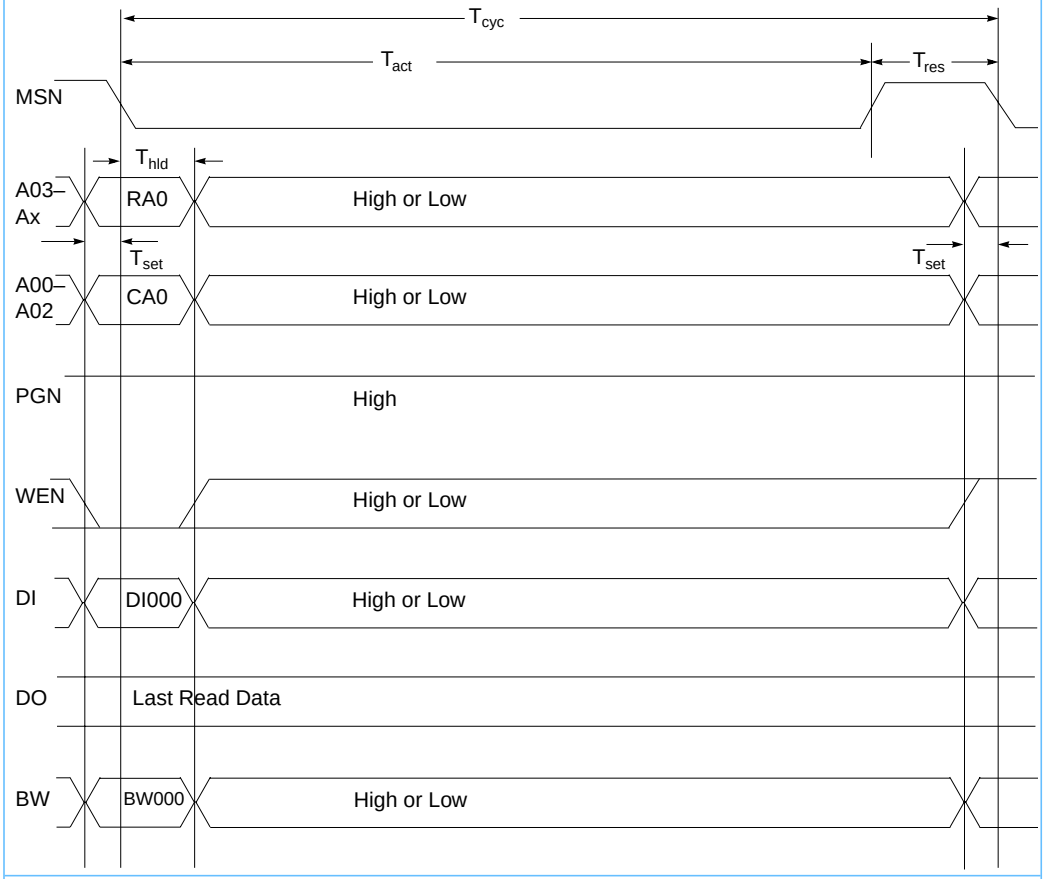
Timing Diagrams

Figure 7. Single Read



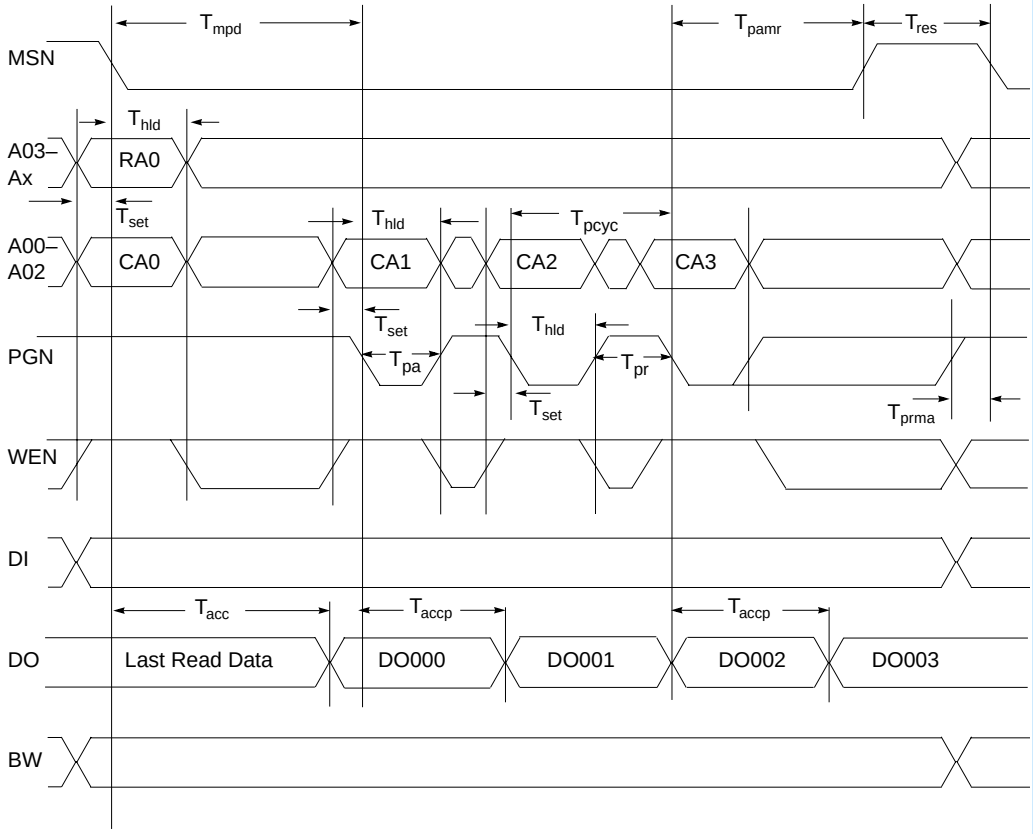
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 8. Single Write



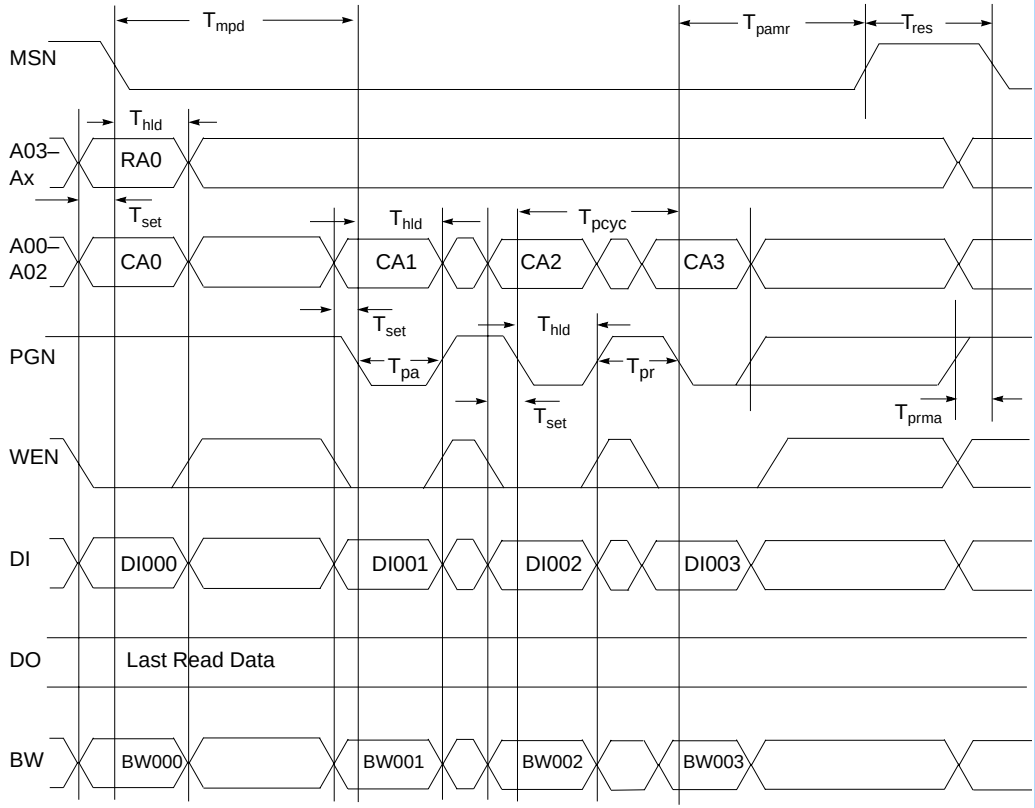
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 9. Page Mode Read Cycle



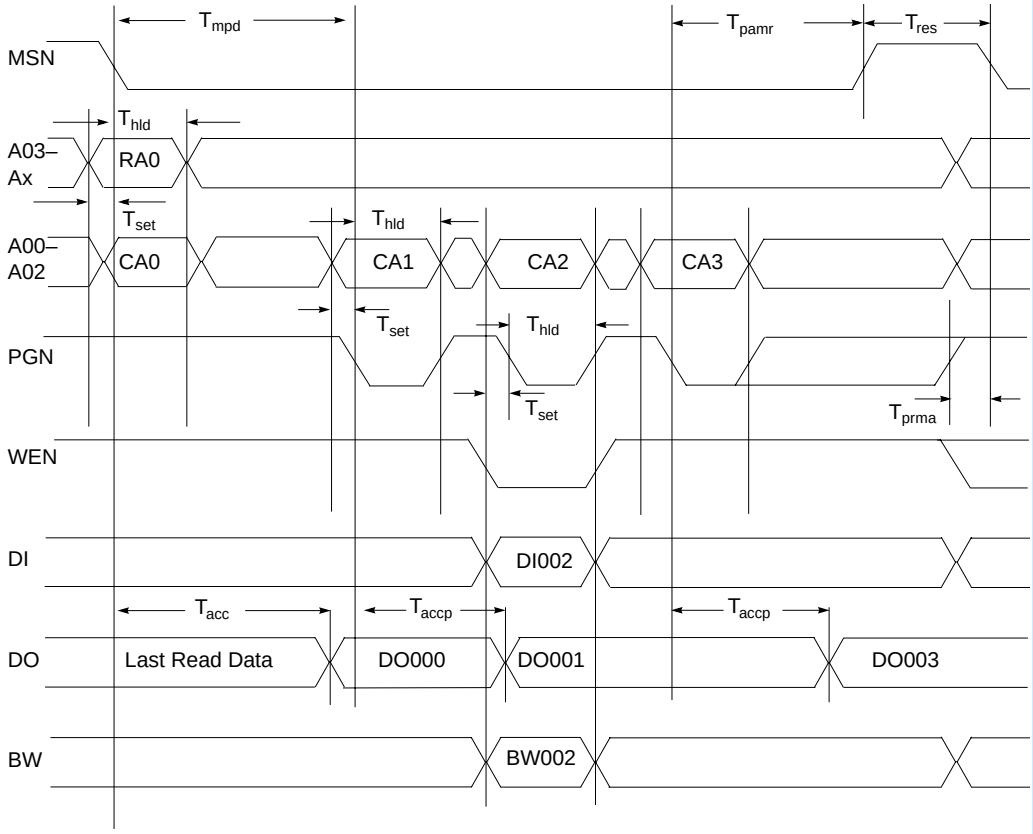
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 10. Page Mode Write Cycle



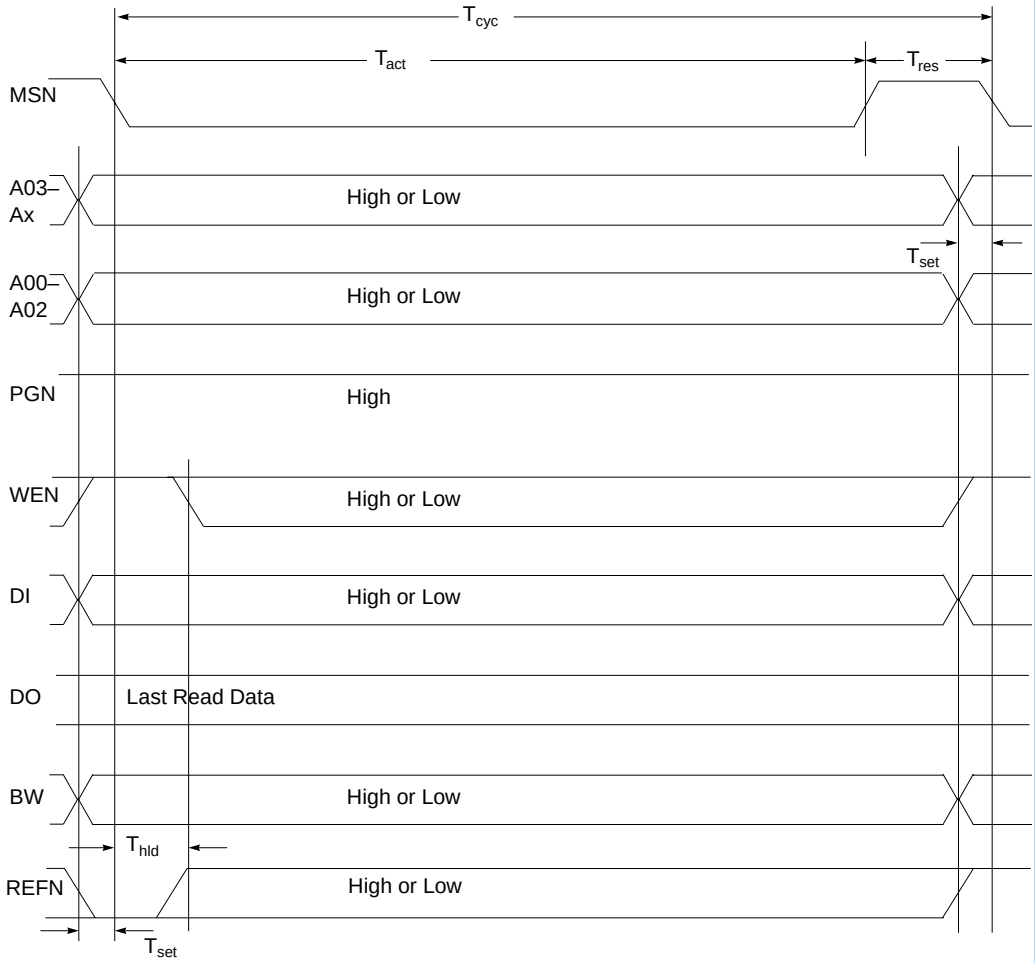
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 11. Page Mode - Read Write Read Cycle



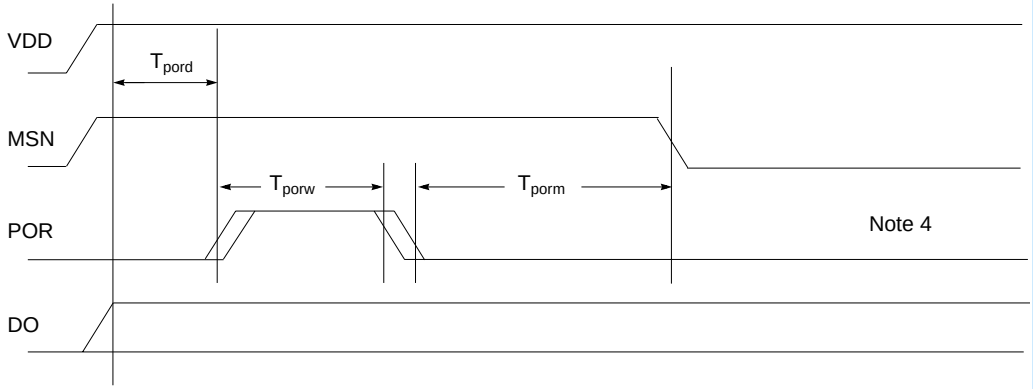
1. All inputs should stay at valid signal levels and not switch unnecessarily.
2. REFN high during all cycles except refresh.

Figure 12. Refresh Cycle



1. All inputs should stay at valid signal levels and not switch unnecessarily.

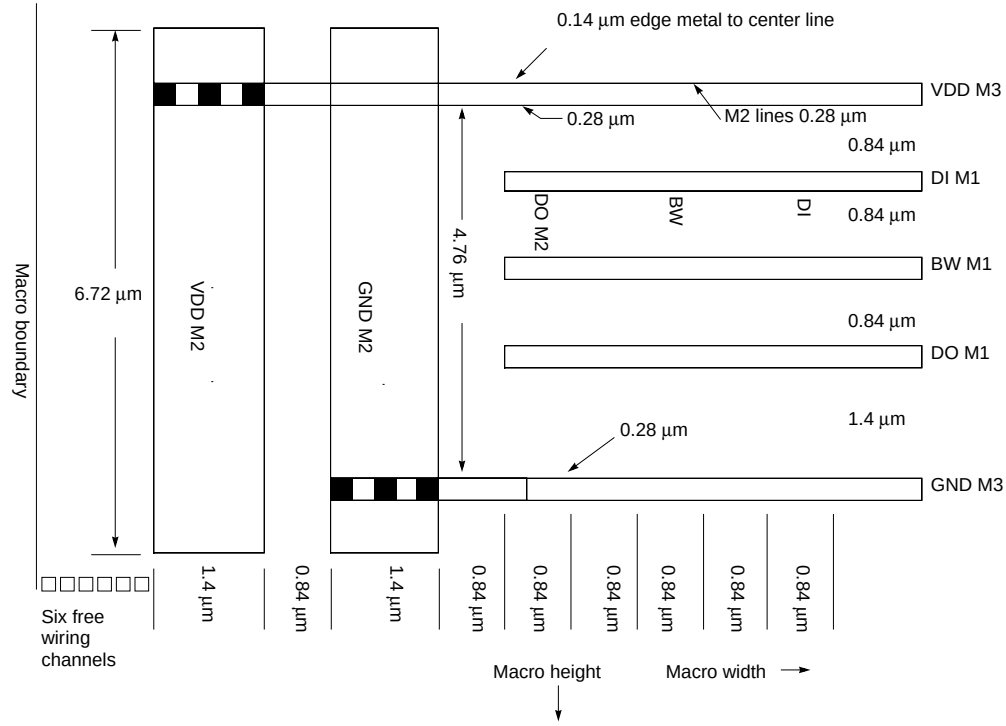
Figure 13. Power-on-reset (POR) Cycle



1. Initial state of DO pins after power up will be a valid high or low, but which binary state will occur is unpredictable.
2. A POR cycle must be performed before using the DRAM macro anytime the chip power supply (V_{dd}) falls below the specified minimum allowable level. The POR pulse must not begin until a minimum of T_{pord} time after VDD has reached its operating level and MSN has reached its inactive state.
3. The first MSN activation edge must not occur until T_{porm} time after the fall of the POR pulse.
4. After the POR cycle, during normal operation, the POR pin remains low.

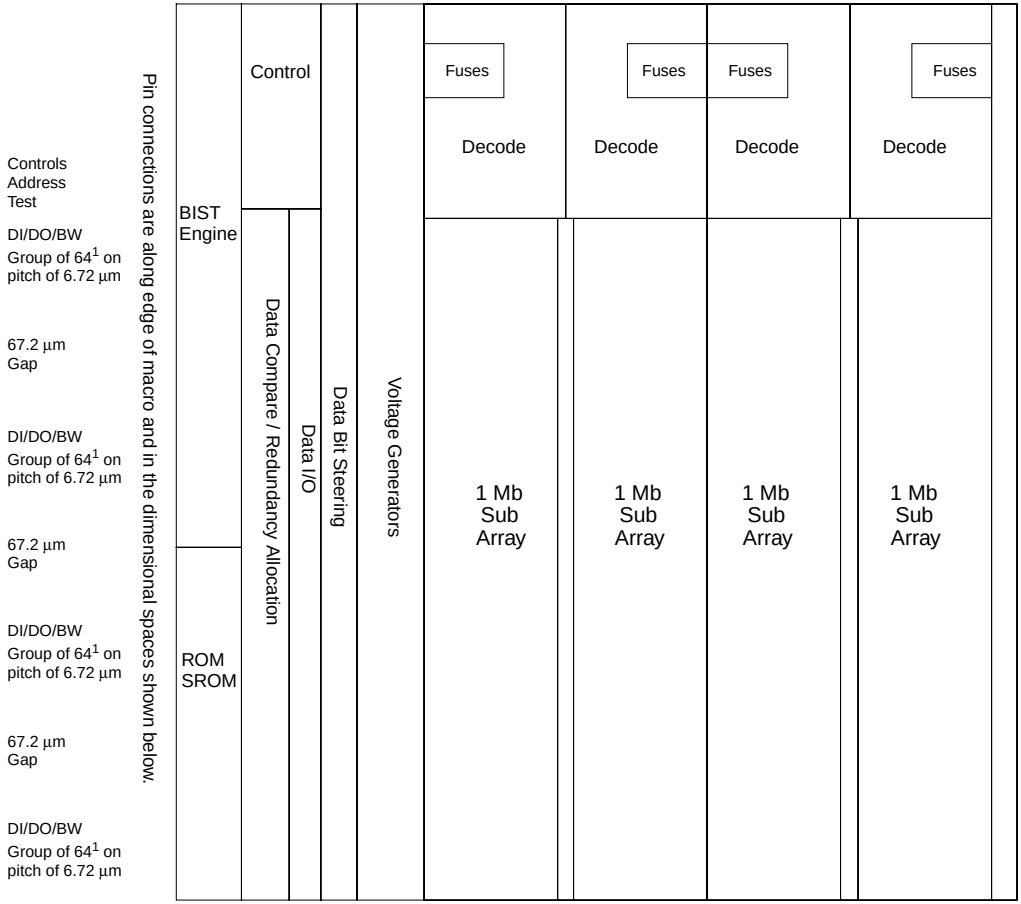
Pin Connections

Figure 14. Pin Connection of DO, DI, and BW at Edge of Macro



1. For design considerations, the macro boundary power buses use five wiring channels versus the standard IBM ASIC methodology of four wiring channels.
2. Dimensions based on a 0.56 µm logic grid.
3. GDSII data is available upon request.
4. Metal wiring directions: M2, M4 ↓
   M1, M3 →

Figure 15. 4Mb DRAM Macro



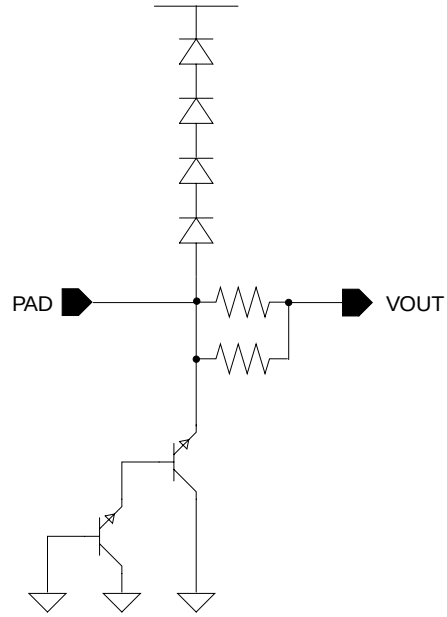
1. The x 292 configuration is in groups of 73 on a pitch of 6.72 µm.

Cell: DRAMVPP, DRAMVPP_PM

Function: Fat Wire Analog Receiver/Driver for Embedded DRAM Analog Inputs

Description:

Provides analog low-impedance pad connection to embedded DRAM test inputs requiring voltages as high as V_{dd} + 1.8V and as low as GND - 1.2V.



Truth Table

Input	Output
PAD	**VOUT**
0	0
1	1
Hi-Z	Hi-Z

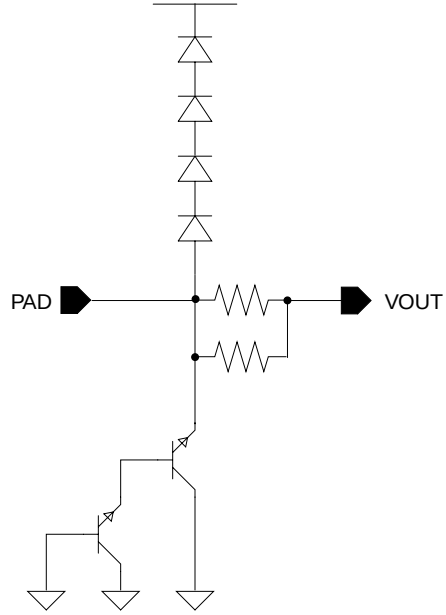
Performance Level	Cell Units
A	1 cell

Cell: DRAMVREFX, DRAMVREFX_PM

Function: Fat Wire Analog Receiver/Driver for Embedded DRAM Analog Inputs

Description:

Provides analog low-impedance pad connection to embedded DRAM test inputs requiring voltages as high as V_{dd} + 1.8V and as low as GND - 1.2V.



Truth Table

Input	Output
PAD	**VOUT**
0	0
1	1
Hi-Z	Hi-Z

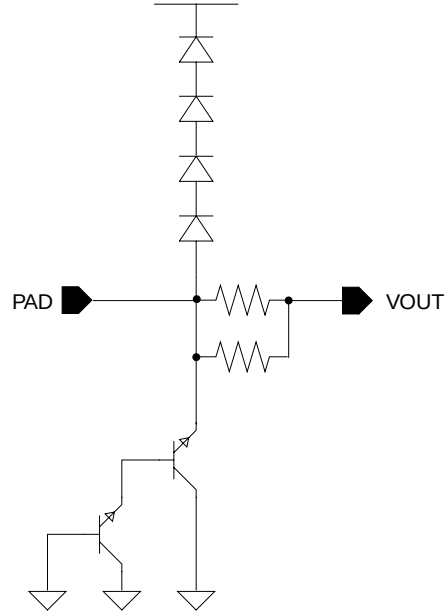
Performance Level	Cell Units
A	1 cell

Cell: DRAMVWL, DRAMVWL_PM

Function: Fat Wire Analog Receiver/Driver for Embedded DRAM Analog Inputs

Description:

Provides analog low-impedance pad connection to embedded DRAM test inputs requiring voltages as high as V_{dd} + 1.8V and as low as GND - 1.2V.



Truth Table

Input	Output
PAD	**VOUT**
0	0
1	1
Hi-Z	Hi-Z

Performance Level	Cell Units
A	1 cell

Compilable Memory Arrays

SRAM1G—Compilable One-Port SRAM

Features

- Fully static array
- Configurations up to 32K words or 128 bits supported
- One read and write port
- Multiple decode options for performance and area optimization
- Latched output data until next read cycle
- Bit write control for data masking
- Multiple array built-in self-test
- Single clock edge operation through use of self-timed restore

The key features of the macro are summarized in Table 29.

Table 29. SRAM1G One-Port SRAM Features

Feature	Capability
Supported V_{dd} range	1.20V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1,16:1, or 32:1
Maximum macro size	1M (1,048,576) bits
Maximum words	32,768 words
Minimum words	64 words
Maximum data width	128 bits
Minimum data width	8 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	60%

Valid Array Sizes

To limit the maximum bitline and wordline lengths in the cell array, reduce array power dissipation, and support up to 1Mb macros, the largest macros can be divided into subarrays. Small arrays requiring up to 64 wordlines will be implemented with one subarray to optimize the control area versus array area. For 96 to 512 wordlines, either one or two subarrays can be used, allowing trade-offs between macro area and performance. Above 512 wordlines, two subarrays must be used to limit the loading on the array bitlines. The array wordlines are limited to a maximum width of 1024 cell columns.

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, DECODE, and NARRAY options are given in Table 30.

Table 30. SRAM1G Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–32768	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 31, “Valid SRAM1G Configurations,” on page 83.
NBIT	8–128	The number of bits per word in the array.
DECODE	4, 8, 16, or 32	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array decreases and the width (X) of the array increases.
NARRAY	1 or 2	The number of subarrays used in the array, limited by: NARRAY = 1 if (NWORD/DECODE) < 96; NARRAY = 1 or 2 if 96 ≤ (NWORD/DECODE) ≤ 512; NARRAY = 2 if 512 < (NWORD/DECODE).

The resultant ranges of valid array configurations are shown in Table 31.

Table 31. Valid SRAM1G Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	64	1024	64	8	128
		1152	2048	128	8	128
	2	384	2048	128	8	128
		2304	4096	256	8	128
8	1	128	2048	128	8	128
		2304	4096	256	8	128
	2	768	4096	256	8	128
		4608	8192	512	8	128
16	1	256	4096	256	8	64
		4608	8192	512	8	64
	2	1536	8192	512	8	64
		9216	16384	1024	8	64
32	1	512	8192	512	8	32
		9216	16384	1024	8	32
	2	3072	16384	1024	8	32
		18432	32768	2048	8	32

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 31, “Valid SRAM1G Configurations”.

If the array is clocked with an address larger than NWORD applied at the address input port, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

Global M2 Wiring Porosity

SRAM1G has no global M2 porosity and approximately 60% M3 porosity over the array.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM1GwwwwwXbbbDddSsM1

where:

SRAM1G	=	one-port SRAM name
w	=	total number of words: 5 digits
b	=	data width in bits: 3 digits
d	=	decode option: 2 digits
s	=	subarray option: 1 digit
M1	=	array clocked timing mode only

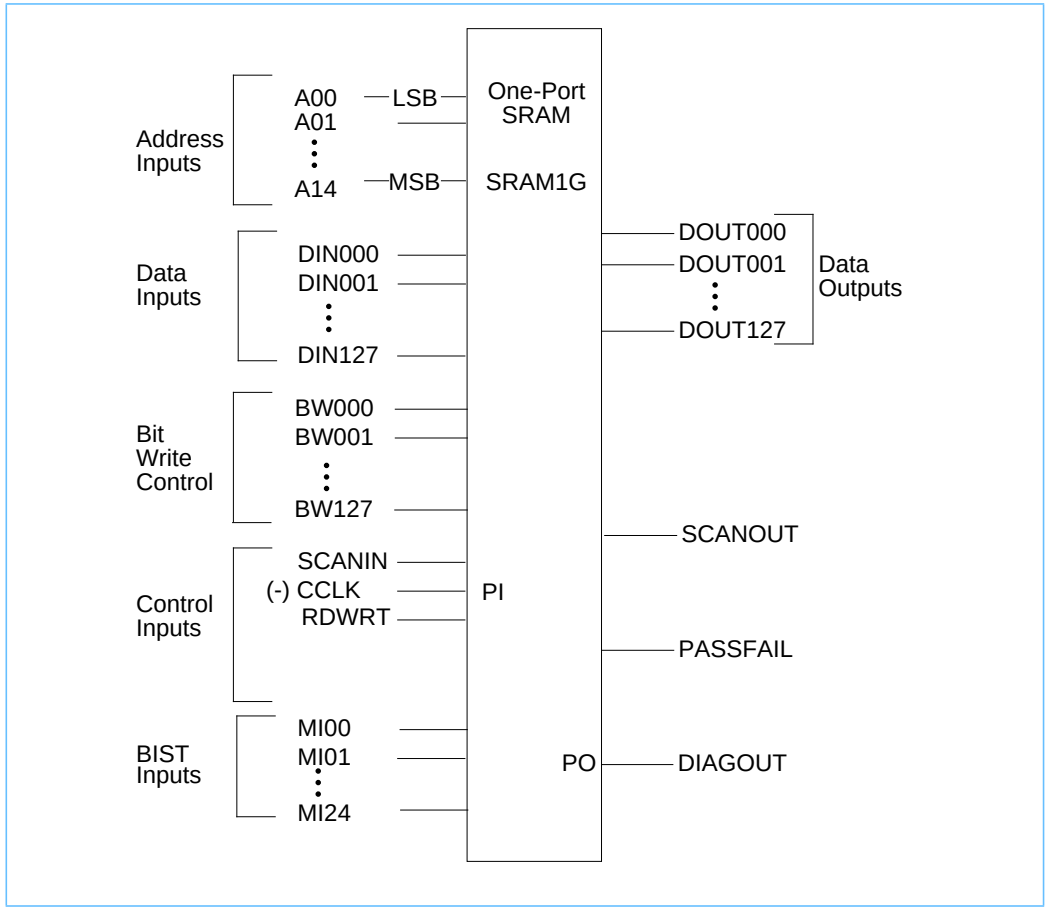
A representative example would be:

SRAM1G01024X008D16S1M1	A 1024-word x 8-bit one-port SRAM, using the 16:1 decode option and one subarray.

Logical Description

A symbolic representation of the one-port SRAM is shown in Figure 16.

Figure 16. SRAM1G One-Port SRAM Logic Symbol



Pin Definitions

Table 32 summarizes the function and proper usage of the macro pins shown in Figure 16 on page 85. The control and input pins must be stable before the clocks initiate a read or write access of the array. Pin timing relationships are described later.

Table 32. Pin Definitions

Pin	Description
A00–A14	The address input pins define the address from or to which data will be read or written. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation words = 2^N. The bit address occupies the least significant bits, using: A00 and A01 for decode = 4:1; A00, A01 and A02 for decode = 8:1; A00, A01, A02, and A03 for decode =16:1; or A00, A01, A02, A03, and A04 for decode = 32:1. The word address follows. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
DIN000–DIN127	The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the DIN000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
BW000–BW127	The bit write control input pins are active high, and one pin is required for each data input bit. The bit write control pins allow masking of the input data. If the pin is held high, the corresponding data input bit is written into the array. If the pin is held low, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pins are used starting at the BW000 least significant bit and counting upwards. If a data input pin is not used, then the corresponding bit write control pin will not appear in the logical or physical models either. However, a bit write control pin is always allocated for every data input pin used. If bit write control is not required, then these pins must be tied high.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
CCLK	The C clock pin initiates a read or write access of the SRAM on its falling edge during functional mode operations. This pin must come from a primary input.
RDWRT	The read/write control pin causes a read of the array to be performed when held high or a write to be performed when held low when the C clock is strobed active.

Table 32. Pin Definitions (Continued)

Pin	Description
MI00–MI24	The BIST pins must be connected to an accompanying BIST1 controller as they control the SRAM during BIST testing. The number required is fixed at 25. The MInn pins must not be connected to anything other than the BIST1 controller.
DOUT000–DOUT127	The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the DOUT000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read. Write operations do not affect the data output pins.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during BIST testing and must be routed to the accompanying BIST1 controller for the array. The PASSFAIL pin must not be connected to anything other than the BIST1 controller. Note that this pin is “nonvalidated” and thus cannot be monitored directly to determine if there are fails in the array. The BIST1 controller “validates” the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

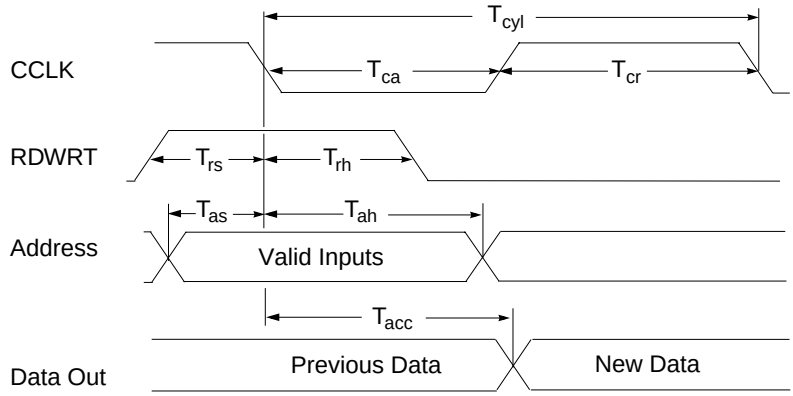
Array functional operation is the normal operation of the SRAM when the BIST1G controller is inactive. Array functional operations include read and write.

Array Clocking Modes

Array Clocked Read

- RDWRT held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is read from the address in the array.
- Data appears at the data out pins after the access time has elapsed.
- Data out is valid until the next read cycle.

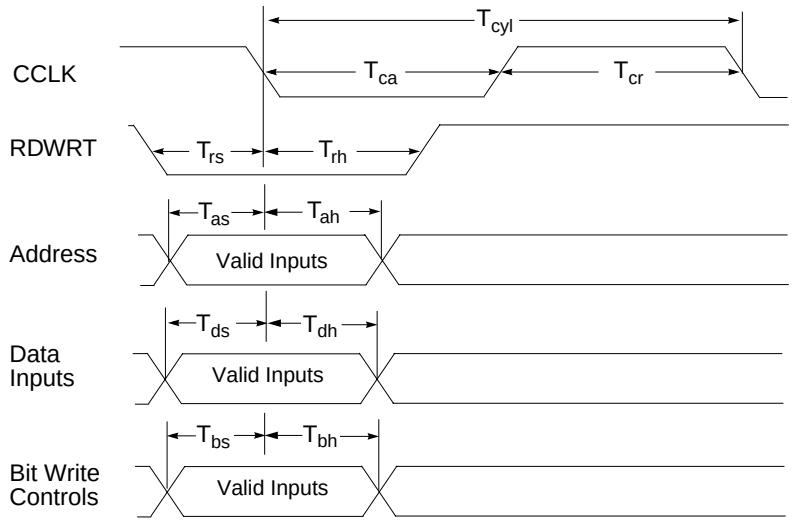
Figure 17. Array Clocked Read Timing



Array Clocked Write

- RDWRT held low or brought low before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is written into the address in the array.
- Data out does not change during a write cycle.

Figure 18. Array Clocked Write Timing



Delay Definitions

Table 33 and Table 34 show setup and hold times for representative “small” and “large” SRAM1G arrays.

Table 33. “Small” SRAM1G00064X016D04S1

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.0
CCLK minimum restore time	T_{cr}	1.1
RDWRT setup time	T_{rs}	0.1
RDWRT hold time	T_{rh}	0.5
Data in setup time	T_{ds}	-0.1
Data in hold time	T_{dh}	0.6
Bit write setup time	T_{bs}	-0.1
Bit write hold time	T_{bh}	0.6
Address setup time	T_{as}	0.7
Address hold time	T_{ah}	1.0
Access time	T_{acc}	1.8
Cycle time	T_{cyl}	2.3

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 34. “Large” SRAM1G32768X032D32S2

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.4
CCLK minimum restore time	T_{cr}	2.0
RDWRT setup time	T_{rs}	0.1
RDWRT hold time	T_{rh}	0.6
Data in setup time	T_{ds}	-0.1
Data in hold time	T_{dh}	0.9
Bit write setup time	T_{bs}	-0.1
Bit write hold time	T_{bh}	0.9
Address setup time	T_{as}	0.7
Address hold time	T_{ah}	2.2
Access time	T_{acc}	3.5
Cycle time	T_{cyl}	4.3

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the SRAM1G power consumption for a particular application, use the following equation:

$$P = (A_{read} \times RC_{int} + A_{write} \times WC_{int}) \times V^2_{dd} \times F_{RAM}$$

where:

- P = Power in microwatts.
- RC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a read access on every cycle. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a write access on every cycle.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read access is performed (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- A_{write} = Write activity factor, which is the fraction of the total clock cycles that a write access is performed (a value between 0 and 1). In typical applications, the write activity is often less than the read activity, as the contents of an SRAM are read more often than they are replaced. The sum of (A_{read} + A_{write}) must be less than or equal to 1.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{RAM} = Clock frequency applied to the SRAM, in MHz.

Array Area and Footprint

Figure 19 shows the general shape of the SRAM and the relative locations of the pins within it. The dimensions for a representative configuration can be obtained from the sizing routines available on the World Wide Web. Access to the Web page can be obtained from an IBM ASICs representative.

Figure 19. SRAM1G Footprint

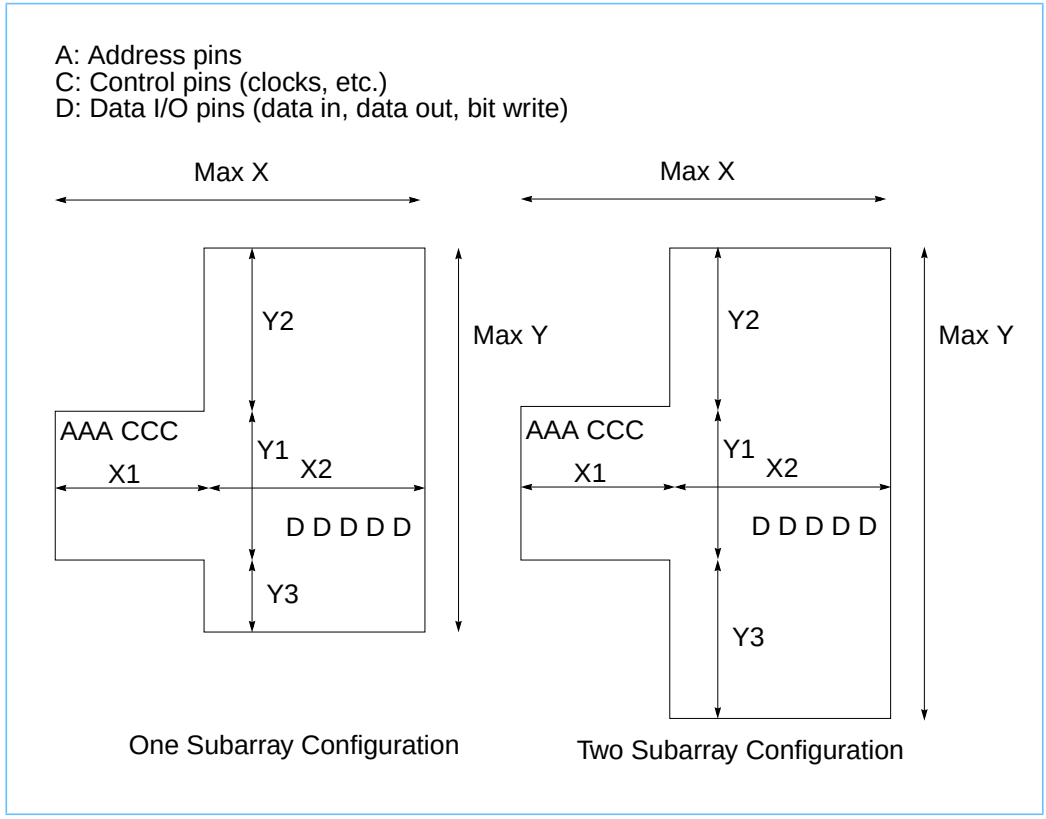


Table 35. SRAM1G Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Sub	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Write Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
256 x 16	4	1	1.9	2.3	44	39	23887	416	60
256 x 32	4	1	1.9	2.3	68	60	38527	660	60
256 x 64	4	1	2.0	2.5	116	101	67807	1148	60
256 x 128	4	1	2.1	2.6	212	182	126367	2124	60
1024 x 16	8	1	2.0	2.5	55	52	54102	660	85
1024 x 32	8	1	2.1	2.5	88	81	95582	1148	85
1024 x 64	4	1	2.5	3.0	133	128	152243	1148	136
1024 x 128	4	1	2.6	3.0	233	223	284979	2124	136
4096 x 16	16	1	2.5	3.0	84	81	152243	1148	136
4096 x 32	16	1	2.6	3.0	138	133	284979	2124	136
4096 x 64	8	1	3.2	4.3	198	206	499940	2124	239
4096 x 128	8	1	3.4	4.4	347	362	966468	4076	239
16384 x 16	32	1	3.2	4.3	151	149	499940	2124	239
16384 x 32	16	2	3.2	4.3	179	177	965896	2124	462
16384 x 64	16	2	3.4	4.4	302	298	1867720	4076	462
32768 x 16	32	2	3.2	4.3	162	157	965896	2124	462
32768 x 32	32	2	3.4	4.4	269	260	1867720	4076	462

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read or write operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the SRAM and can be calculated using the following equation:

Total scan latches = 14 + NBIT (the data word width)

The last bits in the scan chain are the data out bits, with the most significant data out bit being in the (nth - 1) scan latch. The nth scan latch drives the SCANOUT, DIAGOUT, and PASSFAIL output pins.

Multiple Array BIST Testing

MABIST Controller Interface

Every instance of an SRAM1G array on a chip must be connected to a BIST1G controller. Up to 16 SRAM1G arrays can be connected to a single BIST1G controller.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

SRAM1A—Compilable One-Port SRAM for Low Voltage

Features

SRAM1A is physically and logically identical to the SRAM1G compilable one-port SRAM. The models and technical data for SRAM1A are SRAM1G compiler copies. SRAM1A is a separate entity only to distinguish that the design has been modified to support a lower operating voltage, down to 0.90V.

The key features of the macro are summarized in Table 36.

Table 36. SRAM1A One-Port SRAM Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1,16:1, or 32:1
Maximum macro size	1M (1,048,576) bits
Maximum words	32,768 words
Minimum words	64 words
Maximum data width	128 bits
Minimum data width	8 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	60%

Valid Array Sizes

To limit the maximum bitline and wordline lengths in the cell array, reduce array power dissipation, and support up to 1Mb macros, the largest macros can be divided into subarrays. Small arrays requiring up to 64 wordlines will be implemented with one subarray to optimize the control area versus array area. For 96 to 512 wordlines, either one or two subarrays can be used, allowing trade-offs between macro area and performance. Above 512 wordlines, two subarrays must be used to limit the loading on the array bitlines. The array wordlines are limited to a maximum width of 1024 cell columns.

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, DECODE, and NARRAY options are given in Table 37.

Table 37. SRAM1A Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–32768	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 38, “Valid SRAM1A Configurations,” on page 98.
NBIT	8–128	The number of bits per word in the array.
DECODE	4, 8, 16, or 32	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array decreases and the width (X) of the array increases.
NARRAY	1 or 2	The number of subarrays used in the array, limited by: NARRAY = 1 if (NWORD/DECODE) < 96; NARRAY = 1 or 2 if 96 ≤ (NWORD/DECODE) ≤ 512; NARRAY = 2 if 512 < (NWORD/DECODE).

The resultant ranges of valid array configurations are shown in Table 38.

Table 38. Valid SRAM1A Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	64	1024	64	8	128
		1152	2048	128	8	128
	2	384	2048	128	8	128
		2304	4096	256	8	128
8	1	128	2048	128	8	128
		2304	4096	256	8	128
	2	768	4096	256	8	128
		4608	8192	512	8	128
16	1	256	4096	256	8	64
		4608	8192	512	8	64
	2	1536	8192	512	8	64
		9216	16384	1024	8	64
32	1	512	8192	512	8	32
		9216	16384	1024	8	32
	2	3072	16384	1024	8	32
		18432	32768	2048	8	32

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 38, “Valid SRAM1A Configurations”.

If the array is clocked with an address larger than NWORD applied at the address input port, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM1AwwwwwXbbbDddSsM1

where:

SRAM1A	=	one-port SRAM name
w	=	total number of words: 5 digits
b	=	data width in bits: 3 digits
d	=	decode option: 2 digits
s	=	subarray option: 1 digit
M1	=	array clocked timing mode only

A representative example would be:

SRAM1A01024X008D16S1M1	A 1024-word x 8-bit one-port SRAM, using the 16:1 decode option and one subarray.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Multiple Array BIST Testing

MABIST Controller Interface

Every instance of an SRAM1A array on a chip must be connected to a BIST1G controller. Up to 16 one-port SRAM arrays can be connected to a single BIST1G controller.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

SRAM1LG—Compilable Low Power One-Port SRAM

Features

- Fully static array
- Configurations up to 16K words supported
- One read and write port
- Multiple decode options for performance and area optimization
- Latched output data until next read cycle
- Byte write control for data masking
- Multiple array built-in self-test
- Single clock edge operation through use of self-timed restore

The key features of the macro are summarized in Table 39.

Table 39. SRAM1LG One-Port SRAM Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1,16:1, or 32:1
Maximum macro size	256K (294,912) bits
Maximum words	16,384 words
Minimum words	64 words
Maximum data width	36 bits
Minimum data width	8 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	60%

Valid Array Sizes

In order to minimize the power dissipation of this SRAM, the memory cell array is divided into small subarrays which are grouped around the central control section of the array. During a read or write access of the SRAM, only one of these subarrays will be activated. Numerous configuration options as a function of decode, number of subarrays, and quadrants are allowed for optimizing the area and aspect ratio of the array. If DECODE > 4, the minimum number of wordlines per subarray, given by ((NWORD/DECODE)/QUAD), must be equal to or greater than 128 in order to maximize the efficiency in growing the subarrays.

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, DECODE, NSUB, NQUAD, and NBYTE options are given in Table 40.

Table 40. SRAM1LG Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–16384	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 41, “SRAM1LG Valid Configuration Ranges,” on page 104.
NBIT	8–36	The number of bits per word in the array, limited to 8 ≤ NBIT ≤ 36. If 8 ≤ NBIT ≤ 32, NBYTE = 8 or 9. If 33 ≤ NBIT ≤ 36, NBYTE = 9.
DECODE	4, 8, 16, or 32	The number of memory cell columns that are decoded into one data output bit, times the number of subarrays. This parameter is defined for consistency with the other IBM ASIC SRAMs so that the same MABIST control methodology can be used.
NSUB	2, 4, or 8	The number of subarrays in each quadrant.
NQUAD	1 or 2	The number of quadrants in the array.

Table 40. SRAM1LG Keyword Parameter Ranges (Continued)

Keyword	Allowed Values	Description
NBYTE	8 or 9	The number of data input bits masked by each byte write control pin. The byte write (BW) to data in (DIN) pin relationships are: If NBYTE = 8: BW000 controls DIN000–DIN007 BW001 controls DIN008–DIN015 BW002 controls DIN016–DIN023 BW003 controls DIN024–DIN031 If NBYTE = 9: BW000 controls DIN000–DIN008 BW001 controls DIN009–DIN017 BW002 controls DIN018–DIN026 BW003 controls DIN027–DIN035

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 41, “SRAM1LG Valid Configuration Ranges”.

If the array is clocked with an address larger than NWORD applied at the address input port, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

The resultant ranges of valid array configurations are shown in Table 41.

Table 41. SRAM1LG Valid Configuration Ranges

Decode	Subarray	Quad	Word Depth		Word Depth Granularity	Data Width	
			Min	Max		Min	Max
4	2	1	64	1024	64	8	36 (or 32)[1]
		2	128	2048	128	8	36 (or 32)[1]
8	4	1	1024	2048	128	8	36 (or 32)[1]
		2	2048	4096	256	8	36 (or 32)[1]
16	8	1	2048	4096	256	8	36 (or 32)[1]
		2	4096	8192	512	8	36 (or 32)[1]
8	2	1	1024	2048	128	8	18
		2	2048	4096	256	8	18
16	4	1	2048	4096	256	8	18
		2	4096	8192	512	8	18
32	8	1	4096	8192	512	8	18
		2	8192	16384	1024	8	18

1. If data bit width is NBIT ≤ 32, NBYTE = 8 or 9. For data bit widths 33 ≤ NBIT ≤ 36, NBYTE = 9.

Global M2 Wiring Porosity

SRAM1LG has no global M2 porosity and approximately 60% M3 porosity over the array.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM1LGwwwwwXbbbByDddSsQqM1

where:

SRAM1LG	=	low power one-port SRAM name
w	=	total number of words: 5 digits
b	=	data width in bits: 3 digits
y	=	byte write data width option: 1 digit
d	=	decode option: 2 digits
s	=	subarray option: 1 digit
q	=	quadrant option: 1 digit
M1	=	array clocked timing mode only

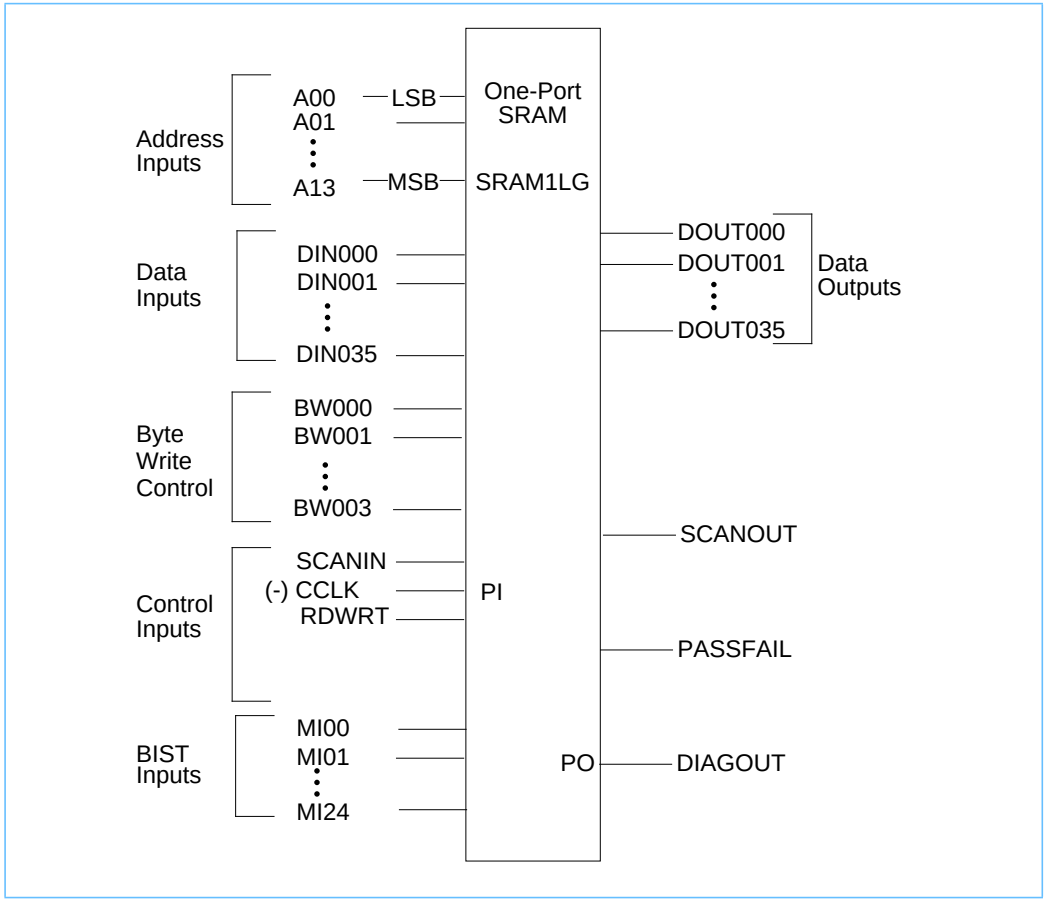
A representative example would be:

SRAM1LG01024X032B8D04S2Q2M1	A 1024-word x 32-bit one-port SRAM, using the 4:1 decode option with two subarrays each in two quadrants. Byte write is configured for 8-bit wide bytes.

Logical Description

A symbolic representation of the one-port SRAM is shown in Figure 20.

Figure 20. SRAM1LG One-Port SRAM Logic Symbol



Pin Definitions

Table 42 summarizes the function and proper usage of the macro pins shown in Figure 20 on page 106. The control and input pins must be stable before the clocks initiate a read or write access of the array. Pin timing relationships are described later.

Table 42. Pin Definitions

Pin	Description
A00–A13	The address input pins define the address from or to which data will be read or written. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation words = 2^N. The bit address occupies least significant bits A0 and A1; the subarray address follows, using A02, A03, and A04; the low-order word address is next, occupying A05, A06, A07, and A08; the quadrant address follows, using A09; the upper word address uses A10, A11, A12, and A13. The minimum address configuration requires one bit address, one subarray address, and four low-order word addresses. Unused address pins will not appear in the logical or physical models and therefore no tie-off procedure is required.
DIN000–DIN035	The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the DIN000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
BW000–BW003	The byte write control input pins are active high, and allow masking of the input data in byte-wide groups. If the pin is held high, the corresponding data input bits are written into the array. If the pin is held low, the corresponding data input bits are ignored, and the array retains its previous contents for those bits. The byte write control input pins perform no function during a read of the array. Pins are used starting at the BW000 least significant bit and counting upwards. If a data input pin is not used, then the corresponding byte write control pin will not appear in the logical or physical models either. However, a byte write control pin is always allocated for every data input pin used. If byte write control is not required, then these pins must be tied high.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
CCLK	The C clock pin initiates a read or write access of the SRAM on its falling edge during functional mode operations. This pin must come from a primary input.
RDWRT	The read/write control pin causes a read of the array to be performed when held high or a write to be performed when held low when the C clock is strobed active.

Table 42. Pin Definitions (Continued)

Pin	Description
MI00–MI24	The BIST pins must be connected to an accompanying BIST1 controller as they control the SRAM during BIST testing. The number required is fixed at 25. The MInn pins must not be connected to anything other than the BIST1 controller.
DOUT000–DOUT035	The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the DOUT000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read. Write operations do not affect the data output pins.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during BIST testing and must be routed to the accompanying BIST1 controller for the array. The PASSFAIL pin must not be connected to anything other than the BIST1 controller. Note that this pin is “nonvalidated” and thus cannot be monitored directly to determine if there are fails in the array. The BIST1 controller “validates” the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

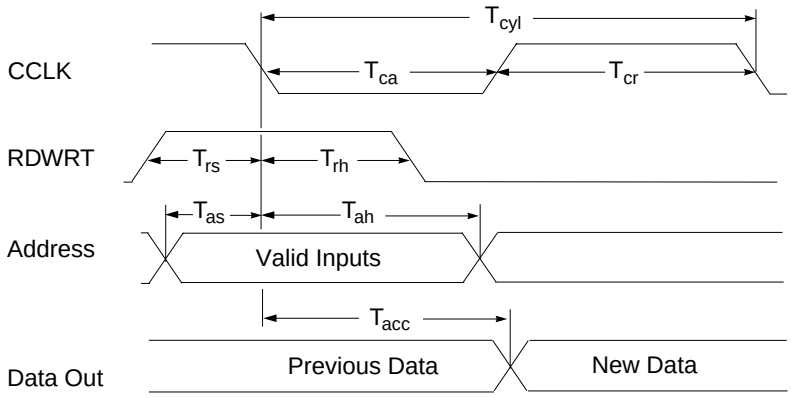
Array functional operation is the normal operation of the SRAM when the BIST1 controller is inactive. Array functional operations include read and write.

Array Clocking Modes

Array Clocked Read

- RDWRT held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is read from the address in the array.
- Data appears at the data out pins after the access time has elapsed.
- Data out is valid until the next read cycle.

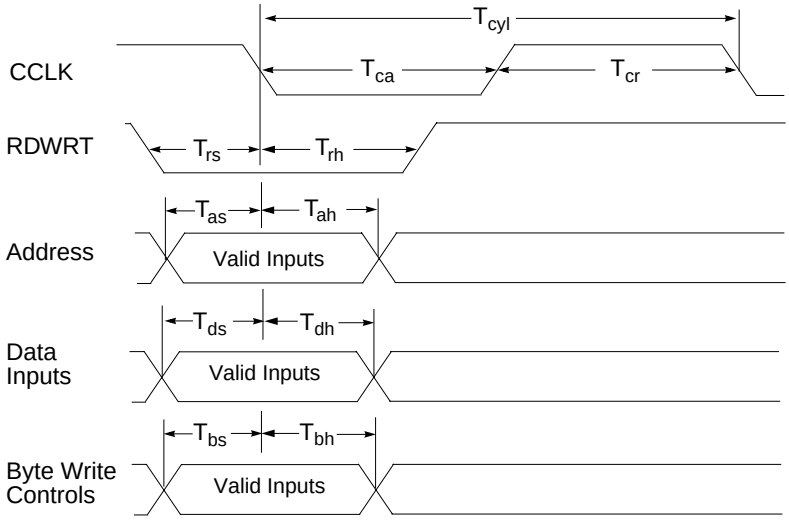
Figure 21. Array Clocked Read Timing



Array Clocked Write

- RDWRT held low or brought low before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is written into the address in the array.
- Data out does not change during a write cycle.

Figure 22. Array Clocked Write Timing



Delay Tables

Table 43 and Table 44 show setup and hold times for representative “small” and “large” SRAM1LG arrays.

Table 43. “Small” SRAM1LG00256X009B9D04S2Q1

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.3
CCLK minimum restore time	T_{cr}	1.3
RDWRT setup time	T_{rs}	0.7
RDWRT hold time	T_{rh}	0.3
Data in setup time	T_{ds}	-0.7
Data in hold time	T_{dh}	0.3
Byte write setup time	T_{bs}	0.4
Byte write hold time	T_{bh}	0.3
Address setup time	T_{as}	0.4
Address hold time	T_{ah}	0.3
Access time	T_{acc}	3.2
Cycle time	T_{cyl}	4.4

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 44. "Large" SRAM1LG16384X018B9D32S8Q2

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.3
CCLK minimum restore time	T_{cr}	1.3
RDWRT setup time	T_{rs}	0.7
RDWRT hold time	T_{rh}	0.3
Data in setup time	T_{ds}	-0.7
Data in hold time	T_{dh}	0.3
Byte write setup time	T_{bs}	0.4
Byte write hold time	T_{bh}	0.3
Address setup time	T_{as}	0.5
Address hold time	T_{ah}	0.3
Access time	T_{acc}	3.5
Cycle time	T_{cyl}	4.6

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a SRAM1LG for a particular application, use the following equation.

$$P = (A_{read} \times RC_{int} + A_{write} \times WC_{int}) \times V^2_{dd} \times F_{RAM}$$

where:

- P = Power in microwatts.
- RC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a read access on every cycle. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a write access on every cycle.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read access is performed (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- A_{write} = Write activity factor, which is the fraction of the total clock cycles that a write access is performed (a value between 0 and 1). In typical applications, the write activity is often less than the read activity, as the contents of an SRAM are read more often than they are replaced. The sum of (A_{read} + A_{write}) must be less than or equal to 1.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{RAM} = Clock frequency applied to the SRAM, in MHz.

Array Area and Footprint

Figure 23 shows the general shape of the SRAM and the relative locations of the pins within it. The dimensions for a representative configuration can be obtained from the sizing routines available on the World Wide Web. Access to the Web page can be obtained from an IBM ASICs representative.

Figure 23. SRAM1LG Footprint

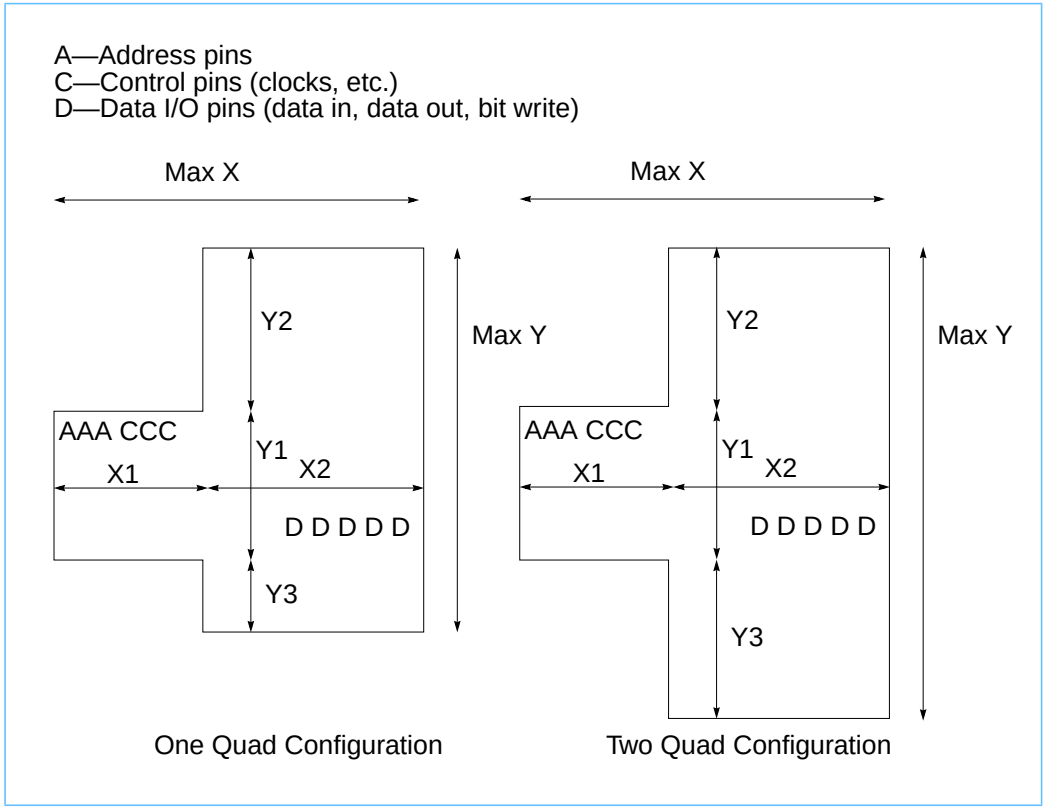


Table 45. SRAM1LG Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Sub	Quad	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Write Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
256 x 9	4	2	1	3.3	4.5	24	19	37292	690	73
256 x 18	4	2	1	3.3	4.5	30	22	44780	807	73
256 x 36	4	2	1	3.3	4.5	43	28	59756	1041	73
1024 x 9	8	2	1	3.3	4.5	26	21	55259	807	98
1024 x 18	8	2	1	3.3	4.5	34	25	76085	1041	98
1024 x 36	4	2	1	3.3	4.5	46	31	108572	1041	149
4096 x 9	16	4	1	3.3	4.5	28	24	119492	1119	149
4096 x 18	16	4	1	3.3	4.5	36	28	185012	1587	149
4096 x 36	8	4	2	3.4	4.6	47	32	327838	1587	258
16384 x 9	32	8	2	3.5	4.6	29	25	368086	1743	258
16384 x 18	32	8	2	3.5	4.6	38	29	609574	2679	258

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read or write operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the SRAM and can be calculated using the following equation:

Total scan latches = 10 + NBIT (the data word width)

The last bits in the scan chain are the data out bits, with the most significant data out bit being in the (nth - 1) scan latch. The nth scan latch drives the SCANOUT, DIAGOUT, and PASSFAIL output pins.

Multiple Array BIST Testing

MABIST Controller Interface

Every instance of an SRAM1LG array on a chip must be connected to a BIST1G controller. Up to 16 one-port SRAMs can be connected to a single BIST1G controller.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

SRAM2G—Compilable Two-Port SRAM

Features

- Fully static array
- Configurations up to 4K words or 128 bits supported
- One dedicated read port and one dedicated write port
- Ports can be operated synchronously or independently
- Write-through capability when read address equals write address
- Multiple decode options for performance and area optimization
- Latched output data until next read cycle
- Bit write control for data masking
- Multiple array built-in self-test
- Single clock edge operation through use of self-timed restore

The key features of the macro are summarized in Table 46.

Table 46. SRAM2G Two-Port SRAM Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1, or 16:1
Maximum macro size	128K (131,072) bits
Maximum words	4096 words
Minimum words	64 words
Maximum data width	128 bits
Minimum data width	8 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%

Table 46. SRAM2G Two-Port SRAM Features (Continued)

Feature	Capability
Global porosity on M2	0%
Global porosity on M3	30%

Valid Array Sizes

In order to limit the maximum bitline and wordline lengths in the cell array, reduce array power dissipation, and support up to 128 Kb macros, the largest macros can be divided into two subarrays. Small arrays requiring up to 32 wordlines will be implemented with one subarray to optimize the control area versus array area. For 32 to 128 wordlines, either one or two subarrays can be used, allowing trade-offs between macro area and performance. Above 128 wordlines, two subarrays must be used to limit the loading on the array bitlines. The array wordlines are limited to a maximum width of 512 cell columns.

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, DECODE, and NARRAY options are given in Table 47.

Table 47. SRAM2G Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–4096	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 48, “Valid SRAM2G Configurations,” on page 119.
NBIT	8–128	The number of bits per word in the array.
DECODE	4, 8, or 16	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array decreases and the width (X) of the array increases.
NARRAY	1 or 2	The number of subarrays used in the array, limited by: NARRAY = 1 if (NWORD/DECODE) $\leq$ 32; NARRAY = 1 or 2 if 32 < (NWORD/DECODE) $\leq$ 128; NARRAY = 2 if 128 < (NWORD/DECODE).

The resultant ranges of valid array configurations are shown in Table 48.

Table 48. Valid SRAM2G Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	64	512	64	8	128
	2	256	1024	128	8	128
8	1	128	1024	128	8	64
	2	512	2048	256	8	64
16	1	256	2048	256	8	32
	2	1024	4096	512	8	32

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 48, “Valid SRAM2G Configurations”.

If the array is clocked with an address larger than NWORD applied at the address input ports, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

There is an exception for write-through mode, when the read address equals the write address and both read and write are active. In this case, the input data will be placed in the data output latches, but the array contents will not be changed.

Global M2 Wiring Porosity

SRAM2G has no global M2 porosity and approximately 30% M3 porosity over the array.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM2GwwwwXbbbDddSsMm

where:

SRAM2G = two-port SRAM name
w = total number of words: 4 digits
b = data width in bits: 3 digits
d = decode option: 2 digits
s = subarray option: 1 digit
m = timing mode: 1 digit
1 = array clocked mode
2 = read/write clocked mode

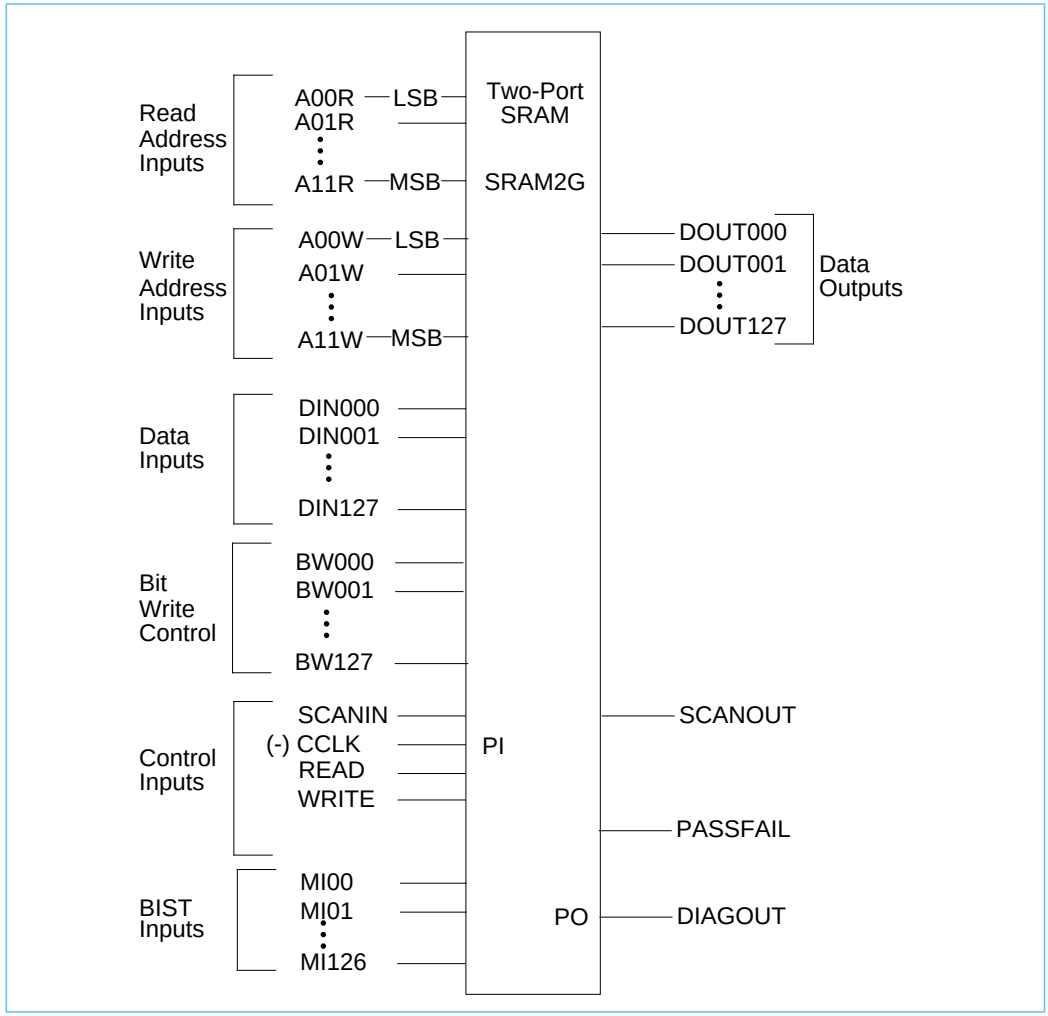
A representative example would be:

SRAM2G0256X064D04S1M1	A 256-word x 64-bit two-port SRAM, using the 4:1 decode option and one subarray, with array-clocked functional mode timing.

Logical Description

A symbolic representation of the two-port SRAM is shown in Figure 24.

Figure 24. SRAM2G Two-Port SRAM Logic Symbol



Pin Definitions

Table 49 summarizes the function and proper usage of the macro pins shown in Figure 24 on page 121. The control and input pins must be stable before the clocks initiate a read or write access of the array. Pin timing relationships are described later.

Table 49. Pin Definitions

Pin	Description
A00R–A11R	The read address input pins define the address from which output data will be read. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation words = 2^N. The bit address occupies the least significant bits, using: A00R and A01R for decode = 4:1; A00R, A01R, and A02R for decode = 8:1; or A00R, A01R, A02R, and A03R for decode = 16:1. The word address follows. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
A00W–A11W	The write address input pins define the address to which input data will be written and follow the same conventions as the read address input pins. There must be an equal number of read and write address pins.
DIN00–DIN127	The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the DIN000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
BW000–BW127	The bit write control input pins are active high, and one pin is required for each data input bit. The bit write control pins allow masking of the input data. If the pin is held high, the corresponding data input bit is written into the array. If the pin is held low, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pins are used starting at the BW000 least significant bit and counting upwards. If a data input pin is not used, then the corresponding bit write control pin will not appear in the logical or physical models either. However, a bit write control pin is always allocated for every data input pin used. If bit write control is not required, then these pins must be tied high.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
CCLK	The C clock pin initiates a read or write access of the SRAM on its falling edge during functional mode operations. This pin must come from a primary input.

Table 49. Pin Definitions (Continued)

Pin	Description
READ	The read pin causes a read of the array to be performed when held high at the same time the C clock is active.
WRITE	The write pin causes a write of the array to be performed when held high at the same time the C clock is active.
MI00–MI26	The BIST pins must be connected to an accompanying BIST2 controller as they control the SRAM during BIST testing. The number required is fixed at 27. The MInn pins must not be connected to anything other than the BIST2 controller.
DOUT000–DOUT127	The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the DOUT000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read. Write operations do not affect the data output pins.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during MABIST testing and must be routed to the accompanying BIST2 controller for the array. The PASSFAIL pin must not be connected to anything other than the BIST2 controller. Note that this pin is “nonvalidated” and thus cannot be monitored directly to determine if there are fails in the array. The BIST2 controller “validates” the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

Array functional operation is the normal operation of the SRAM when the BIST2G controller is inactive. Array functional operations include read, write, and write-through.

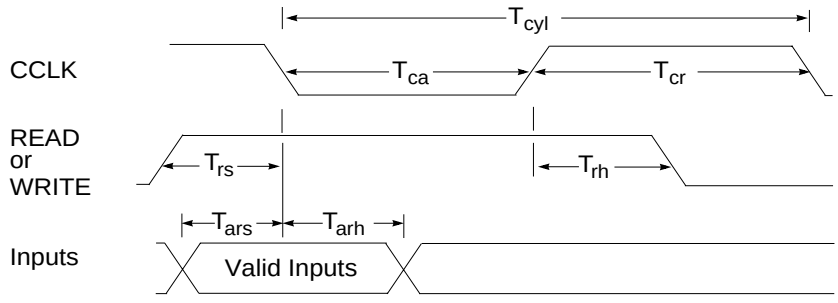
Two timing modes are defined within functional operation: array clocked and read-write clocked, which allow read and write operations to be synchronized or to be performed independently.

Array Clocked Mode

Array Clocked Mode Definition

In array clocked mode, the read and write operations are synchronized by activating the READ and WRITE inputs before initiating the cycle by dropping the CCLK input, as shown in Figure 25. On a given cycle, it is not necessary to activate both the READ and WRITE lines. Each can be executed alone, or if neither is activated, the falling CCLK will not initiate an array access.

Figure 25. Array Clocked Operation



CCLK falling initiates the access cycle
Inputs set up and held relative to the CCLK

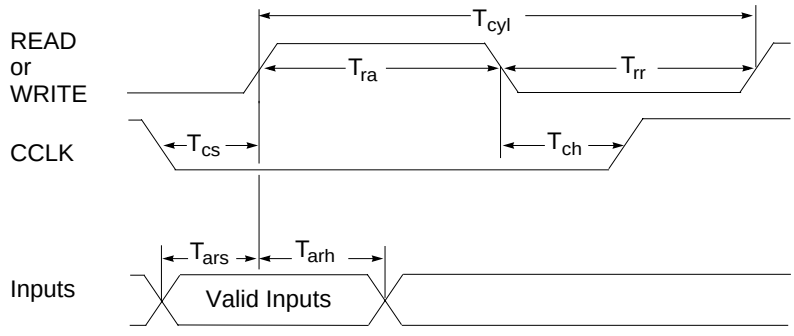
Read-Write Clocked Mode Definition

In read-write clocked mode, the read and write operations can be independent by activating CCLK first, and using the READ and WRITE control lines to independently initiate read and write cycles respectively, as shown in Figure 26. In this mode, the read and write cycle times are defined independently.

To preserve data integrity when the write address equals read address, minimum READ to WRITE and WRITE to READ setup times are required. If the READ and WRITE signals are synchronized (that is, they always have the same timing relationship between them), then these setup times can be verified using ASIC timing tools. However, if the READ and WRITE clocks are operated asynchronously, there is no way to ensure that these timings

will be met, and there will be an “unknown” region where it is not known whether the previously stored data in the cell array or the new write port data has been read from the array. The new write port data will always be written correctly into the cell array, independent of the timing relationship between the READ and WRITE signals.

Figure 26. Read-Write Clocked Operation



READ clock rising initiates the read cycle
WRITE clock rising initiates the write cycle
Inputs set up and held relative to their respective READ or WRITE clock

Write-Through Definition

A read and write operation to the same address during the same cycle is called write-through operation. During write-through, data is read from the write port data-in pins, rather than from the array cells. Therefore, write-through read access time is less than for a normal cell array read access. However, if the bit write pin is selected to block the write of a bit, then the write-through operation is blocked for that bit, and data is read from the cell array with a normal read access time.

The write-through path can only be activated during an array clocked operation, where the READ and WRITE signals have been activated before the CCLK is activated. The write-through path will not be activated in read-write clocked mode, where the READ or WRITE signals go active while the CCLK is already active. Thus, if there are situations where the read address equals the write address during read-write clocked operation, the precautions described above must be observed.

Array Clocking Modes in Array Functional Operation

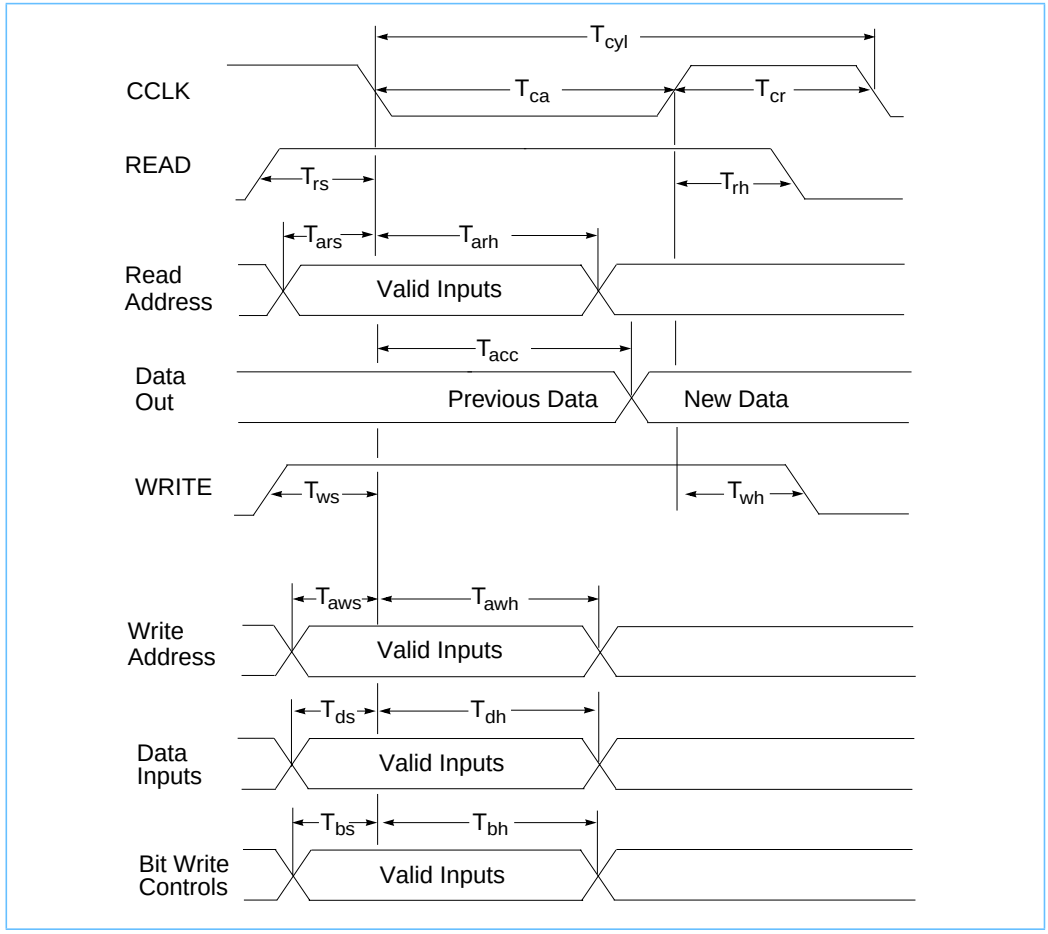
Array Clocked Read and Write

- READ and WRITE clocks held high or brought high before the CCLK edge.
- Read address does not equal write address.
- CCLK falling initiates the read and write cycles.
- Data is read from the read address in the array.
- Data is written into the write address in the array for pins with the bit write control high.

Array Clocked Write-Through

- READ and WRITE clocks held high or brought high before the CCLK edge.
- Read address equals write address.
- CLK falling initiates the write-through cycle.
- For pins with the bit write control high, data is written into the write address in the array and also appears on the data outputs.
- For pins with the bit write control low, data is not written into the write address in the array, and the previous data from that location appears on the data output pin.

Figure 27. Array Clocked Read and Write Timing



Read-Write Clocking Modes in Array Functional Operation

Read-Write Clocked Read-Only

- CCLK held low or brought low before the READ clock edge.
- WRITE clock held low.
- READ clock rising initiates the access cycle.
- Data is read from the read address in the array.
- Data appears at the data out pins after the access time has elapsed.
- No setup or hold time requirements on write address, data input, or bit write control pins.

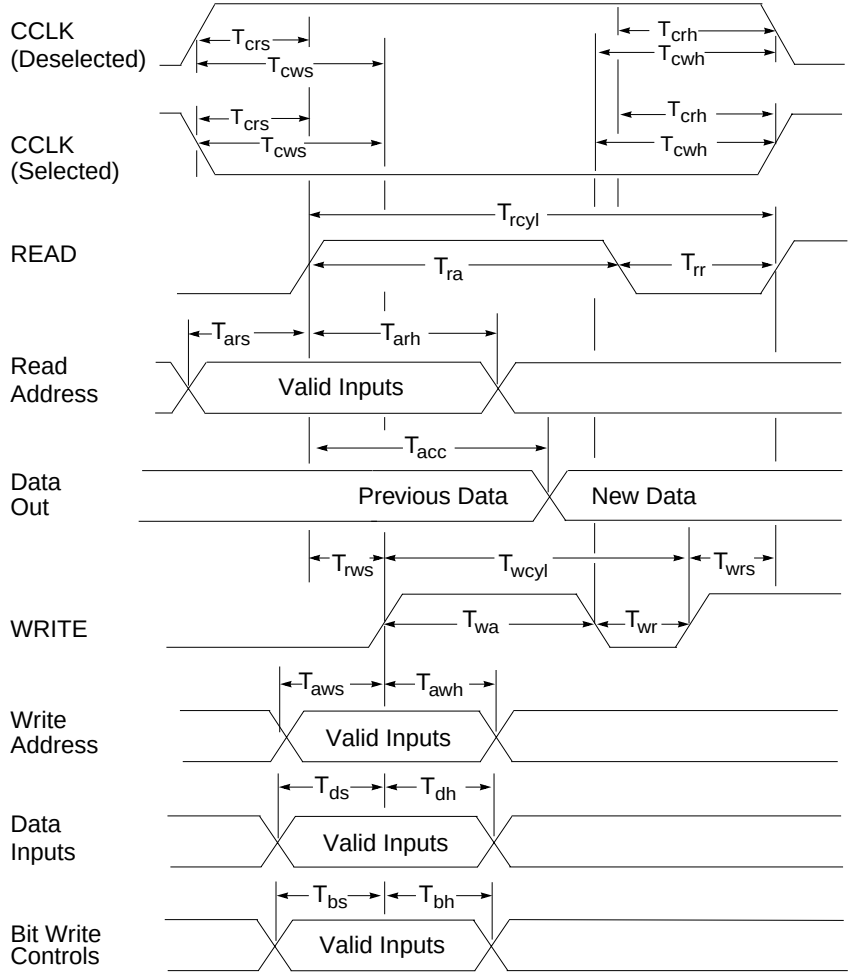
Read-Write Clocked Write-Only

- CCLK held low or brought low before the WRITE clock edge.
- READ clock held low.
- WRITE clock rising initiates the access cycle.
- Data is written into the write address in the array for pins with the bit write control high.
- Data out does not change during a write-only cycle.
- No setup or hold time requirements on read address.

Read-Write Clocked Read and Write

- CCLK held low or brought low before both the READ and WRITE clock edges.
- Read address does not equal write address.
- Read clock rising initiates the read cycle.
- Write clock rising initiates the write cycle.
- Data is read from the read address in the array.
- Data is written into the write address in the array for pins with the bit write control high.

Figure 28. Read-Write Clocked Read and Write Timing



Delay Tables

Table 50 and Table 51 show setup and hold times for representative “small” and “large” SRAM2G arrays.

Table 50. “Small” SRAM2G0064X016D04S1

Timing Parameter	Abbreviation	Minimum (ns)
Array Clocked Mode		
CCLK minimum active time	T_{ca}	0.9
CCLK minimum restore time	T_{cr}	0.8
READ clock setup time	T_{rs}	0.5
READ clock hold time	T_{rh}	-0.3
WRITE clock setup time	T_{ws}	0.5
WRITE clock hold time	T_{wh}	-0.3
Data in setup time	T_{ds}	0.0
Data in hold time	T_{dh}	1.0
Bit write setup time (selected)	T_{bs}	0.0
Bit write hold time (selected)	T_{bh}	1.0
Read address setup time	T_{ars}	0.6
Read address hold time	T_{arh}	0.8
Write address setup time	T_{aws}	0.6
Write address hold time	T_{awh}	0.8
Access time	T_{acc}	1.7
Cycle time	T_{cyl}	2.6

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 50. "Small" SRAM2G0064X016D04S1 (Continued)

Timing Parameter	Abbreviation	Minimum (ns)
Read/Write Clocked Mode		
READ clock minimum active time	T_{ra}	1.0
READ clock minimum restore time	T_{rr}	0.7
WRITE clock minimum active time	T_{wa}	1.0
WRITE clock minimum restore time	T_{wr}	0.7
CCLK setup time before READ	T_{crs}	0.6
CCLK hold time after READ	T_{crh}	0.5
CCLK setup time before WRITE	T_{cws}	0.6
CCLK hold time after WRITE	T_{cwh}	0.5
READ clock setup before WRITE	T_{rws}	0.6
WRITE clock setup before READ	T_{wrs}	0.9
Data in setup time	T_{ds}	-0.2
Data in hold time	T_{dh}	1.2
Bit write setup time (selected)	T_{bs}	-0.3
Bit write hold time (selected)	T_{bh}	1.2
Read address setup time	T_{ars}	0.1
Read address hold time	T_{arh}	0.9
Write address setup time	T_{aws}	0.1
Write address hold time	T_{awh}	1.1
Access time	T_{acc}	2.0
Read cycle time	T_{rcyl}	2.3
Write cycle time	T_{wcyl}	2.5

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 51. “Large” SRAM2G4096X032D16S2

Timing Parameter	Abbreviation	Minimum (ns)
Array Clocked Mode		
CCLK minimum active time	T_{ca}	1.0
CCLK minimum restore time	T_{cr}	1.1
READ clock setup time	T_{rs}	0.5
READ clock hold time	T_{rh}	-0.3
WRITE clock setup time	T_{ws}	0.5
WRITE clock hold time	T_{wh}	-0.3
Data in setup time	T_{ds}	-0.1
Data in hold time	T_{dh}	1.1
Bit write setup time (selected)	T_{bs}	-0.1
Bit write hold time (selected)	T_{bh}	1.1
Read address setup time	T_{ars}	0.7
Read address hold time	T_{arh}	0.9
Write address setup time	T_{aws}	0.6
Write address hold time	T_{awh}	0.9
Access time	T_{acc}	2.2
Cycle time	T_{cyl}	2.9

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 51. "Large" SRAM2G4096X032D16S2 (Continued)

Timing Parameter	Abbreviation	Minimum (ns)
Read/Write Clocked Mode		
READ clock minimum active time	T_{ra}	1.1
READ clock minimum restore time	T_{rr}	1.0
WRITE clock minimum active time	T_{wa}	1.1
WRITE clock minimum restore time	T_{wr}	0.8
CCLK setup time before READ	T_{crs}	0.6
CCLK hold time after READ	T_{crh}	0.5
CCLK setup time before WRITE	T_{cws}	0.6
CCLK hold time after WRITE	T_{cwh}	0.5
READ clock setup before WRITE	T_{rws}	0.6
WRITE clock setup before READ	T_{wrs}	1.0
Data in setup time	T_{ds}	-0.4
Data in hold time	T_{dh}	1.4
Bit write setup time (selected)	T_{bs}	-0.4
Bit write hold time (selected)	T_{bh}	1.4
Read address setup time	T_{ars}	0.3
Read address hold time	T_{arh}	0.9
Write address setup time	T_{aws}	0.2
Write address hold time	T_{awh}	1.2
Access time	T_{acc}	2.4
Read cycle time	T_{rcyl}	2.8
Write cycle time	T_{wcyl}	2.8

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a SRAM2G for a particular application, use the following equation:

$$P = (A_{read} \times RC_{int} + A_{write} \times WC_{int}) \times V^2_{dd} \times F_{RAM}$$

where:

- P = Power in microwatts
- RC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a read access on every cycle. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a write access on every cycle.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read access is performed (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- A_{write} = Write activity factor, which is the fraction of the total clock cycles that a write access is performed (a value between 0 and 1). In typical applications, the write activity is often less than the read activity, as the contents of an SRAM are read more often than they are replaced. For a 2-port SRAM, the sum of the read and write activity factors can be greater than 1, but must be less than or equal to 2.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{RAM} = Clock frequency applied to the SRAM, in MHz.

Array Area and Footprint

Figure 29 shows the general shape of the SRAM, and the relative locations of the pins within it. The dimensions for a representative configuration can be obtained from the sizing routines available on the World Wide Web. Access to the Web page can be obtained from an IBM ASICs representative.

Figure 29. SRAM2G Footprint

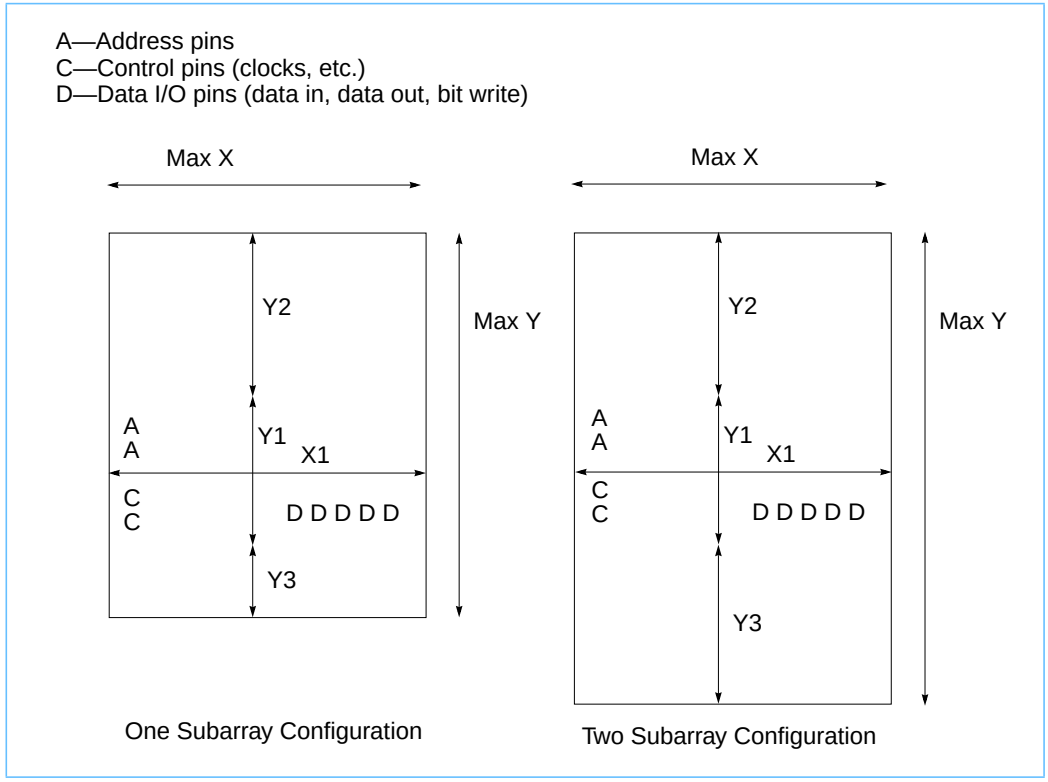


Table 52. SRAM2G Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Sub	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Write Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
256 x 16	4	1	1.8	2.6	65	36	42588	819	52
256 x 32	4	1	1.8	2.6	101	54	70876	1363	52
256 x 64	4	1	1.9	2.7	174	90	127452	2451	52
256 x 128	4	1	2.0	2.7	319	162	240708	4629	52
1024 x 16	8	1	2.0	2.8	114	58	103588	1363	76
1024 x 32	8	1	2.1	2.8	179	86	186276	2451	76
1024 x 64	8	1	2.1	2.9	309	141	351804	4629	76
1024 x 128	4	2	2.1	2.9	358	183	648060	4629	140
4096 x 16	16	2	2.1	2.8	173	79	343140	2451	140
4096 x 32	16	2	2.1	2.9	292	125	648060	4629	140

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read or write operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the SRAM and can be calculated using the following equation:

Total scan latches = 15 + NBIT (the data word width)

The last bits in the scan chain are the data out bits, with the most significant data out bit being in the (nth - 1) scan latch. The nth scan latch drives the SCANOUT, DIAGOUT, and PASSFAIL output pins.

Multiple Array BIST Testing

MABIST Controller Interface

Every instance of an SRAM2G array on a chip must be connected to a BIST2G controller. Up to 16 SRAM2G arrays can be connected to a single BIST2G controller.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

BIST1G and BIST2G—BIST Controllers for SRAMs

Features

- Complete test of all array functions
- Up to 16 arrays tested in parallel from one controller
- System LBIST compatible

The key features of the macro are summarized in Table 53.

Table 53. BIST Controller Features

Feature	Capability
BIST1G and BIST2G supported V_{dd} range	0.90V–1.95V
Macro dimensions—BIST1G	396 x 19 chip unit cells
Macro dimensions—BIST2G	396 x 19 chip unit cells
Macro area—BIST1G	7,524 chip unit cells
Macro area—BIST2G	7,524 chip unit cells
DC test methodology	Multiple array BIST
AC test methodology	Access time
Global porosity on M1—BIST1G	0%
Global porosity on M1—BIST2G	0%
Global porosity on M2—BIST1G	50%
Global porosity on M2—BIST2G	50%
Global porosity on M3—BIST1G	75%
Global porosity on M3—BIST2G	75%

BIST Description

The BIST controller performs all of the necessary DC tests for the arrays during product test by applying addresses, data inputs, bit write controls, and read/write controls to the array. The BIST control signals are multiplexed with the functional inputs for the address, data, and control signals with minimal impact on the SRAM's access and setup and hold times.

Usage Requirements

Whenever compilable one-port or two-port SRAMs are used, the BIST controllers must be used to generate the BIST test patterns required to verify the SRAMs during product test. BIST1G can be used to control from 1 to 16 one-port SRAMs of any configuration, and BIST2G can be used to control from 1 to 16 two-port SRAMs of any configuration.

Symbol Naming Conventions

The BIST controllers do not have a dependence on the SRAM configurations to which they are connected. Therefore, their names are simply:

BIST1G *= BIST controller for one-port SRAMs*

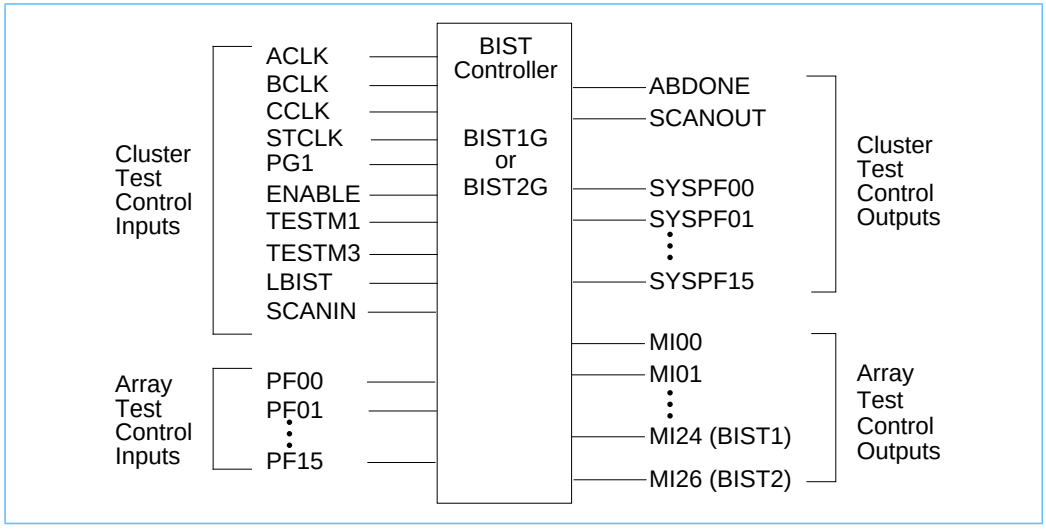
BIST2G *= BIST controller for two-port SRAMs*

Logical Description

Logical Symbol

A symbolic representation of the BIST1G or BIST2G controller is shown in Figure 30.

Figure 30. BIST1G and BIST2G Controller Logic Symbol



Pin Definitions

Table 54 on page 141 summarizes the function and use of the macro pins shown in Figure 30. Information describing the use of these pins in various test modes can be obtained from an IBM ASICs representative.

Table 54. Pin Definitions

Pin	Description
ACLK	The A clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD A clocks on the chip. The A clock is active high during scan operations and must be held low during array mode operation.
BCLK	The B clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD B clocks on the chip. The B clock is active high during scan and BIST operations.
CCLK	The C clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is active high during BIST operations and must come from a primary input but can be common with other LSSD C clocks on the chip. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
STCLK	The system test oscillator clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
PG1	The C clock gate pin is used to gate the CCLK signal. This pin is usually held high, unless it is used during LBIST operations.
ENABLE	The self-test clock enable pin is used to gate the STCLK signal. This pin is usually held high, unless it is used during LBIST operations.
TESTM1	The TESTM1 pin is used together with the TESTM3 pin to set the test state of the BIST controller and the attached arrays. TESTM1 is held low for functional operation of the array.
TESTM3	The TESTM3 pin is used together with the TESTM1 pin to set the test state of the BIST controller and the attached arrays. TESTM3 is held low for functional operation of the array and must be routed from a chip primary input.
LBIST	The LBIST pin must be held high during system LBIST testing to block the B clock to the SRAMs. It must be held low during logic flush and scan operations.
PF00–PF15	The PF pins are array test inputs which receive the pass/fail state of the arrays on each BIST test cycle. One PF pin is connected to each array being tested. Unused PF pins must be tied to ground.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the BIST controller. The scan-in pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
ABDONE	The ABIST done pin goes high when the BIST controller has completed issuing test patterns to the arrays within its cluster. This pin does not have to be connected.

Table 54. Pin Definitions (Continued)

Pin	Description
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the BIST controller. The scan-out pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
SYSPF00–SYSPF15	The SYSPF pins are cluster test outputs which allow the BIST pass/fail bits to be observed by on-chip system test logic without requiring a scan operation. These pins are not required to be connected.
MI00–MI26	The MI array test pins are only routed to the arrays under the control of the BIST macro and control the SRAMs during BIST testing. The MI pins must not be wired to any other circuits within the ASIC chip. BIST1G uses MI00–MI24; BIST2G uses MI00–MI26.

Operational Modes

For complete information on integrating the BIST1G or BIST2G controllers into a chip test environment, contact your IBM ASICs representative.

Macro Footprint

The BIST1G and BIST2G controllers are rectangular.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is fixed for all configurations at:

BIST1G scan latches = 108
BIST2G scan latches = 112

MABIST Test Mode Clock Cycle Calculations

The number of clock cycles required to complete the BIST test is also fixed at:

BIST1G clock cycles = 2,423,893
BIST2G clock cycles = 2,554,968

SRAM1R—Compilable High Density One-Port SRAM

Features

- Fully static array
- Configurations up to 32K words or 128 bits supported
- One read and write port
- Multiple decode options for performance and area optimization
- Latched output data until next read cycle
- Bit write control for data masking
- Array built-in self-test
- Single clock edge operation through use of self-timed restore
- Wordline redundancy activated by laser-blow fuses

The key features of the macro are summarized in Table 55.

Table 55. SRAM1R One-Port SRAM Features

Feature	Capability
Supported V_{dd} range	1.40V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1,16:1, or 32:1
Maximum macro size	1M (1,048,576) bits
Minimum macro size	32K (32,768) bits
Maximum words	32,768 words
Minimum words	256 words
Maximum data width	128 bits
Minimum data width	8 bits
DC test methodology	Array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%

Table 55. SRAM1R One-Port SRAM Features (Continued)

Feature	Capability
Global porosity on M2	0%
Global porosity on M3	60%
Wordline redundancy	4 wordlines per subarray

Valid Array Sizes

To limit the maximum bitline and wordline lengths in the cell array, reduce array power dissipation, and support up to 1Mb macros, the largest macros can be divided into subarrays. Small arrays requiring up to 64 wordlines will be implemented with one subarray to optimize the control area versus array area. For 96 to 512 wordlines, either one or two subarrays can be used, allowing trade-offs between macro area and performance. Above 512 wordlines, two subarrays must be used to limit the loading on the array bitlines. The array wordlines are limited to a maximum width of 1024 cell columns.

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, DECODE, and NARRAY options are given in Table 56.

Table 56. SRAM1R Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	256–32768	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 57, “Valid SRAM1R Configurations,” on page 145.
NBIT	8–128	The number of bits per word in the array.
DECODE	4, 8, 16, or 32	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array decreases and the width (X) of the array increases.
NARRAY	1 or 2	The number of subarrays used in the array, limited by: NARRAY = 1 if (NWORD/DECODE) < 96; NARRAY = 1 or 2 if 96 ≤ (NWORD/DECODE) ≤ 512; NARRAY = 2 if 512 < (NWORD/DECODE).

The resultant ranges of valid array configurations are shown in Table 57.

Table 57. Valid SRAM1R Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	256	1024	64	8	128
		1152	2048	128	8	128
	2	384	2048	128	8	128
		2304	4096	256	8	128
8	1	256	2048	128	8	128
		2304	4096	256	8	128
	2	768	4096	256	8	128
		4608	8192	512	8	128
16	1	256	4096	256	8	64
		4608	8192	512	8	64
	2	1536	8192	512	8	64
		9216	16384	1024	8	64
32	1	512	8192	512	8	32
		9216	16384	1024	8	32
	2	3072	16384	1024	8	32
		18432	32768	2048	8	32

Note: Valid configurations must contain a minimum of 32,768 bits, as given by word depth x data width.

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 57.

If the array is clocked with an address larger than NWORD applied at the address input port, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

Global M2 Wiring Porosity

SRAM1R has no global M2 porosity and approximately 60% M3 porosity over the array.

Usage Limitations

The number of SRAMs with redundancy on a chip cannot exceed three times the number of LSSD scan chains not containing an embedded DRAM on the chip. For example, if a chip contains 24 scan chains, and two of these chains contain embedded DRAMs, then the total number of SRAMS with redundancy allowed is given by the following equation:

$$(24 - 2) * 3 = 66$$

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM1RwwwwwXbbbDddSsM1

where:

SRAM1R	=	high density one-port SRAM name
w	=	total number of words: 5 digits
b	=	data width in bits: 3 digits
d	=	decode option: 2 digits
s	=	subarray option: 1 digit
M1	=	array-clocked timing mode only

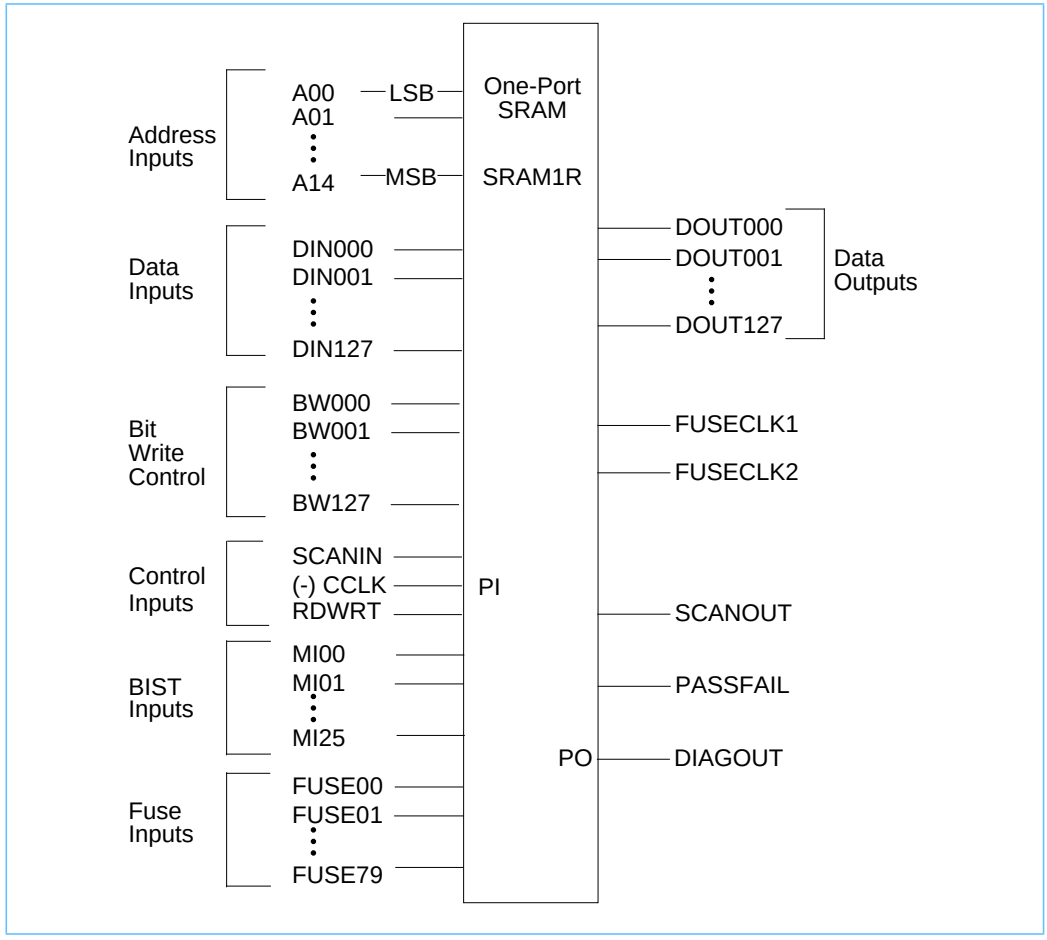
A representative example would be:

SRAM1R01024X008D16S1M1	A 1024-word x 8-bit one-port SRAM, using the 16:1 decode option and one subarray.

Logical Description

A symbolic representation of the one-port SRAM is shown in Figure 31.

Figure 31. SRAM1R One-Port SRAM Logic Symbol



Pin Definitions

Table 58 summarizes the function and proper usage of the macro pins shown in Figure 31 on page 147. The control and input pins must be stable before the clocks initiate a read or write access of the array. Pin timing relationships are described later.

Table 58. Pin Definitions

Pin	Description
A00–A14	The address input pins define the address from or to which data will be read or written. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation words = 2^N. The bit address occupies the least significant bits, using: A00 and A01 for decode = 4:1; A00, A01, and A02 for decode = 8:1; A00, A01, A02, and A03 for decode = 16:1; or A00, A01, A02, A03, and A04 for decode = 32:1. The word address follows. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
DIN000–DIN127	The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the DIN000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
BW000–BW127	The bit write control input pins are active high, and one pin is required for each data input bit. The bit write control pins allow masking of the input data. If the pin is held high, the corresponding data input bit is written into the array. If the pin is held low, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pins are used starting at the BW000 least significant bit and counting upwards. If a data input pin is not used, then the corresponding bit write control pin will not appear in the logical or physical models either. However, a bit write control pin is always allocated for every data input pin used. If bit write control is not required, then these pins must be tied high.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
CCLK	The C clock pin initiates a read or write access of the SRAM on its falling edge during functional mode operations. This pin must come from a primary input.
RDWRT	The read/write control pin causes a read of the array to be performed when held high or a write to be performed when held low when the C clock is strobed active.
MI00–MI25	The BIST input pins must be connected to an accompanying BIST1R controller as they control the SRAM during BIST testing. The number required is fixed at 26. The MInn pins must not be connected to anything other than the BIST1R controller.

Table 58. Pin Definitions (Continued)

Pin	Description
FUSE00–FUSE79	The fuse input pins must be connected to an accompanying fuse macro as they provide coded data used by the SRAM's redundancy circuitry. Only pins FUSE00–FUSE39 will appear on a one subarray macro, while all fuse pins (FUSE00–FUSE79) will be used on a two subarray macro.
DOUT000–DOUT127	The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the DOUT000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read. Write operations do not affect the data output pins.
FUSECLK1 and FUSECLK2	The fuse clock pins must be connected to an accompanying fuse macro to drive the power-on-reset clock which loads the fuse data into the SRAM. Only pin FUSECLK1 will appear on a one subarray macro, while both FUSECLK1 and FUSECLK2 will be used on a two subarray macro.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during BIST testing and must be routed to the accompanying BIST1R controller for the array. The PASSFAIL pin must not be connected to anything other than the BIST1R controller. Note that this pin is "nonvalidated" and thus cannot be monitored directly to determine if there are fails in the array. The BIST1R controller "validates" the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics, to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

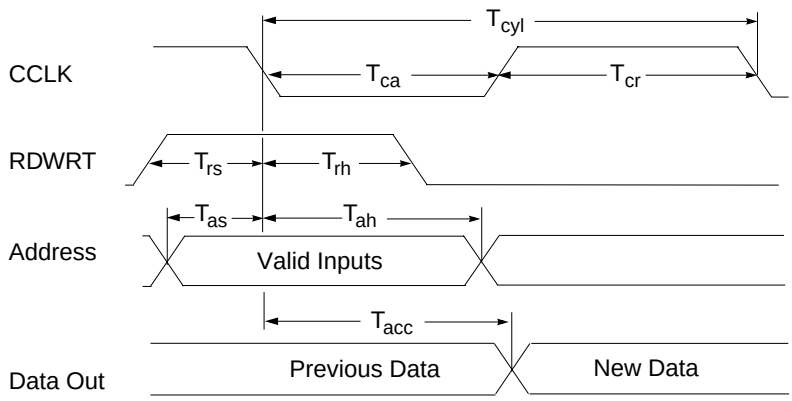
Array functional operation is the normal operation of the SRAM when the BIST1R controller is inactive. Array functional operations include read and write.

Array Clocking Modes

Array Clocked Read

- RDWRT held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is read from the address in the array.
- Data appears at the data out pins after the access time has elapsed.
- Data out is valid until the next read cycle.

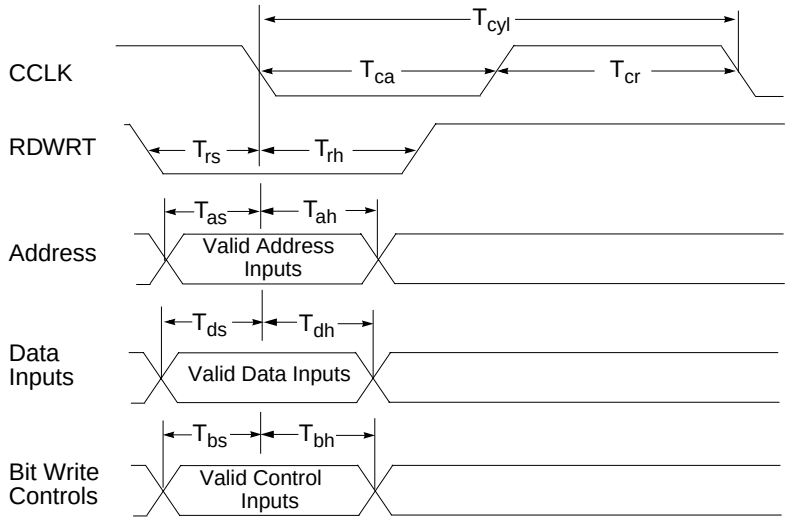
Figure 32. Array Clocked Read Timing



Array Clocked Write

- RDWRT held low or brought low before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is written into the address in the array.
- Data out does not change during a write cycle.

Figure 33. Array Clocked Write Timing



Delay Tables

Table 59 and Table 60 show setup and hold times for representative “small” and “large” SRAM1R arrays.

Table 59. “Small” SRAM1R01024X032D08S1

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	0.9
CCLK minimum restore time	T_{cr}	0.9
RDWRT setup time	T_{rs}	0.2
RDWRT hold time	T_{rh}	0.5
Data in setup time	T_{ds}	0.1
Data in hold time	T_{dh}	0.8
Bit write setup time	T_{bs}	0.2
Bit write hold time	T_{bh}	0.8
Address setup time	T_{as}	1.0
Address hold time	T_{ah}	0.4
Access time	T_{acc}	2.1
Cycle time	T_{cyl}	2.4

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 60. “Large” SRAM1R32768X032D32S2

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.2
CCLK minimum restore time	T_{cr}	1.7
RDWRT setup time	T_{rs}	1.6
RDWRT hold time	T_{rh}	0.5
Data in setup time	T_{ds}	0.1
Data in hold time	T_{dh}	1.0
Bit write setup time	T_{bs}	0.2
Bit write hold time	T_{bh}	1.0
Address setup time	T_{as}	1.0
Address hold time	T_{ah}	0.4
Access time	T_{acc}	3.3
Cycle time	T_{cyl}	3.4

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a SRAM1R for a particular application, use the following equation.

$$P = (A_{read} \times RC_{int} + A_{write} \times WC_{int}) \times V^2_{dd} \times F_{RAM}$$

where:

- P = Power in microwatts.
- RC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a read access on every cycle. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a write access on every cycle.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read access is performed (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- A_{write} = Write activity factor, which is the fraction of the total clock cycles that a write access is performed (a value between 0 and 1). In typical applications, the write activity is often less than the read activity, as the contents of an SRAM are read more often than they are replaced. The sum of (A_{read} + A_{write}) must be less than or equal to 1.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{RAM} = Clock frequency applied to the SRAM, in MHz.

Array Area and Footprint

Figure 34 shows the general shape of the SRAM and the relative locations of the pins within it. The dimensions for a particular configuration can be obtained from the sizing routines available on the World Wide Web. Access to the Web page can be obtained from an IBM ASICs representative.

Figure 34. SRAM1R Footprint

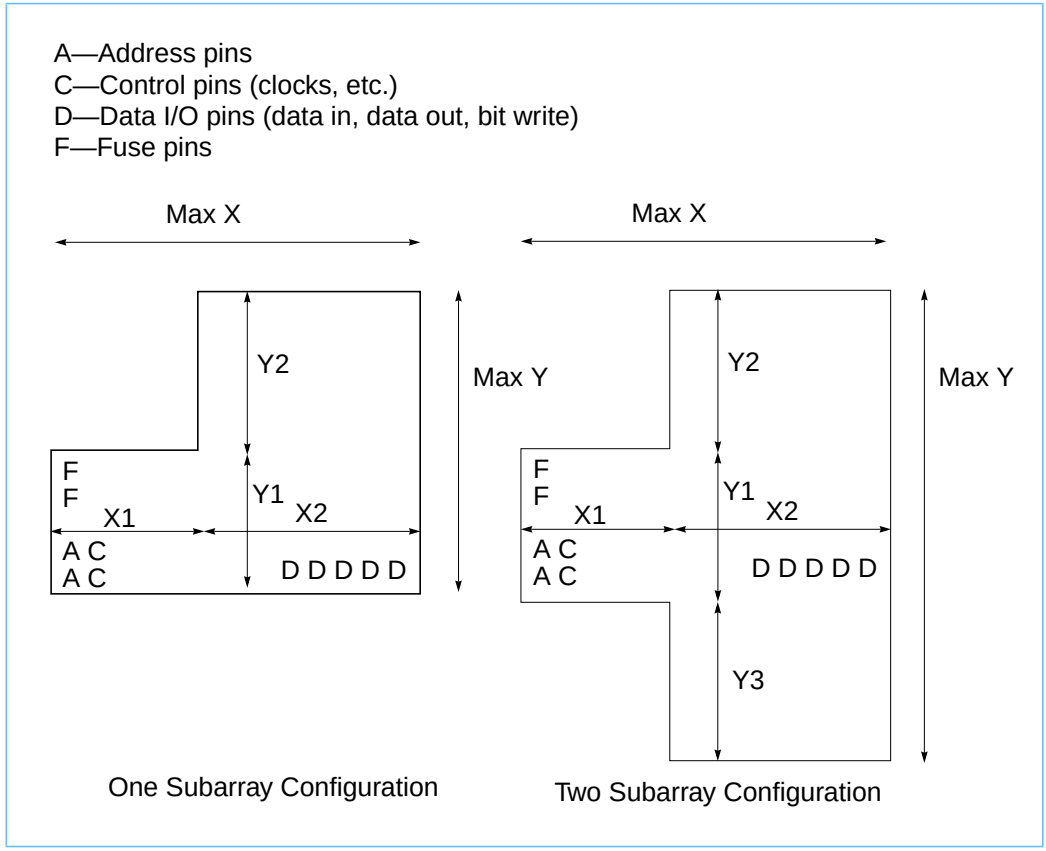


Table 61. SRAM1R Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Sub	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Write Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
256 x 128	4	1	2.0	2.2	212	182	108345	1747	63
1024 x 32	8	1	2.1	2.4	88	81	79240	959	86
1024 x 64	4	1	2.3	2.7	133	128	119425	959	131
1024 x 128	4	1	2.4	2.7	233	223	222653	1747	131
4096 x 16	16	1	2.4	2.7	84	81	119425	959	131
4096 x 32	16	1	2.5	2.7	138	133	222653	1747	131
4096 x 64	8	1	3.0	3.3	198	206	380667	1747	225
4096 x 128	8	1	3.2	3.4	347	362	735267	3323	225
16384 x 16	32	1	3.1	3.3	151	149	380667	1747	225
16384 x 32	16	2	3.0	3.3	179	177	729888	1747	432
16384 x 64	16	2	3.2	3.4	302	298	1410720	3323	432
32768 x 16	32	2	3.1	3.3	162	157	729888	1747	432
32768 x 32	32	2	3.3	3.4	269	260	1410720	3323	432

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read or write operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the SRAM and can be calculated using the following equation:

Total scan latches = 14 + NBIT (the data word width)

The last bits in the scan chain are the data out bits, with the most significant data out bit being in the (nth - 1) scan latch. The nth scan latch drives the SCANOUT, DIAGOUT, and PASSFAIL output pins.

BIST Array Testing

BIST Controller Interface

Every instance of an SRAM1R array on a chip must be connected to a BIST1R controller.

Redundancy

Fuse Macro Interface

Every instance of an SRAM1R array on a chip must be connected to a FUSE macro. One subarray SRAM1R arrays must use a FUSES1ppmmm macro, and two subarray SRAM1R arrays must use both a FUSES1ppmmm macro and a FUSES2ppmmm macro. Refer to the fuse “Symbol Naming Conventions” on page 172 for the complete naming convention as a function of the chip image to be used.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

SRAM1RN—Compilable High Density One-Port SRAM without Fuse Redundancy

Features

SRAM1RN is physically and logically identical to the SRAM1R compilable high density one-port SRAM with redundancy. The models and technical data for SRAM1RN are SRAM1R compiler copies. SRAM1RN is a separate entity only to distinguish the connection requirements on a chip, which differ from the SRAM1R in the following two ways:

- Must connect to a BIST1RN controller
- All FUSEnn input pins must be tied high.

The key features of the macro are summarized in Table 62.

Table 62. SRAM1RN One-Port SRAM Features

Feature	Capability
Supported V_{dd} range	1.40V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1,16:1, or 32:1
Maximum macro size	1M (1,048,576) bits
Minimum macro size	512 bits
Maximum words	32,768 words
Minimum words	64 words
Maximum data width	128 bits
Minimum data width	8 bits
DC test methodology	Array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%

Table 62. SRAM1RN One-Port SRAM Features (Continued)

Feature	Capability
Global porosity on M2	0%
Global porosity on M3	60%
Wordline redundancy	Inactive, FUSE pins tied off

Usage Restrictions

SRAM1RN should only be quoted for use in customer applications after approval from program management and manufacturing. It should only be considered for applications with less than 1 Mb total SRAM1RN bits on the chip, and where the chip size is small enough such that the use of SRAM1RN versus the standard SRAM produces a meaningful reduction in chip size.

SRAM1RN is not limited to a maximum number of arrays on a chip as a function of scan chains the way SRAM1R is. Any number can be used.

Valid Array Sizes

To limit the maximum bitline and wordline lengths in the cell array, reduce array power dissipation, and support up to 1Mb macros, the largest macros can be divided into subarrays. Small arrays requiring up to 64 wordlines will be implemented with one subarray to optimize the control area versus array area. For 96 to 512 wordlines, either one or two subarrays can be used, allowing trade-offs between macro area and performance. Above 512 wordlines, two subarrays must be used to limit the loading on the array bitlines. The array wordlines are limited to a maximum width of 1024 cell columns.

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, DECODE, and NARRAY options are shown in Table 63.

Table 63. SRAM1RN Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–32768	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 64, “Valid SRAM1RN Configurations,” on page 161.
NBIT	8–128	The number of bits per word in the array.
DECODE	4, 8, 16, or 32	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array decreases and the width (X) of the array increases.
NARRAY	1 or 2	The number of subarrays used in the array, limited by: NARRAY = 1 if (NWORD/DECODE) < 96; NARRAY = 1 or 2 if 96 ≤ (NWORD/DECODE) ≤ 512; NARRAY = 2 if 512 < (NWORD/DECODE).

The resultant ranges of valid array configurations are shown in Table 64.

Table 64. Valid SRAM1RN Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	64	1024	64	8	128
		1152	2048	128	8	128
	2	384	2048	128	8	128
		2304	4096	256	8	128

Table 64. Valid SRAM1RN Configurations (Continued)

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
8	1	256	2048	128	8	128
		2304	4096	256	8	128
	2	768	4096	256	8	128
		4608	8192	512	8	128
16	1	256	4096	256	8	64
		4608	8192	512	8	64
	2	1536	8192	512	8	64
		9216	16384	1024	8	64
32	1	512	8192	512	8	32
		9216	16384	1024	8	32
	2	3072	16384	1024	8	32
		18432	32768	2048	8	32

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM1RNwwwwwXbbbDddSsM1

where:

SRAM1RN	=	high density one-port SRAM without fuse redundancy name
w	=	total number of words: 5 digits
b	=	data width in bits: 3 digits
d	=	decode option: 2 digits
s	=	subarray option: 1 digit
M1	=	array-clocked timing mode only

A representative example would be:

SRAM1RN01024X008D16S1M1	A 1024-word x 8-bit one-port SRAM, using the 16:1 decode option and one subarray.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

BIST1R—BIST Controller for SRAM1R

Features

- Complete test of all array functions
- One controller required for each SRAM1R
- System LBIST compatible

The key features of the macro are summarized in Table 65.

Table 65. BIST Controller Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Macro dimensions	419 x 31 chip unit cells
Macro area	12,989 chip unit cells
DC test methodology	BIST
AC test methodology	Access time
Global porosity on M1	0%
Global porosity on M2	50%
Global porosity on M3	75%

BIST Description

The BIST controller performs all of the necessary DC tests for the arrays during product test by applying addresses, data inputs, bit write controls, and read/write controls to the array. The BIST control signals are multiplexed with the functional inputs for the address, data, and control signals with minimal impact on the SRAM's access and setup and hold times.

Usage Requirements

Whenever compilable SRAM1Rs with fuse redundancy are used, the BIST1R controller must be used to generate the BIST test patterns required to verify the SRAMs during

product test. One BIST1R must be used for every SRAM1R of any configuration.

To facilitate scan output of fuse redundancy values, BIST1R macros must be placed at scan-out end of LSSD scan chains, no more than three deep from the end, with no other scannable elements between them. BIST1R macros cannot be placed in the same LSSD scan chain with an embedded DRAM.

Symbol Naming Conventions

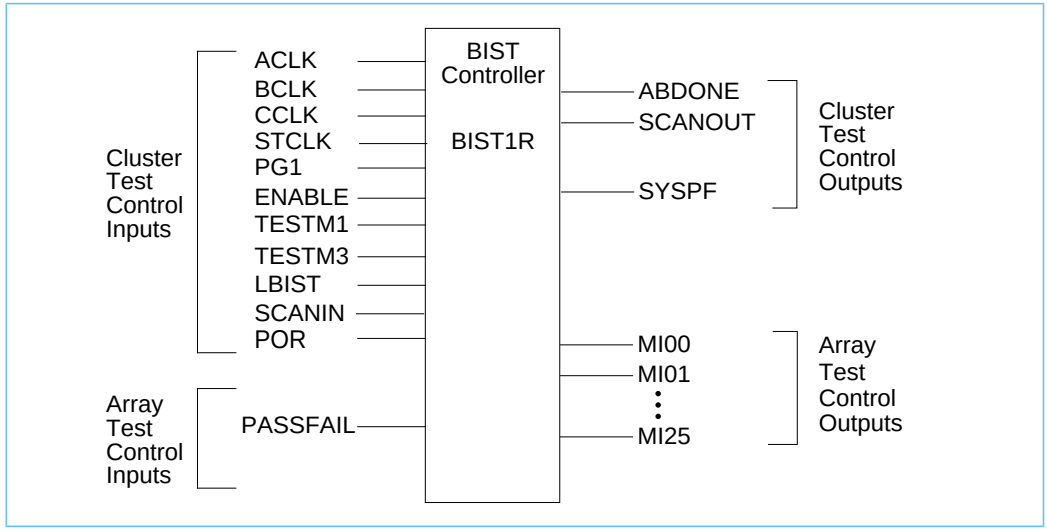
The BIST1R controller does not have a dependence on the SRAM configurations to which it is connected. Therefore, there is a single instance named BIST1R.

Logical Description

Logical Symbol

A symbolic representation of the BIST1R controller is shown in Figure 35.

Figure 35. BIST1R Controller Logic Symbol



Pin Definitions

Table 66 on page 166 summarizes the function and use of the macro pins shown in Figure 35. Information describing the use of these pins in various test modes can be obtained from an IBM ASICs representative.

Table 66. Pin Definitions

Pin	Description
ACLK	The A clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD A clocks on the chip. The A clock is active high during scan operations and must be held low during array mode operation.
BCLK	The B clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD B clocks on the chip. The B clock is active high during scan and BIST operations.
CCLK	The C clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is active high during BIST operations and must come from a primary input but can be common with other LSSD C clocks on the chip. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
STCLK	The system test oscillator clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
PG1	The C clock gate pin is used to gate the CCLK signal. This pin is usually held high, unless it is used during LBIST operations.
ENABLE	The self-test clock enable pin is used to gate the STCLK signal. This pin is usually held high, unless it is used during LBIST operations.
TESTM1	The TESTM1 pin is used together with the TESTM3 pin to set the test state of the BIST controller and the attached arrays. TESTM1 is held low for functional operation of the array.
TESTM3	The TESTM3 pin is used together with the TESTM1 pin to set the test state of the BIST controller and the attached arrays. TESTM3 is held low for functional operation of the array and must be routed from a chip primary input.
POR	The power-on-reset pin is used to initialize the fuse latches before operation of the SRAM can occur. POR must be brought high, then returned low before any operation of the SRAM, and must be held low for all subsequent functional or test operations. The POR pin must be pulsed high, with the TESTM3 pin held low, for a pulse width of 50 ns. The first functional access of the SRAM can occur 50 ns after POR returns low.

Table 66. Pin Definitions (Continued)

Pin	Description
LBIST	The LBIST pin must be held high during system LBIST testing to block the B clock to the SRAMs. It must be held low during logic flush and scan operations.
PASSFAIL	The PASSFAIL pin is an array test input which receives the pass/fail state of the array on each BIST test cycle.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the BIST controller. The scan-in pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
ABDONE	The ABIST done pin goes high when the BIST controller has completed issuing test patterns to the arrays within its cluster. This pin does not have to be connected.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the BIST controller. The scan-out pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip. BIST1R controllers must be placed at the end of a scan chain no more than three deep to balance the manufacturing test observability of fuse redundancy values from multiple scan chains within the 256 fail-count limitation. As a result, the SCANOUT pin must connect to a chip scan out, or to the SCANIN of another BIST1R controller, stacked no more than three deep. See “Usage Requirements” on page 164.
SYSPF	The SYSPF pin is a cluster test output which allows the BIST pass/fail bit to be observed by on-chip system test logic without requiring a scan operation. This pin is not required to be connected.
MI00–MI25	The MI array test pins are only routed to the arrays under the control of the BIST macro and control the SRAMs during BIST testing. The MI pins must not be wired to any other circuits within the ASIC chip.

Operational Modes

For information on integrating the BIST1R controller into a chip test environment, contact your IBM ASICs representative.

Macro Footprint

The BIST1R controller is rectangular.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is fixed for all configurations at 210.

BIST Test Mode Clock Cycle Calculations

The number of clock cycles required to complete the BIST test is fixed at 2,423,893 cycles.

BIST1RN—BIST Controller for SRAM1RN without Fuse Redundancy

Features

BIST1RN is physically and logically identical to the BIST1R controller for SRAM1R. The models and technical data for BIST1RN are BIST1R copies. BIST1RN is a separate entity only to distinguish the chip connection requirements, and test sequences which differ from the BIST1R in the following two ways:

- Must only connect to SRAM1RN arrays; one controller required for each SRAM1RN
- Flags an SRAM as failing on first fail; does not collect data on failing addresses

The key features of the macro are summarized in Table 67.

Table 67. BIST Controller Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Macro dimensions	419 x 31 chip unit cells
Macro area	12,989 chip unit cells
DC test methodology	BIST
AC test methodology	Access time
Global porosity on M1	0%
Global porosity on M2	TBD%

BIST Description

The BIST controller performs all of the necessary DC tests for the arrays during product test by applying addresses, data inputs, bit write controls, and read/write controls to the array. The BIST control signals are multiplexed with the functional inputs for the address, data, and control signals with minimal impact on the SRAM’s access and setup and hold times.

Usage Requirements

Whenever compilable SRAM1RNs without fuse redundancy are used, the BIST1RN controller must be used to generate the BIST test patterns required to verify the SRAMs during product test. One BIST1RN must be used for every SRAM1RN of any configuration.

The placement of BIST1RNs in scan chains is not restricted the way BIST1R is. Any number can be placed anywhere in a scan chain.

Symbol Naming Conventions

The BIST1RN controller does not have a dependence on the SRAM configurations to which it is connected. Therefore, there is a single instance named BIST1RN.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is fixed for all configurations at 210.

BIST Test Mode Clock Cycle Calculations

The number of clock cycles required to complete the BIST test is fixed at 2,423,893 cycles.

FUSE—Fuse Macro for SRAM1R

Features

- Laser fuse macro for implementing wordline redundancy in the SRAM1R compilable one-port SRAM

The key features of the macro are summarized in Table 68.

Table 68. FUSE Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Macro area	9120 chip unit cells
DC test methodology	Multiple array BIST
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	0%
Global porosity on M4	0%
Global porosity on M5	0%

Macro Description

The fuse macro contains metal fuses which can be blown with a laser to implement redundancy in the SRAM1R compilable array.

Usage Requirements

Whenever an SRAM1R compilable one-port SRAM is used, one or two fuse macros must be used to provide fuse redundancy capability. If a one subarray SRAM1R is used, an S1-type fuse macro is used. If a two subarray SRAM1R is used, both an S1-type and an S2-type fuse macro must be used. Fuse macros cannot be shared between SRAM1R instances.

Symbol Naming Conventions

The fuse macro name must match the chip image type on which it is to be used.

FUSESsppmmm
where:

FUSE = Fuse macro name
s = subarray to connect to: 1 or 2
pp = package type: C4 = C4 image, or WB = wire bond image
mmm = last metal level name

Table 69. Fuse Naming Conventions and Dimensions

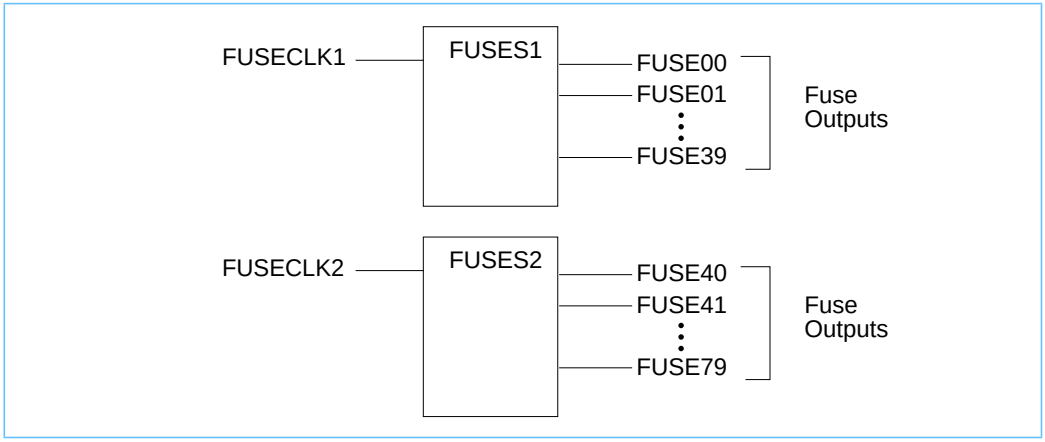
Fuse Macro Name	Image Type	Last Metal Level	Dimensions (cells x cells)	Total Area (cells)
FUSES1WBMZ4 FUSES2WBMZ4	wire bond	mz4	228 x 32	7296
FUSES1WBMZ5 FUSES2WBMZ5	wire bond	mz5	228 x 32	7296
FUSES1WBMZ6 FUSES2WBMZ6	wire bond	mz6	228 x 32	7296
FUSES1WBMT4 FUSES2WBMT4	wire bond	mt4	228 x 32	7296
FUSES1WBMT5 FUSES2WBMT5	wire bond	mt5	228 x 32	7296
FUSES1WBMT6 FUSES2WBMT6	wire bond	mt6	228 x 32	7296
FUSES1C4MZ5 FUSES2C4MZ5	peripheral C4	mz5	384 x 19	7296
FUSES1C4MZ6 FUSES2C4MZ6	peripheral C4	mz6	228 x 32	7296
FUSES1C4MZ6 FUSES2C4MZ6	array C4	mz6	228 x 32	7296
FUSES1C4LM6 FUSES2C4LM6	array C4	lm6	230 x 38	8740

Logical Description

Logical Symbol

A symbolic representation of the fuse macro is shown in Figure 36.

Figure 36. FUSE Macro Logic Symbol



Pin Definitions

Table 70 summarizes the function and use of the macro pins shown in Figure 36. Information describing the use of these pins in various test modes can be obtained from an IBM ASICs representative.

Table 70. Pin Definitions

Pin	Description
FUSECLK1, FUSECLK2	The fuse clock pin must be connected to the SRAM1R array to drive the power-on-reset clock which loads the fuse data into the SRAM. Pin FUSECLK1 will appear on an S1 macro, and FUSECLK2 will appear on an S2 macro.
FUSE00–FUSE79	The fuse output pins to connect to the SRAM. They connect to the pins with corresponding names on the SRAM1R inputs. Pins FUSE00–FUSE39 appear on an S1 macro, and pins FUSE40–FUSE79 appear on an S2 macro. All must be connected, and no other elements can be connected to these nets.

Operational Modes

For information on integrating the fuse macros into a chip test environment, contact your IBM ASICs representative.

Macro Footprint

The fuse macros are rectangular.

Scan Chain Definition

LSSD Latch Count Calculations

There are no scannable latches in the fuse macro.

SRAM2B—Compilable Dual-Port SRAM

Features

- Fully static array
- Configurations up to 8K words or 128 bits supported
- Two independent read/write ports
- Does not resolve read address equals write address collisions
- Multiple decode options for performance and area optimization
- Latched output data until next read cycle
- Bit write control for data masking
- Multiple array built-in self-test
- Single clock edge operation per port through use of self-timed restore

The key features of the macro are summarized in Table 71.

Table 71. SRAM2B Dual-Port SRAM Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1, 8:1, or 16:1
Maximum macro size	256K (262,144) bits
Maximum words	8192 words
Minimum words	64 words
Maximum data width	128 bits
Minimum data width	8 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	37%

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, and DECODE, options are shown in Table 72.

Table 72. SRAM2B Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–8192	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 73, “Valid SRAM2B Configurations,” on page 176.
NBIT	8–128	The number of bits per word in the array.
DECODE	4, 8, or 16	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes.

The resultant ranges of valid array sizes are shown in Table 73.

Table 73. Valid SRAM2B Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	64	2048	64	8	128
8	1	128	4096	128	8	64
16	1	256	8192	256	8	32

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 73, “Valid SRAM2B Configurations”.

If the array is clocked with an address larger than NWORD applied at the address input ports, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM2BwwwwXbbbDddSsMm

where:

SRAM2B = two-port SRAM name
w = total number of words: 4 digits
b = data width in bits: 3 digits
d = decode option: 2 digits
s = subarray option: 1 digit
m = timing mode: 1 digit
1 = array-clocked mode

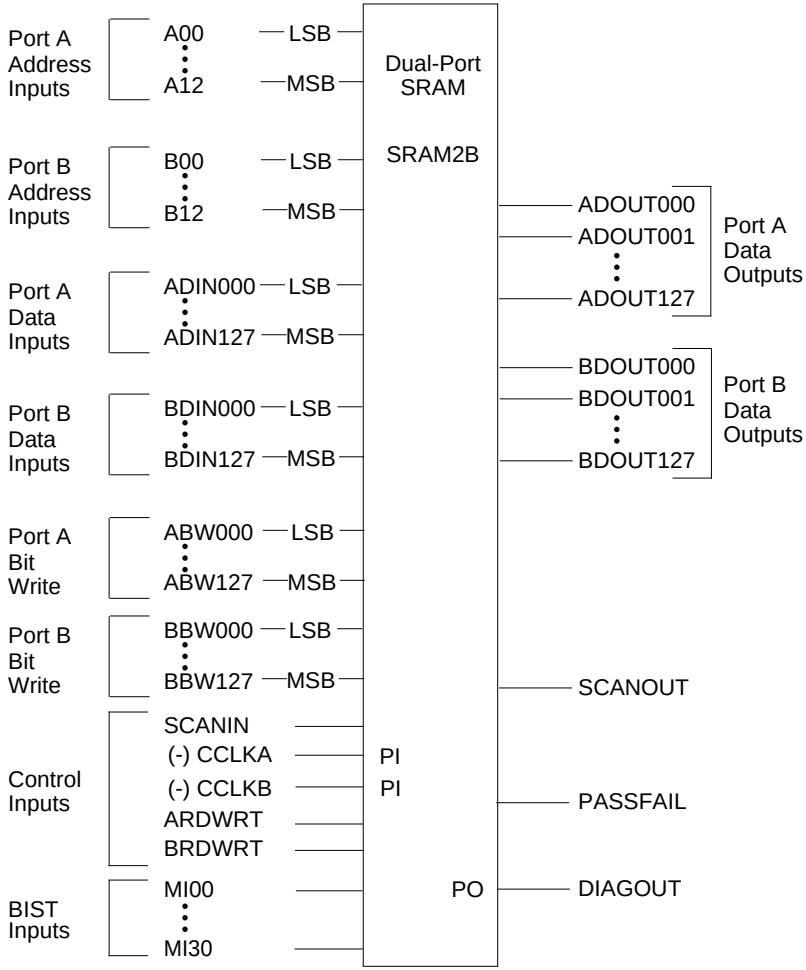
A representative example would be:

SRAM2B0256X064D04S1M1	A 256-word x 64-bit dual-port SRAM, using the 4:1 decode option and one subarray, with array-clocked functional mode timing.

Logical Description

A symbolic representation of the dual-port SRAM is shown in Figure 37.

Figure 37. SRAM2B Dual-Port SRAM Logic Symbol



Pin Definitions

Table 74 summarizes the function and proper usage of the macro pins shown in Figure 37 on page 178. The control and input pins must be stable before the clocks initiate a read or write access of the array. Pin timing relationships are described later.

Table 74. Pin Definitions

Pin	Description
A00–A12	The port A address input pins define the address to which input data will be written, or from which output data will be read for port A. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation, words = 2^N. The bit address occupies the least significant bits, using: A00 and A01 for decode = 4:1; A00, A01, and A02 for decode = 8:1; or A00, A01, A02, and A03 for decode = 16:1. The word address follows. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
B00–B12	The port B address input pins follow the same conventions as the port A address input pins. There must be an equal number of port A and port B address pins.
ADIN000–ADIN127	The port A data input pins provide the input data to be written to port A.The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the ADIN000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
BDIN000–BDIN127	The port B data input pins follow the same conventions as the port A data input pins. There must be an equal number of port A and port B data pins.
ABW000–ABW127	The port A bit write input pins allow masking of the input data on port A. The bit write pins are active high, and one pin is required for each data input bit. If the pin is held high, the corresponding data input bit is written into the array. If the pin is held low, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pins are used starting at the ABW000 least significant bit and counting upwards. If a data input pin is not used, then the corresponding bit write control pin will not appear in the logical or physical models either. However, a bit write control pin is always allocated for every data input pin used. If bit write control is not required, then these pins must be tied high.
BBW000–BBW127	The port B bit write input pins follow the same conventions as the port A bit write pins.

Table 74. Pin Definitions (Continued)

Pin	Description
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
CCLKA	The CCCLKA pin initiates a read or write access of port A on its falling edge during functional mode operations. This pin must come from a primary input.
CCLKB	The CCCLKB pin initiates a read or write access of port B on its falling edge during functional mode operations. This pin must come from a primary input.
ARDWRT	The ARDWRT pin causes a read of port A to be performed when held high or a write to be performed when held low when the CCCLKA is strobed active.
BRDWRT	The BRDWRT pin causes a read of port B to be performed when held high or a write to be performed when held low when the CCCLKB is strobed active.
MI00–MI30	The BIST pins must be connected to an accompanying BIST2B controller as they control the SRAM during BIST testing. The number required is fixed at 31. The MInn pins must not be connected to anything other than the BIST2B controller.
ADOUT000–ADOUT127	The port A data output pins provide the output data read from port A.The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the ADOUT000 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read of port A. Write operations do not affect the data output pins.
BDOUT000–BDOUT127	The port B data output pins follow the same conventions as the port A data output pins. There must be an equal number of port A and port B data pins.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during MABIST testing and must be routed to the accompanying BIST2B controller for the array. The PASSFAIL pin must not be connected to anything other than the BIST2B controller. Note that this pin is “nonvalidated” and as a result cannot be monitored directly to determine if there are fails in the array. The BIST2B controller “validates” the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

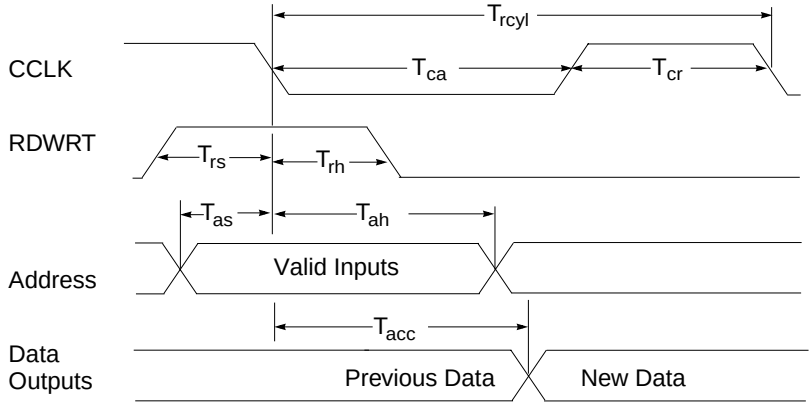
Array functional operation is the normal operation of the SRAM when the BIST2B controller is inactive. Array functional operations include read and write.

Read Operation

- RDWRT signal held high or brought high before the CCLK edge
- Address inputs stabilized before the CCLK edge
- CCLK falling initiates the read cycle
- Data is read to the data output pins from the address in the array.

The timings for a valid read operation on either port are shown in Figure 38.

Figure 38. SRAM2B Read Timings

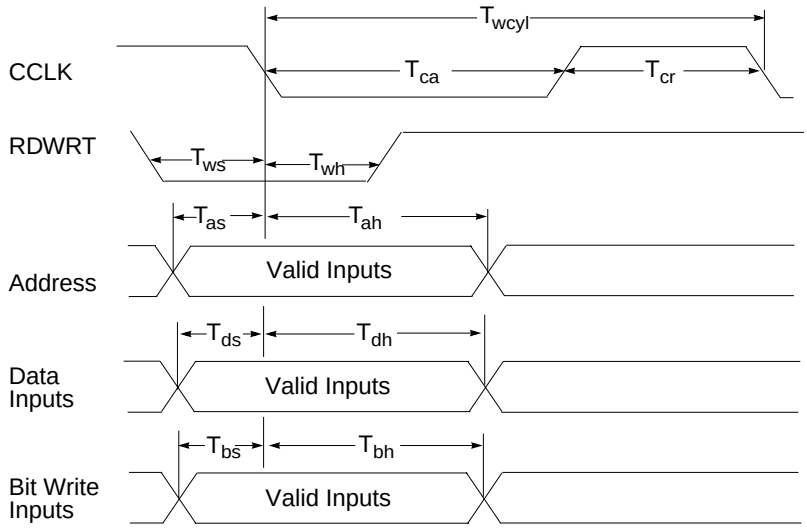


Write Operation

- RDWRT signal held low or brought low before the CCLK edge
- Address, data, and bit write inputs stabilized before the CCLK edge
- CCLK falling initiates the write cycle
- Data input is written to the address in the array.

The timings for a valid write operation on either port are shown in Figure 39.

Figure 39. SRAM2B Write Timings



Address Collisions

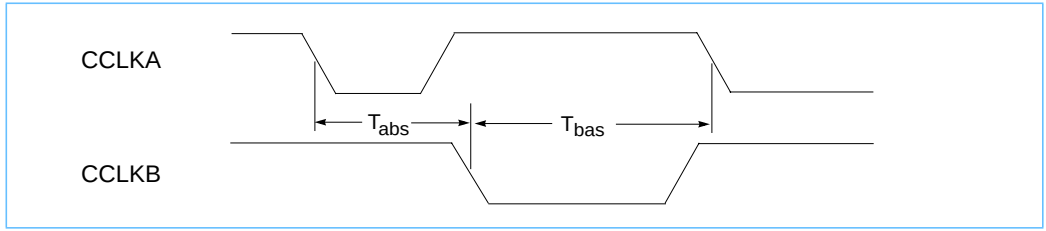
Special cases arise when both port A and port B address inputs are equal and read and write operations are performed. If both ports are performing a read, there is no concern, as the current address contents will appear on both data output ports. If one port is performing a read while the other is performing a write, the timing relationship between the CCLKA and CCLKB edges will determine whether the previous data, new data, or unknown data will appear on the output port being read. However, the correct input data will be stored in the written memory location. If both ports are performing a write, the timing relationship between the CCLKA and CCLKB edges will determine whether the address location stores the port A or port B input data, or unknown data.

To avoid conflicts where unknown data can be written to a memory location or be read to the outputs, non-overlap constraints are defined for the CCLKA and CCLKB clocks as shown in Figure 40. There are two modes defined in the delay rules for this SRAM:

Clock_Synch	The default timing mode, it contains the T_{abs} and T_{bas} non-overlap checks.
Clock_Asynch	An optional mode which does not contain the T_{abs} and T_{bas} non-overlap checks, and which should only be used if address collision is handled elsewhere in the system, either by ensuring that addresses will never be equal, or by expecting unknown “X” data to result when they are. If these conditions are met, then using the Clock_Asynch mode will eliminate the timing errors that would otherwise result when doing timing analysis with non-synchronized CCLKA and CCLKB.

The T_{abs} and T_{bas} non-overlap checks are coded in the logical simulation models for the SRAM, and will only be completely checked when running delay simulation with back-annotated timings.

Figure 40. SRAM2B Clock Separation Requirements



Delay Tables

Table 75 and Table 76 show setup and hold delays for representative “small” and “large” SRAM2B arrays.

Table 75. “Small” SRAM2B0256X032D04S1M1

Timing Parameter	Abbreviation	Minimum (ns)
CCLK (A or B) minimum active time	T_{ca}	0.4
CCLK (A or B) minimum restore time	T_{cr}	0.4
RDWRT (A or B) setup time before read	T_{rs}	0.4
RDWRT (A or B) hold time after read	T_{rh}	0.1
RDWRT (A or B) setup time before write	T_{ws}	0.4
RDWRT (A or B) hold time after write	T_{wh}	0.1
Data in (A or B) setup time	T_{ds}	0.4
Data in (A or B) hold time	T_{dh}	0.3
Bit write (A or B) setup time	T_{bs}	0.3
Bit write (A or B) hold time	T_{bh}	0.3
Address (A or B) setup time	T_{as}	0.4
Address (A or B) hold time	T_{ah}	0.4
CCLKA separation before CCLKB	T_{abs}	1.5
CCLKB separation before CCLKA	T_{bas}	1.5
Read cycle time	T_{rcyl}	2.4
Write cycle time	T_{wcyl}	2.4
Access time	T_{acc}	1.9

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 76. "Large" SRAM2B8192X032D16S1M1

Timing Parameter	Abbreviation	Minimum (ns)
CCLK (A or B) minimum active time	T_{ca}	0.4
CCLK (A or B) minimum restore time	T_{cr}	0.4
RDWRT (A or B) setup time before read	T_{rs}	0.4
RDWRT (A or B) hold time after read	T_{rh}	0.1
RDWRT (A or B) setup time before write	T_{ws}	0.4
RDWRT (A or B) hold time after write	T_{wh}	0.1
Data in (A or B) setup time	T_{ds}	0.7
Data in (A or B) hold time	T_{dh}	0.6
Bit write (A or B) setup time	T_{bs}	0.7
Bit write (A or B) hold time	T_{bh}	0.5
Address (A or B) setup time	T_{as}	1.3
Address (A or B) hold time	T_{ah}	0.4
CCLKA separation before CCLKB	T_{abs}	3.2
CCLKB separation before CCLKA	T_{bas}	3.2
Read cycle time	T_{rcyl}	5.5
Write cycle time	T_{wcyl}	5.5
Access time	T_{acc}	4.5

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a SRAM2B for a particular application, use the following equation:

$$P = [((A_{readA} \times RC_{int} + A_{writeA} \times WC_{int}) \times F_{port\ A}) + ((A_{readB} \times RC_{int} + A_{writeB} \times WC_{int}) \times F_{port\ B})] \times V^2_{dd}$$

where:

- P = Power in microwatts
- RC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a read access on every cycle. RC_{int} has the same value for both port A and port B. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a write access on every cycle. WC_{int} has the same value for both port A and port B.
- A_{readA} = Read activity factor for port A, which is the fraction of the total CCLKA clock cycles that a read access is performed on port A (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- A_{readB} = Read activity factor for port B, which is the fraction of the total CCLKB clock cycles that a read access is performed on port B (a value between 0 and 1).
- A_{writeA} = Write activity factor for port A, which is the fraction of the total CCLKA clock cycles that a write access is performed on port A (a value between 0 and 1). In typical applications, the write activity is often less than the read activity, as the contents of an SRAM are read more often than they are replaced. For this 2-port SRAM, the

sum of the read and write activity factors must be less than or equal to 1 for each port, but the sum of both ports can be greater than 1, but must be less than or equal to 2.

- A_{writeB} = Write activity factor for port B, which is the fraction of the total CCLKB clock cycles that a write access is performed on port B (a value between 0 and 1).
- $F_{port\ A}$ = Clock frequency applied to the port A CCLKA, in MHz.
- $F_{port\ B}$ = Clock frequency applied to the port B CCLKB, in MHz.
- V_{dd} = Power supply voltage of the chip in volts.

Array Area and Footprint

Figure 41 shows the general shape of the SRAM, and the relative locations of the pins within it. The dimensions for a representative configuration can be obtained from the sizing routines available on the World Wide Web. Access to the Web page can be obtained from an IBM ASICs representative.

Figure 41. SRAM2B Footprint

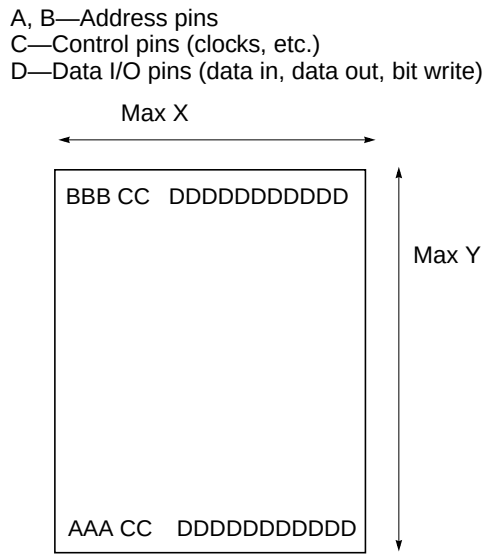


Table 77. SRAM2B Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Sub	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Write Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
256 x 16	4	1	1.8	2.2	36	31	58558	874	67
256 x 32	4	1	1.9	2.4	54	43	86430	1290	67
256 x 64	4	1	2.3	2.7	90	69	142174	2122	67
256 x 128	4	1	3.1	3.4	163	120	253662	3786	67
1024 x 16	8	1	2.1	2.6	44	41	108360	1290	84
1024 x 32	8	1	2.6	3.0	68	62	178248	2122	84
1024 x 64	4	1	2.9	3.6	102	96	311934	2122	147
1024 x 128	4	1	3.7	4.3	180	166	556542	3786	147
4096 x 16	16	1	3.0	3.6	73	71	290714	2122	137
4096 x 32	8	1	3.6	4.9	97	99	517768	2122	244
4096 x 64	8	1	4.4	5.5	159	162	923784	3786	244
8192 x 16	16	1	3.6	4.9	92	90	517768	2122	244
8192 x 32	16	1	4.6	5.5	151	145	923784	3786	244

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read or write operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the SRAM and can be calculated using the following equation:

Total scan latches = 29 + (2 x NBIT) (the data word width)

Multiple Array BIST Testing

MABIST Controller Interface

Every instance of an SRAM2B array on a chip must be connected to a BIST2B controller. Up to 16 SRAM2B arrays can be connected to a single BIST2B controller.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

BIST2B—BIST Controller for SRAM2B

Features

- Complete test of all array functions
- Up to 16 arrays tested in parallel from one controller
- System LBIST compatible

The key features of the macro are summarized in Table 78.

Table 78. BIST Controller Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Macro dimensions	437 x 20 chip unit cells
Macro area	8740 chip unit cells
DC test methodology	Multiple array BIST
AC test methodology	Access time
Global porosity on M1	0%
Global porosity on M2	50%
Global porosity on M3	75%

BIST Description

The BIST controller performs all of the necessary DC tests for the arrays during product test by applying addresses, data inputs, bit write controls, and read/write controls to the array. The BIST control signals are multiplexed with the functional inputs for the address, data, and control signals with minimal impact on the SRAM's access, setup, and hold times.

Usage Requirements

Whenever compilable dual-port SRAMs are used, the BIST2B controller must be used to generate the BIST test patterns required to verify the SRAMs during product test. BIST2B can be used to control from one to sixteen SRAM2Bs of any configuration.

Symbol Naming Conventions

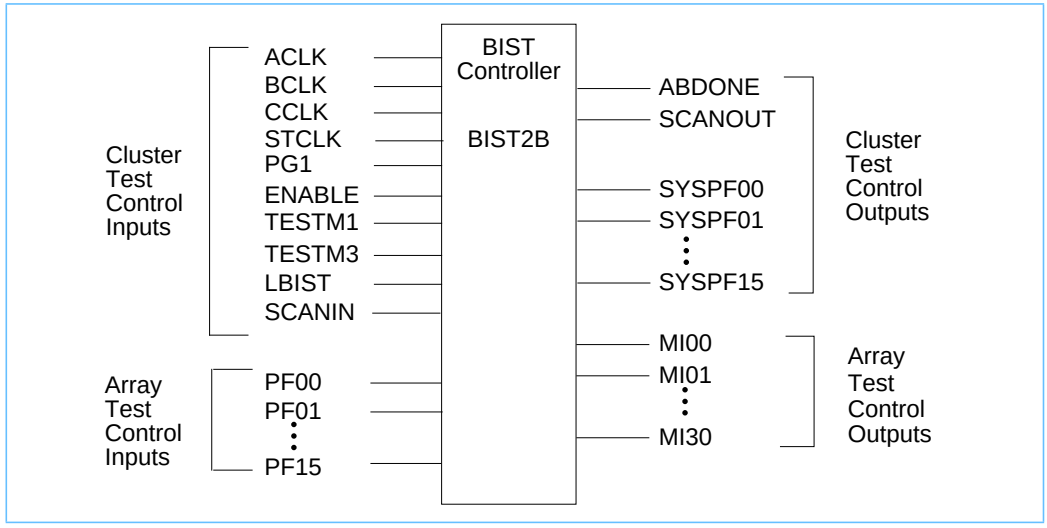
The BIST2B controller does not have a dependence on the SRAM to which it is connected. Therefore, there is a single instance named BIST2B.

Logical Description

Logical Symbol

A symbolic representation of the BIST2B controller is shown in Figure 42.

Figure 42. BIST2B Controller Logic Symbol



Pin Definitions

Table 79 summarizes the function and use of the macro pins shown in Figure 42. Information describing the use of these pins in various test modes can be obtained from an IBM ASICs representative.

Table 79. Pin Definitions

Pin	Description
ACLK	The A clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD A clocks on the chip. The A clock is active high during scan operations and must be held low during array mode operation.
BCLK	The B clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD B clocks on the chip. The B clock is active high during scan and BIST operations.
CCLK	The C clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is active high during BIST operations and must come from a primary input but can be common with other LSSD C clocks on the chip. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
STCLK	The system test oscillator clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
PG1	The C clock gate pin is used to gate the CCLK signal. This pin is usually held high, unless it is used during LBIST operations.
ENABLE	The self-test clock enable pin is used to gate the STCLK signal. This pin is usually held high, unless it is used during LBIST operations.
TESTM1	The TESTM1 pin is used together with the TESTM3 pin to set the test state of the BIST controller and the attached arrays. TESTM1 is held low for functional operation of the array.
TESTM3	The TESTM3 pin is used together with the TESTM1 pin to set the test state of the BIST controller and the attached arrays. TESTM3 is held low for functional operation of the array and must be routed from a chip primary input.
LBIST	The LBIST pin must be held high during system LBIST testing to block the B clock to the SRAMs. It must be held low during logic flush and scan operations.

Table 79. Pin Definitions (Continued)

Pin	Description
PF00–PF15	The PF pins are array test inputs which receive the pass/fail state of the arrays on each BIST test cycle. One PF pin is connected to each array being tested. Unused PF pins must be tied to ground.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the BIST controller. The scan-in pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
ABDONE	The ABIST done pin goes high when the BIST controller has completed issuing test patterns to the arrays within its cluster. This pin does not have to be connected.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the BIST controller. The scan-out pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
SYSPF00–SYSPF15	The SYSPF pins are cluster test outputs which allow the BIST pass/fail bits to be observed by on-chip system test logic without requiring a scan operation. These pins are not required to be connected.
MI00–MI30	The MI array test pins are only routed to the arrays under the control of the BIST macro and control the SRAMs during BIST testing. The MI pins must not be wired to any other circuits within the ASIC chip.

Operational Modes

For complete documentation on integrating the BIST2B controller into a chip test environment, contact your IBM ASICs representative.

Macro Footprint

The BIST2B controller is rectangular, 437 unit cells wide by 20 cells high, resulting in a total area of 8740 unit cells.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is fixed at:

BIST2B scan latches = 122

MABIST Test Mode Clock Cycle Calculations

The number of clock cycles required to complete the BIST test is fixed at:

BIST2B clock cycles = 2,157,832

SRAM4G—Compilable Sequential Four-Port SRAM

Features

- Fully static array
- Configurations up to 2K words or 40 bits supported
- Two independent read-followed-by-write ports
- Does not resolve read address equals write address collisions
- Multiple decode options for performance and area optimization
- Latched output data until next read cycle
- Bit write control for data masking
- Multiple array built-in self-test
- Single clock edge operation per port through use of self-timed restore

The key features of the macro are summarized in Table 80.

Table 80. SRAM4G Four-Port SRAM Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Array architecture	M2 bitlines
Array column decode options	4:1 or 8:1
Maximum macro size	80K (81,920) bits
Maximum words	2048 words
Minimum words	64 words
Maximum data width	40 bits
Minimum data width	4 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	TBD%

Keyword Definitions and Limits

The resultant limits and conditions on the NWORD, NBIT, and DECODE, options are shown in Table 81.

Table 81. SRAM4G Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64–2048	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 82, “Valid SRAM4G Configurations,” on page 196.
NBIT	4–40	The number of bits per word in the array.
DECODE	4 or 8	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes.

The resultant ranges of valid array sizes are shown in Table 82.

Table 82. Valid SRAM4G Configurations

Decode	Subarray	Word Depth		Word Depth Granularity	Data Width	
		Min	Max		Min	Max
4	1	64	1024	64	4	40
8	1	128	2048	128	4	40

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 82, “Valid SRAM4G Configurations”.

If the array is clocked with an address larger than NWORD applied at the address input ports, no wordline in the array will be activated. Therefore, if the array is in write mode, the array contents will remain unchanged. However, if the array is in read mode, the output circuitry will be activated, and unknown, or “X,” data will be placed in the data output latches.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

SRAM4GwwwwXbbbDddSsMm

where:

SRAM4G = four-port SRAM name
w = total number of words: 4 digits
b = data width in bits: 3 digits
d = decode option: 2 digits
s = subarray option: 1 digit
m = timing mode: 1 digit
1 = array-clocked mode

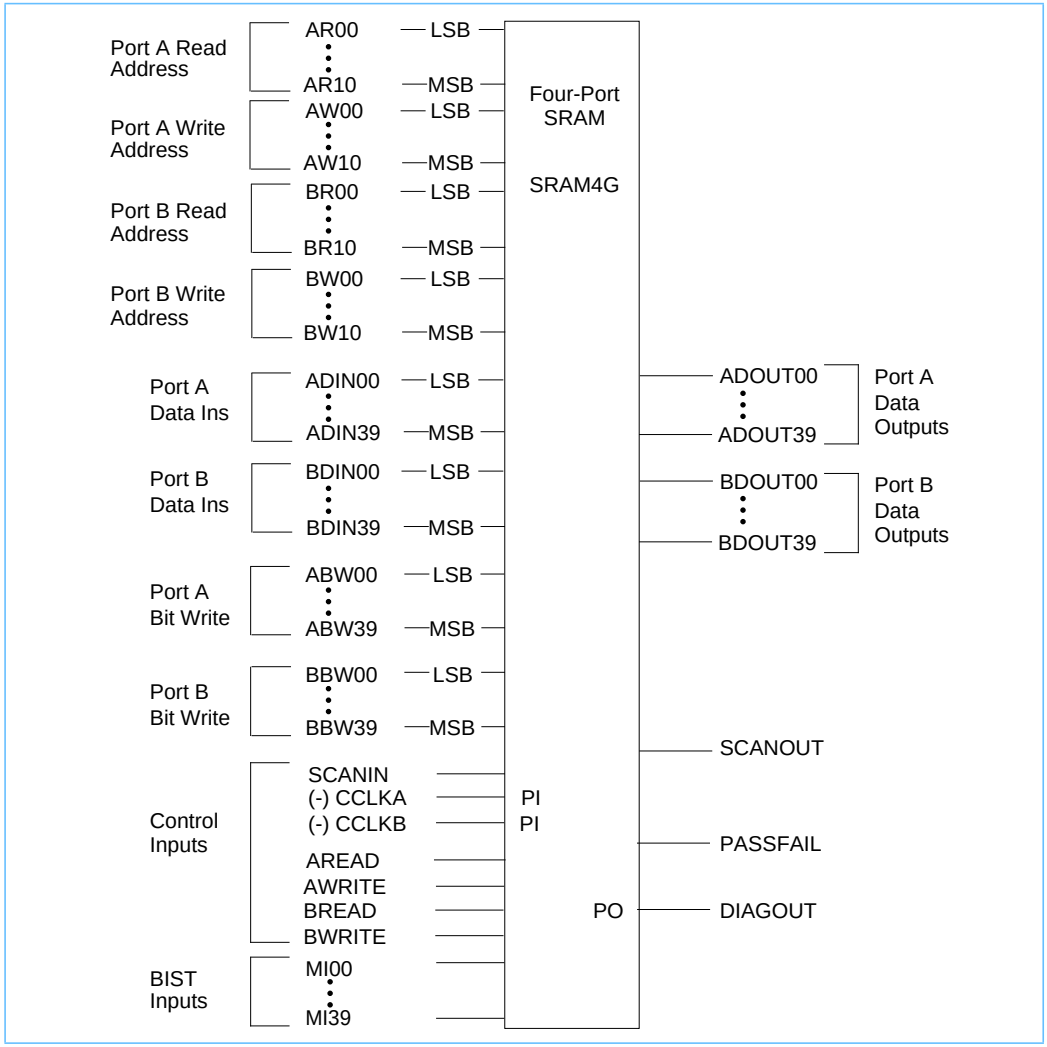
A representative example would be:

SRAM4G0256X032D04S1M1	A 256-word x 32-bit four-port SRAM, using the 4:1 decode option and one subarray, with array-clocked functional mode timing.

Logical Description

A symbolic representation of the four-port SRAM is shown in Figure 43.

Figure 43. SRAM4G Four-Port SRAM Logic Symbol



Pin Definitions

Table 83 summarizes the function and proper usage of the macro pins shown in Figure 43 on page 198. The control and input pins must be stable before the clocks initiate a read or write access of the array. Pin timing relationships are described later.

Table 83. Pin Definitions

Pin	Description
AR00–AR10	The port A read address input pins define the address from which output data will be read for port A. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation, words = 2^N. The bit address occupies the least significant bits, using: AR00 and AR01 for decode = 4:1 or AR00, AR01, and AR02 for decode = 8:1. The word address follows. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
AW00–AW10	The port A write address input pins define the address to which input data will be written into port A. These pins follow the same conventions as the port A read address input pins. There must be an equal number of address pins on all four ports.
BR00–BR10	The port B read address input pins define the address from which output data will be read for port B. These pins follow the same conventions as the port A address input pins. There must be an equal number of address pins on all four ports.
BW00–BW10	The port B write address input pins define the address to which input data will be written into port B. These pins follow the same conventions as the port A address input pins. There must be an equal number of address pins on all four ports.
ADIN00–ADIN39	The port A data input pins provide the input data to be written to port A.The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the ADIN00 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
BDIN00–BDIN39	The port B data input pins follow the same conventions as the port A data input pins. There must be an equal number of data pins on all four ports.

Table 83. Pin Definitions (Continued)

Pin	Description
ABW00–ABW39	The port A bit write input pins allow masking of the input data on port A. The bit write pins are active high, and one pin is required for each data input bit. If the pin is held high, the corresponding data input bit is written into the array. If the pin is held low, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The bit write control input pins perform no function during a read of the array. Pins are used starting at the ABW00 least significant bit and counting upwards. If a data input pin is not used, then the corresponding bit write control pin will not appear in the logical or physical models either. However, a bit write control pin is always allocated for every data input pin used. If bit write control is not required, then these pins must be tied high.
BBW000–BBW39	The port B bit write input pins follow the same conventions as the port A bit write pins.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
CCLKA	The CCCLKA pin initiates a read followed by a write access of port A on its falling edge during functional mode operations. This pin must come from a primary input.
CCLKB	The CCCLKB pin initiates a read followed by a write access of port B on its falling edge during functional mode operations. This pin must come from a primary input.
AREAD	The AREAD pin causes a read of port A to be performed when held high when the CCLKA is strobed active.
AWRITE	The AWRITE pin causes a write of port A to be performed when held high when the CCLKA is strobed active.
BREAD	The BREAD pin causes a read of port B to be performed when held high when the CCLKB is strobed active.
BWRITE	The BWRITE pin causes a write of port B to be performed when held high when the CCLKB is strobed active.
MI00–MI39	The BIST pins must be connected to an accompanying BIST4G controller as they control the SRAM during BIST testing. The number required is fixed at 40. The MInn pins must not be connected to anything other than the BIST4G controller.

Table 83. Pin Definitions (Continued)

Pin	Description
ADOUT00-ADOUT39	The port A data output pins provide the output data read from port A.The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the ADOUT00 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read of port A. Write operations do not affect the data output pins.
BDOUT00–BDOUT39	The port B data output pins follow the same conventions as the port A data output pins. There must be an equal number of data pins on all four ports.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the SRAM. The SRAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during MABIST testing and must be routed to the accompanying BIST4G controller for the array. The PASSFAIL pin must not be connected to anything other than the BIST4G controller. Note that this pin is “nonvalidated” and as a result cannot be monitored directly to determine if there are fails in the array. The BIST4G controller “validates” the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

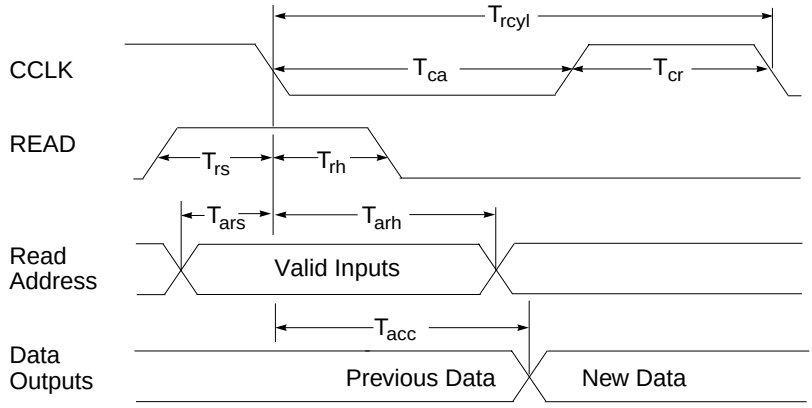
Array functional operation is the normal operation of the SRAM when the BIST4G controller is inactive. Array functional operations include read and write.

Read Operation

- READ signal held high or brought high before the CCLK edge
- Address inputs stabilized before the CCLK edge
- CCLK falling initiates the read cycle
- Data is read to the data output pins from the address in the array.

The timings for a valid read operation on either port are shown in Figure 44.

Figure 44. SRAM4G Read Timings

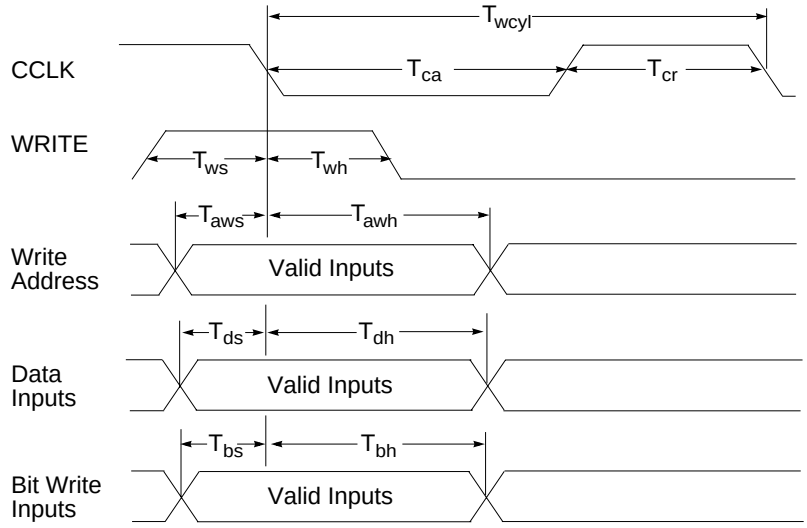


Write Operation

- WRITE signal held high or brought high before the CCLK edge
- Address, data, and bit write inputs stabilized before the CCLK edge
- CCLK falling initiates the write cycle
- Data input is written to the address in the array.

The timings for a valid write operation on either port are shown in Figure 45 on page 203.

Figure 45. SRAM4G Write Timings



Partial Operations

When either port A or port B is strobed with a falling edge of its CCLK, and both its READ and WRITE control lines are active, then a read followed by a write is performed, where the internal timing of the SRAM4G sequences the write after the read. The minimum cycle time will be determined by the time required to complete both operations. But, if the READ control is inactive while the WRITE is active, the write will be performed immediately after the CCLK edge, and a shorter minimum cycle time will be required for that port. Conversely, if the WRITE control is inactive while the READ is active, the minimum cycle time requirement will be reduced to that of a read cycle alone.

This feature may be useful where only read operations or only write operations are performed on one port, that port could then be operated at a faster cycle time. The faster cycle time cannot be used if there will be some cycles where both the read and write are to be performed in one cycle.

If only one operation is performed, only the minimum cycle time requirement changes. The read access time and all input setup and hold times remain the same.

Address Collisions

Special cases arise when any two or more port address inputs are equal and read and write operations are performed. If both ports are performing a read, there is no concern, as the current address contents will appear on both data output ports. If one port is performing a write and the other attempts to perform a read or a write to the same address, unpredictable results can occur. If the second port is performing a read, the timing relationship between the two CCLKn edges will determine whether the previous data, new data, or unknown data will appear on that output port. However, the correct input data will be stored in the written memory location. If the second port is performing a write, the timing relationship between the two CCLKn edges will determine whether the first port's input data, the second port's input data, or unknown data will be written to the address. Table 84 summarizes which equal address conditions will cause problems, and which will not.

Table 84. SRAM4G Address Collision Conditions

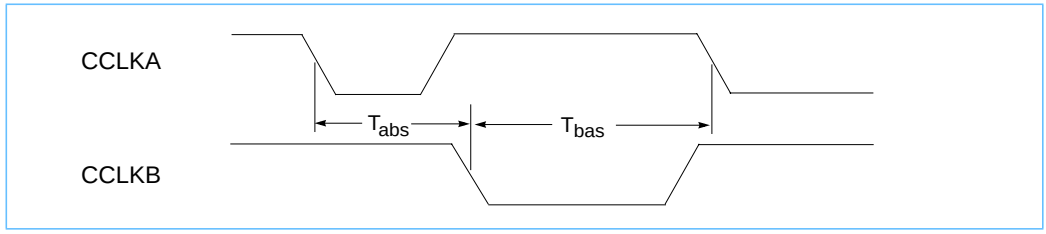
Addresses	Result
Read address port A = Read address port B	Both ports will read valid data.
Read address port A = Write address port A	The valid present contents of the address will be read from port A, then valid new data will be written into the address.
Read address port B = Write address port B	The valid present contents of the address will be read from port B, then valid new data will be written into the address.
Read address port A = Write address port B	**Invalid** data will be read from port A. Valid new data will be written from port B to the address.
Read address port B = Write address port A	**Invalid** data will be read from port B. Valid new data will be written from port A to the address.
Write address port A = Write address port B	**Invalid** data will be written to the address.

To avoid conflicts where unknown data can be written to a memory location or be read to the outputs, non-overlap constraints are defined for the CCLKA and CCLKB clocks as shown in Figure 46. There are two modes defined in the delay rules for this SRAM:

Clock_Synch	The default timing mode, it contains the T_{abs} and T_{bas} non-overlap checks.
Clock_Asynch	An optional mode which does not contain the T_{abs} and T_{bas} non-overlap checks, and which should only be used if address collision is handled elsewhere in the system, either by ensuring that addresses will never be equal, or by expecting unknown “X” data to result when they are. If these conditions are met, then using the Clock_Asynch mode will eliminate the timing errors that would otherwise result when doing timing analysis with non-synchronized CCLKA and CCLKB.

The T_{abs} and T_{bas} non-overlap checks are coded in the logical simulation models for the SRAM, and will only be completely checked when running delay simulation with back-annotated timings.

Figure 46. SRAM4G Clock Separation Requirements



Delay Definitions

Table 85. "Large" SRAM4G2048X040D08S1M1

Timing Parameter	Abbreviation	Minimum (ns)
CCLKn minimum active time	T_{ca}	1.3
CCLKn minimum restore time	T_{cr}	1.0
nREAD setup time before read	T_{rs}	0.4
nREAD hold time after read	T_{rh}	0.5
nWRITE setup time before write	T_{ws}	0.3
nWRITE hold time after write	T_{wh}	0.5
Data in setup time	T_{ds}	-0.1
Data in hold time	T_{dh}	0.9
Bit write setup time	T_{bs}	-0.2
Bit write hold time	T_{bh}	0.9
Read address setup time	T_{ars}	0.3
Read address hold time	T_{arh}	0.4
Write address setup time	T_{aws}	0.2
Write address hold time	T_{awh}	0.4
CCLKA separation before CCLKB	T_{abs}	4.8
CCLKB separation before CCLKA	T_{bas}	4.8
Read cycle time	T_{rcyl}	4.8
Write cycle time	T_{wcyl}	4.8
Access time	T_{acc}	2.2

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 86. "Small" SRAM4G0128X040D04S1M1

Timing Parameter	Abbreviation	Minimum (ns)
CCLKn minimum active time	T_{ca}	1.3
CCLKn minimum restore time	T_{cr}	1.0
nREAD setup time before read	T_{rs}	0.4
nREAD hold time after read	T_{rh}	0.4
nWRITE setup time before write	T_{ws}	0.3
nWRITE hold time after write	T_{wh}	0.4
Data in setup time	T_{ds}	-0.1
Data in hold time	T_{dh}	0.8
Bit write setup time	T_{bs}	-0.2
Bit write hold time	T_{bh}	0.8
Read address setup time	T_{ars}	0.3
Read address hold time	T_{arh}	0.4
Write address setup time	T_{aws}	0.2
Write address hold time	T_{awh}	0.4
CCLKA separation before CCLKB	T_{abs}	3.4
CCLKB separation before CCLKA	T_{bas}	3.4
Read cycle time	T_{rcyl}	3.4
Write cycle time	T_{wcyl}	3.4
Access time	T_{acc}	1.6

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a SRAM4G for a particular application, use the following equation:

$$P = [((A_{readA} \times RC_{int} + A_{writeA} \times WC_{int}) \times F_{port\ A}) + ((A_{readB} \times RC_{int} + A_{writeB} \times WC_{int}) \times F_{port\ B})] \times V^2_{dd}$$

where:

- P = Power in microwatts
- RC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a read access on every cycle. RC_{int} has the same value for both ports. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance of that size SRAM in pF, derived assuming a write access on every cycle. WC_{int} has the same value for both ports.
- A_{readn} = Read activity factor for port n, which is the fraction of the total CCLKn clock cycles that a read access is performed on port n (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- A_{writen} = Write activity factor for port n, which is the fraction of the total CCLKn clock cycles that a write access is performed on port n (a value between 0 and 1). In typical applications, the write activity is often less than the read activity, as the contents of an SRAM are read more often than they are replaced. For this four-port SRAM, the read or write activity factors must be less than or equal to 1 for each port, but the sum of all four activity factors can be greater than 1, but must be less than or equal to 4.
- $F_{port\ n}$ = Clock frequency applied to the port n CCLKn, in MHz.
- V_{dd} = Power supply voltage of the chip in volts.

Array Area and Footprint

Figure 47 shows the general shape of the SRAM, and the relative locations of the pins within it. The dimensions for a particular configuration can be obtained from the sizing routines available on the World Wide Web. Access to the Web page can be obtained from an IBM ASICs representative.

Figure 47. SRAM4G Footprint

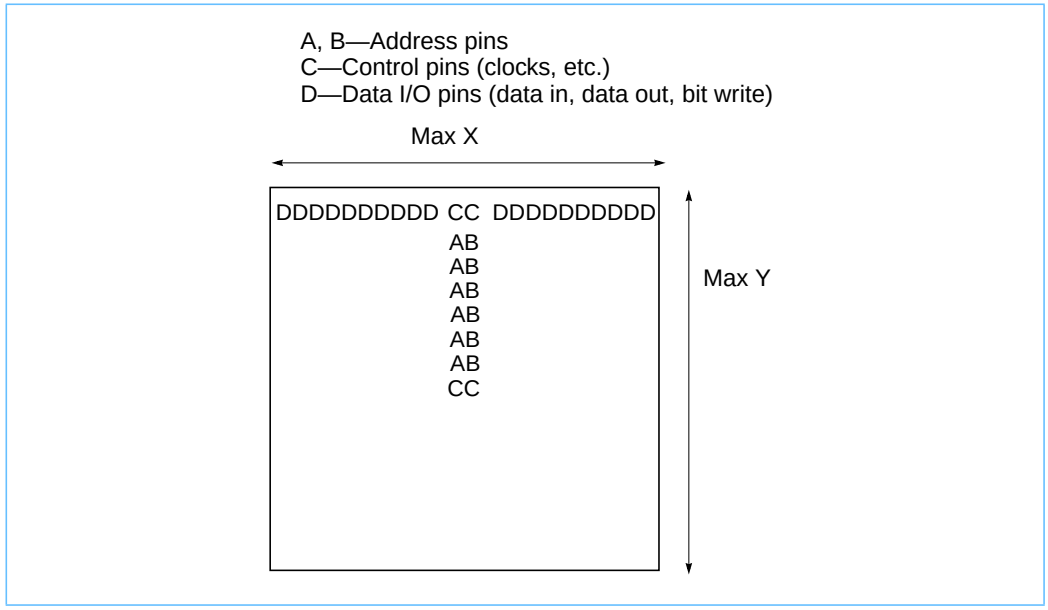


Table 87. SRAM4G Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Sub	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Write Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
256 x 16	4	1	1.8	3.8	36	31	47874	846	58
256 x 32	4	1	1.8	3.8	54	43	72002	1262	58
256 x 40	4	1	1.9	3.9	63	50	84066	1470	58
512 x 16	4	1	1.8	3.8	38	35	69076	826	85
512 x 32	4	1	1.8	3.8	57	49	104436	1242	85
512 x 40	4	1	1.9	3.9	66	56	122116	1450	85
1024 x 16	8	1	1.8	3.8	44	41	96660	1242	81
1024 x 32	8	1	1.9	3.9	68	62	159892	2074	81
1024 x 40	4	1	1.9	3.9	73	69	198966	1450	138
2048 x 16	8	1	1.8	3.8	51	50	162486	1242	135
2048 x 32	8	1	1.9	3.9	77	74	269814	2074	135
2048 x 40	8	1	1.9	3.9	91	86	323478	2490	135

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read or write operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the SRAM and can be calculated using the following equation:

Total scan latches = 23 + (2 x NBIT) (the data word width)

Multiple Array BIST Testing

MABIST Controller Interface

Every instance of an SRAM4G array on a chip must be connected to a BIST4G controller. Up to 16 SRAM4G arrays can be connected to a single BIST4G controller.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

BIST4G—BIST Controller for SRAM4G

Features

- Complete test of all array functions
- Up to 16 arrays tested in parallel from one controller
- System LBIST compatible

The key features of the macro are summarized in Table 88.

Table 88. BIST Controller Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Macro dimensions	513 x 43 chip unit cells
Macro area	22059 chip unit cells
DC test methodology	Multiple array BIST
AC test methodology	Access time
Global porosity on M1	0%
Global porosity on M2	50%
Global porosity on M3	75%

BIST Description

The BIST controller performs all of the necessary DC tests for the arrays during product test by applying addresses, data inputs, bit write controls, and read/write controls to the array. The BIST control signals are multiplexed with the functional inputs for the address, data, and control signals with minimal impact on the SRAM's access, setup, and hold times.

Usage Requirements

Whenever compilable four-port SRAMs are used, the BIST4G controller must be used to generate the BIST test patterns required to verify the SRAMs during product test. BIST4G can be used to control from one to sixteen SRAM4Gs of any configuration.

Symbol Naming Conventions

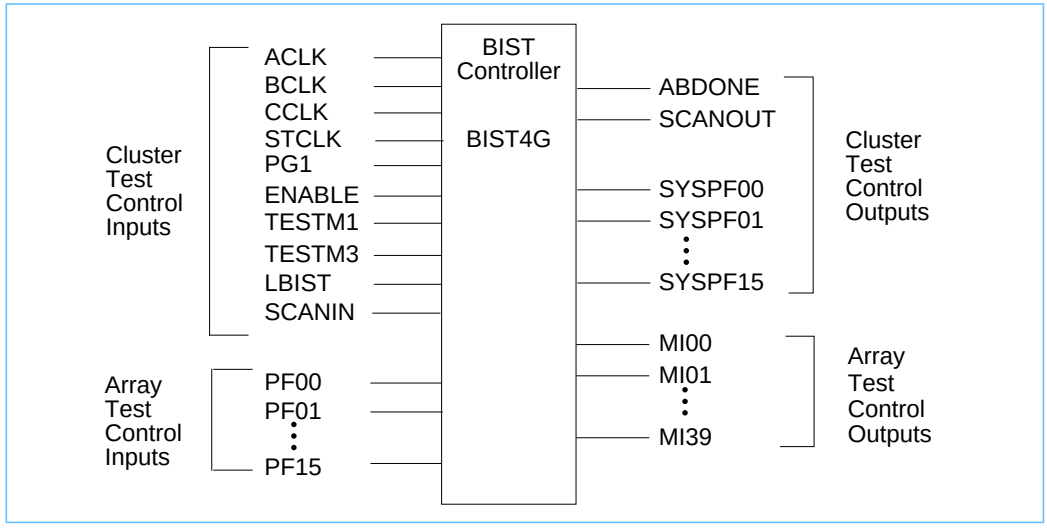
The BIST4G controller does not have a dependence on the SRAM to which it is connected. Therefore, there is a single instance named BIST4G.

Logical Description

Logical Symbol

A symbolic representation of the BIST4G controller is shown in Figure 48.

Figure 48. BIST4G Controller Logic Symbol



Pin Definitions

Table 89 summarizes the function and use of the macro pins shown in Figure 48. Information describing the use of these pins in various test modes can be obtained from an IBM ASICs representative.

Table 89. Pin Definitions

Pin	Description
ACLK	The A clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD A clocks on the chip. The A clock is active high during scan operations and must be held low during array mode operation.
BCLK	The B clock pin is used only during test operations and not during array mode operation of the SRAM. This pin must come from a primary input but can be common with other LSSD B clocks on the chip. The B clock is active high during scan and BIST operations.
CCLK	The C clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is active high during BIST operations and must come from a primary input but can be common with other LSSD C clocks on the chip. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
STCLK	The system test oscillator clock pin is used only during test operations and not during array mode operation of the SRAM. This pin is preferred to be held inactive during array functional mode operation to reduce power consumption in the BIST logic.
PG1	The C clock gate pin is used to gate the CCLK signal. This pin is usually held high, unless it is used during LBIST operations.
ENABLE	The self-test clock enable pin is used to gate the STCLK signal. This pin is usually held high, unless it is used during LBIST operations.
TESTM1	The TESTM1 pin is used together with the TESTM3 pin to set the test state of the BIST controller and the attached arrays. TESTM1 is held low for functional operation of the array.
TESTM3	The TESTM3 pin is used together with the TESTM1 pin to set the test state of the BIST controller and the attached arrays. TESTM3 is held low for functional operation of the array and must be routed from a chip primary input.
LBIST	The LBIST pin must be held high during system LBIST testing to block the B clock to the SRAMs. It must be held low during logic flush and scan operations.

Table 89. Pin Definitions (Continued)

Pin	Description
PF00–PF15	The PF pins are array test inputs which receive the pass/fail state of the arrays on each BIST test cycle. One PF pin is connected to each array being tested. Unused PF pins must be tied to ground.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the BIST controller. The scan-in pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
ABDONE	The ABIST done pin goes high when the BIST controller has completed issuing test patterns to the arrays within its cluster. This pin does not have to be connected.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the BIST controller. The scan-out pin must be placed in a scan path to conform to LSSD test requirements. The scan path can include other elements on the chip.
SYSPF00–SYSPF15	The SYSPF pins are cluster test outputs which allow the BIST pass/fail bits to be observed by on-chip system test logic without requiring a scan operation. These pins are not required to be connected.
MI00–MI39	The MI array test pins are only routed to the arrays under the control of the BIST macro and control the SRAMs during BIST testing. The MI pins must not be wired to any other circuits within the ASIC chip.

Operational Modes

For complete documentation on integrating the BIST4G controller into a chip test environment, contact your IBM ASICs representative.

Macro Footprint

The BIST4G controller is rectangular, 513 unit cells wide by 43 cells high, resulting in a total area of 22059 unit cells.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is fixed at:

BIST4G scan latches = 299

MABIST Test Mode Clock Cycle Calculations

The number of clock cycles required to complete the BIST test is fixed at:

BIST4G clock cycles = 439,595

ROMEH and ROMLH—Compilable High Performance ROM

Features

- Options for early personalization (EH) with diffusion mask or late personalization (LH) with contact mask
- Configurable 256–32K address space and 4–64 data bits
- Latched input/output
- Built-in self-test (RBIST)
- Single clock-edge operation with self restore
- Zero standby current

The key features of the macro are summarized in Table 90.

Table 90. ROM Features

Feature	Capability
Supported V_{dd} range	1.40V–1.95V
Array architecture	M1 bitlines
Maximum macro size	1M bits
Words	256 to 32K words
Data width	4 to 64 bits
Decode option	32:1 or 16:1
DC test methodology	Full RBIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	100%

Keyword Definitions and Limits

The limits and conditions on the NWORD, NBIT, and DECODE options are shown in

Table 91 on page 218.

Table 91. ROMEH/ROMLH Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	256–32768	The total number of words in the array. Non-power-of-two NWORD counts are supported, but must meet the word depth granularity requirements given in Table 92, “ROMEH/ROMLH Valid Sizes”.
NBIT	4–64	The number of bits per word in the array.
DECODE	16 or 32	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array increases and the width (X) of the array decreases.

The resultant ranges of valid array sizes are shown in Table 92.

Table 92. ROMEH/ROMLH Valid Sizes

Decode	Word Depth		Word Depth Granularity	Data Width	
	Min	Max		Min	Max
16	256	2048	256	8	64
	2560	4096	512	8	64
	5120	8192	1024	8	64
	10240	16384	2048	8	64
32	512	4096	512	4	32
	5120	8192	1024	4	32
	10240	16384	2048	4	32
	20480	32768	4096	4	32

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two can be used, but are confined to increments dictated by the physical constraints of the array. The minimum increment that the array can grow by is given by the “word depth granularity” values in Table 92.

If the array is clocked with an address larger than NWORD applied at the address input port, the data from the last valid address will remain latched in the data output registers.

Global M2 Wiring Porosity

ROMEH/ROMLH has no global M2 porosity over the array.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

ROMEHwwwwwXbbbDddM1Cccc

or

ROMLHwwwwwXbbbDddM1Cccc

where:

ROMEH = Early personalized ROM name
ROMLH = Late personalized ROM name
w = total number of words: 5 digits
b = data width in bits: 3 digits
d = decode option: 2 digits
M1 = array clocked timing mode only
c = personalization: 3 digits—
differentiates between up to 1000 different personalizations for each size ROM. SA-27E personalizations start with ‘5’ as the first digit.

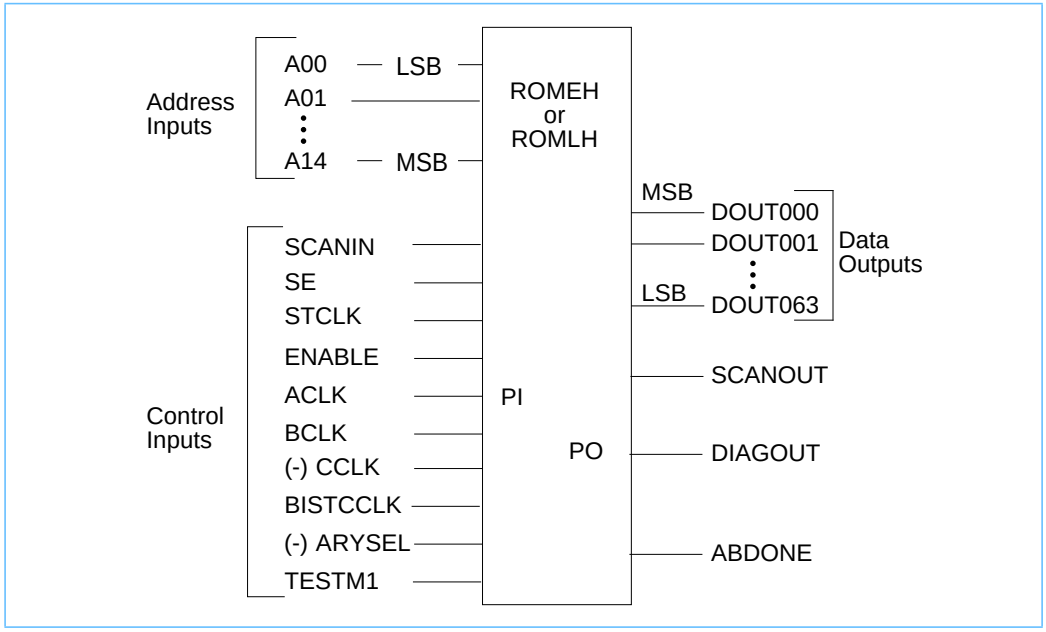
A representative example would be:

ROMLH02048X016D16M1C507	A 2048-word x 16-bit, decode of 16, late-personalized ROM, containing the 7th personalization implemented for this size array, with array-clocked functional mode timing.

Logical Description

A symbolic representation of ROMEH/ROMLH is shown in Figure 49.

Figure 49. ROMEH or ROMLH Logic Symbol



Pin Definitions

Table 93 summarizes the function and proper usage of the macro pins shown in Figure 49. The control and input pins must be stable before the CCLK initiates an access of the array. Pin timing relationships are described later.

Table 93. Pin Definitions

Pin	Description
A00–A14	The address input pins define the address from which output data will be read. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation: words = 2^N. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
SCANIN	The SCANIN pin is a standard LSSD pin for the scannable latches internal to the ROM. The ROM can be placed in a scan path with other elements on a chip. The SCANIN pin must be used to conform to LSSD test requirements.
SE	The SE pin must be held high for both normal LSSD scan operation and BIST scan initialization. The SE pin must be held low during BIST operation. For normal functional operation, the SE pin can be held high or low.
ENABLE[1]	The ENABLE input activates the STCLK (OSC) input to generate the internal test clocks. This allows the use of a single clock for testing in the system environment, instead of the two external BCLK and BISTCCLK as is done during manufacturing ABIST testing. **Note:** BISTCCLK and BCLK must be held high. See the datasheet for standard cell CLKSPL.
STCLK[1]	This pin is used to generate the internal test clocks in the system environment from a single clock input where LSSD clocks are not available.
ACLK	The ACLK (A clock) pin is used only during test operations, and not during array mode operation of the ROM. This pin must come from a primary input, but can be common with other LSSD A clocks on the chip. The ACLK is active high during scan operations, and must be held low during array mode operation.
BCLK	The BCLK (B clock) pin is used only during test operations, and not during array mode operation of the ROM. This pin must come from a primary input, but can be common with other LSSD B clocks on the chip. The BCLK is active high during scan operations and manufacturing ABIST testing, and must be held constant (high or low) during array mode operation.
CCLK	The CCLK pin initiates a read access of the ROM on its falling edge during normal operation. This pin must come from a primary input. This is not used during BIST.
BISTCCLK	BISTCCLK is used to generate the internal clocks used during manufacturing ABIST testing.

1. During manufacturing ABIST mode, ENABLE is held high and STCLK is held low.

Table 93. Pin Definitions (Continued)

Pin	Description
ARYSEL	The ARYSEL (array select) pin is active low. If held high, it will prevent read accesses of the array from being initiated. The ARYSEL pin can be used to select an array if there are multiple arrays on a chip driven by common clock and control lines. If not used, the ARYSEL pin must be tied low. It is disabled during test mode by TESTM1.
TESTM1	The TESTM1 pin is used to set the test state of the ROM. TESTM1 is held low for functional operation of the macro.
DOUT000–DOUT063	The data output pins are noninverting. Pins are used starting at DOUT000 and counting upwards. **The DOUT000 bit is always the most-significant bit.** If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read.
SCANOUT	The SCANOUT pin is a standard LSSD pin from the scannable latches internal to the ROM. The ROM can be placed in a scan path with other elements on a chip. The SCANOUT pin must be used to conform to LSSD test requirements.
DIAGOUT	The DIAGOUT (diagnostic output) pin is taken from the L2 stage of the least-significant data out latch, and must be routed to a primary output, but can be multiplexed with other outputs. This pin is used only for diagnostics, to observe the output data before it enters the compression circuitry.
ABDONE	The ABDONE (ABIST done) pin goes high when the last ABIST cycle has completed. This pin is available for system use, but is not required to be connected for test.

1. During manufacturing ABIST mode, ENABLE is held high and STCLK is held low.

Array Mode Functional Operation

Definition

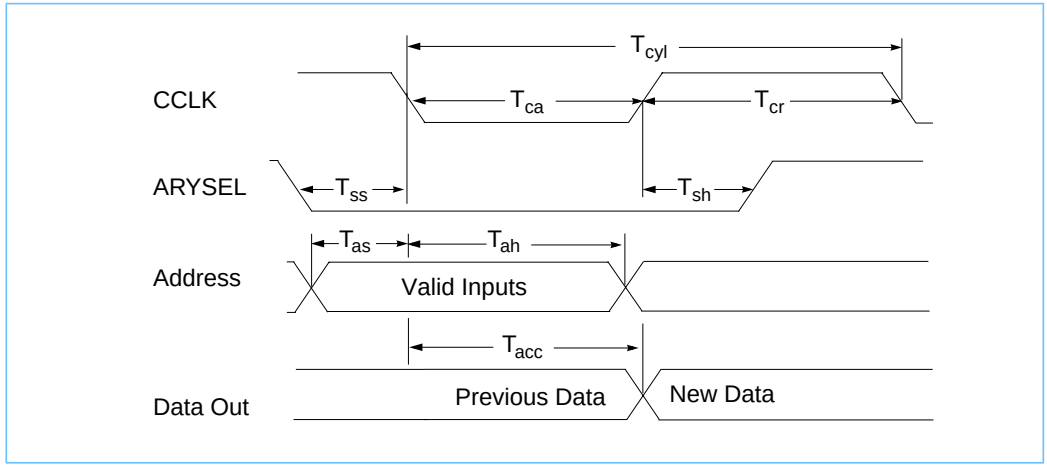
Array mode operation is the normal functional operation of the ROM, when the TESTM1 input is held low. The ACLK and BCLK pins must be controlled according to standard LSSD requirements.

Array Clocking Modes

Array Clocked Read

- CCLK falling initiates the access cycle.
- Data is read from the address in the array.
- Data appears at the data output pins after the access time has elapsed.
- Data output is valid until the next read cycle.

Figure 50. Array Clocked Read Timing



Delay Definitions

Table 94 and Table 95 on page 224 show setup and hold times for representative “small” and “large” ROMLH arrays.

Table 94. "Small" ROMLH00256X016D16

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.0
CCLK minimum restore time	T_{cr}	1.0
ARYSEL setup time	T_{ss}	0.4
ARYSEL hold time	T_{sh}	0.4
Address setup time	T_{as}	-0.1
Address hold time	T_{ah}	0.5
Access time	T_{acc}	2.7
Cycle time	T_{cyl}	2.9

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 95. "Large" ROMLH32768X032D32

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	1.0
CCLK minimum restore time	T_{cr}	1.0
ARYSEL setup time	T_{ss}	0.4
ARYSEL hold time	T_{sh}	0.4
Address setup time	T_{as}	-0.1
Address hold time	T_{ah}	0.5
Access time	T_{acc}	4.7
Cycle time	T_{cyl}	6.0

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools available on this Web page allow the user to enter the desired word and bit counts for an array to obtain the physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a ROM for a particular application, use the following equation.

$$P = A_{read} \times C_{int} \times V^2_{dd} \times F_{ROM}$$

where:

- P = Power in microwatts
- C_{int} = Internal capacitance of that size ROM in pF, derived assuming a read access on every cycle. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read access is performed (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{ROM} = Clock frequency applied to the ROM, in MHz.

Array Area and Footprint

Figure 51 shows the general shape of the ROM, and the relative locations of the pins within it. The dimensions for a particular configuration can be obtained from the sizing routines available on the World Wide Web.

Figure 51. ROMLH or ROMEH Footprint

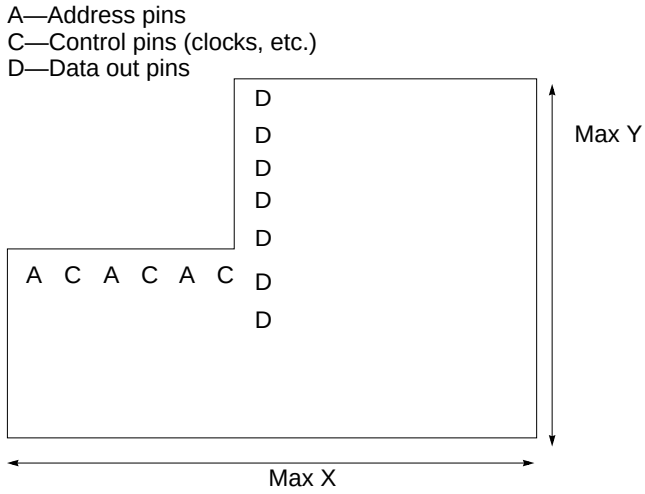


Table 96. ROMEH Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
1024 x 16	16	2.7	2.9	TBD	23033	501	62
1024 x 32	16	2.8	3.1	TBD	32471	501	101
1024 x 64	16	3.0	3.3	TBD	51589	501	180
4096 x 16	16	3.0	3.3	TBD	39587	768	62
4096 x 32	16	3.0	3.4	TBD	59438	768	101
4096 x 64	16	3.2	3.7	TBD	99649	768	180
16384 x 16	32	3.4	3.9	TBD	95495	1125	101
16384 x 32	32	3.6	4.2	TBD	163909	1125	180
16384 x 64	16	4.3	5.3	TBD	292249	1838	180
32768 x 16	32	4.1	5.0	TBD	167508	1838	101
32768 x 32	32	4.3	5.3	TBD	292249	1838	180

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Table 97. ROMLH Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
1024 x 16	16	2.7	3.0	TBD	26387	533	67
1024 x 32	16	2.9	3.1	TBD	38717	533	112
1024 x 64	16	3.1	3.4	TBD	63103	533	201
4096 x 16	16	3.1	3.5	TBD	50708	896	67
4096 x 32	16	3.2	3.6	TBD	79373	896	112
4096 x 64	16	3.4	3.9	TBD	136066	896	201
16384 x 16	32	3.6	4.3	TBD	133693	1381	112
16384 x 32	32	3.8	4.6	TBD	233551	1381	201
16384 x 64	16	4.7	6.0	TBD	428320	2350	201
32768 x 16	32	4.5	5.6	TBD	242221	2350	112
32768 x 32	32	4.7	6.0	TBD	428320	2350	201

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the ROM, and can be calculated using the following equation:

Total latches = 86 + NBIT where NBIT = number of data bits per word

Personalization Methodology

Personality File Format

The ROM personality file is a text (ASCII) file which must contain only the following:

- White space (spaces, new lines, tabs, and form-feeds).
- Comment type one: opening delimiter is '`/*`', closing delimiter is '`*/`'.
- Comment type two: opening delimiter is '`//`', closing delimiter is a new-line or form-feed character. **Everything to the right of the '`//`' is a comment.**
- Personality data: one field per line of binary numbers (consisting of zeros and ones), with no spaces or blanks between the numbers for the width of the word. Any unused address locations should be filled with zeros.

Binary numbers are separated by white space and/or comments. The first binary number in the file is assigned to address location 0 of the ROM, the second binary number is assigned to address location 1, etc. The left-most bit of each binary number is the most-significant bit, which corresponds to pin DOUT000 on the output; the right-most bit of each binary number is the least significant bit.

An example personality file for a 4-word by 8-bit ROM with personality would be:

```
/* Example personality for 4-word by 8-bit ROM. */
11110000 // This word is assigned to address 0.
11011011 // This word is assigned to address 1.
10100101 /* This word is assigned to address 2.*/
11100111 /* This word is assigned to address 3.*/

/* This personality data created 22 MAY 1998 15:47 PM EDT. */
```

ROMEP and ROMLP—Compilable Low-Power ROM

Features

- Options for early personalization (EP) with diffusion mask or late personalization (LP) with contact mask
- Configurable 256–32K address space and 4–64 data bits
- Latched input/output
- Built-in self-test (RBIST)
- Single clock edge operation with self restore
- Zero standby current

The key features of the macro are summarized in Table 98.

Table 98. ROM Features

Feature	Capability
Supported V_{dd} range	1.20V–1.95V
Array architecture	M1 bitlines
Maximum macro size	1M bits
Words	256 to 32K words
Data width	4 to 64 bits
Decode option	32:1 or 16:1
DC test methodology	Full RBIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	100%

Keyword Definitions and Limits

The limits and conditions on the NWORD, NBIT, and DECODE options are given in Table 99.

Table 99. ROMEP/ROMLP Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	256–32768	The total number of words in the array.
NBIT	4–64	The number of bits per word in the array.
DECODE	16 or 32	The number of cell columns that are decoded into one data output bit. As the DECODE option is changed for a given NWORD and NBIT configuration, the aspect ratio of the array changes: as DECODE increases, the height (Y) of the array increases and the width (X) of the array decreases.

The resultant ranges of valid array sizes are shown in Table 100.

Table 100. ROMEP/ROMLP Valid Sizes

Decode	Word Depth		Word Depth Granularity	Data Width	
	Min	Max		Min	Max
16	256	16384	by powers of 2	8	64
32	512	32768	by powers of 2	4	32

Non-Power-of-Two NWORD Counts

NWORD values which are not powers of two cannot be used.

Global M2 Wiring Porosity

ROMEP/ROMLP has no global M2 porosity over the array.

Symbol Naming Conventions

The naming strategy for the compilable memory arrays is defined such that unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

ROMEPwwwwwXbbbDddM1Cccc

or

ROMLPwwwwwXbbbDddM1Cccc

where:

ROMEP = Early personalized ROM name
ROMLP = Late personalized ROM name
w = total number of words: 5 digits
b = data width in bits: 3 digits
d = decode option: 2 digits
M1 = array clocked timing mode only
c = personalization: 3 digits—
differentiates between up to 1000 different personalizations for each size ROM. SA-27E personalizations start with ‘5’ as the first digit.

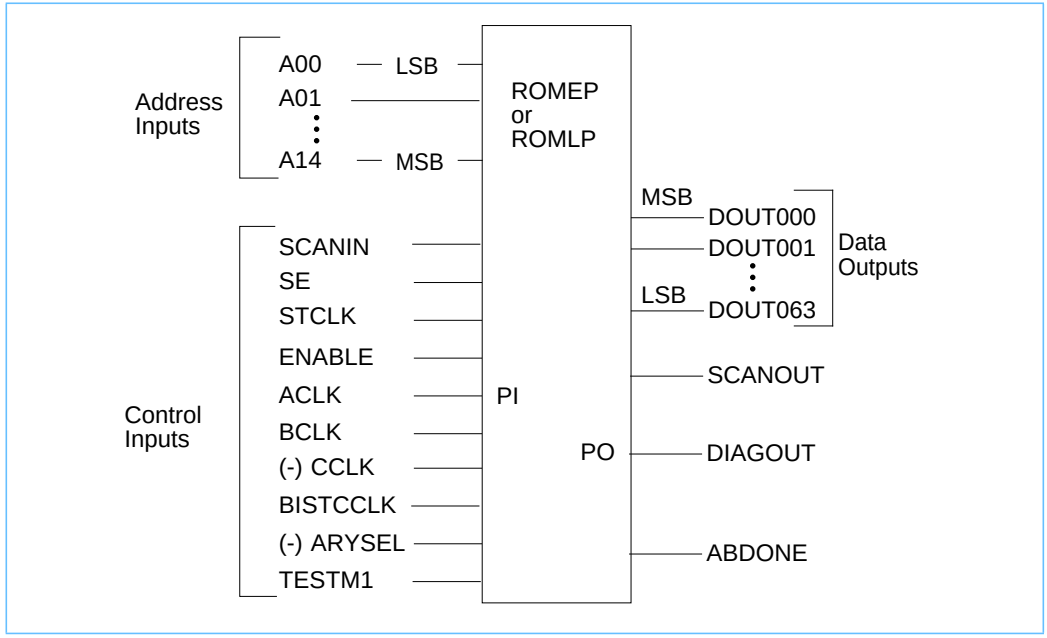
A representative example would be:

ROMLP02048X016D16M1C507	A 2048-word x 16-bit, decode of 16, late-personalized ROM, containing the 7th personalization implemented for this size array, with array clocked functional mode timing.

Logical Description

A symbolic representation of ROMEP/ROMLP is shown in Figure 52.

Figure 52. ROMEP or ROMLP Logic Symbol



Pin Definitions

Table 101 on page 234 summarizes the function and proper usage of the macro pins shown in Figure 52. The control and input pins must be stable before the CCLK initiates an access of the array. Pin timing relationships are described later.

Table 101. Pin Definitions

Pin	Description
A00–A14	The address input pins define the address from which output data will be read. The number used is dependent on the word count of the array selected. Pins are used starting at the A00 least significant bit and counting upwards. The number of address pins required (N) is determined from the equation: words = 2^N. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
SCANIN	The SCANIN pin is a standard LSSD pin for the scannable latches internal to the ROM. The ROM can be placed in a scan path with other elements on a chip. The SCANIN pin must be used to conform to LSSD test requirements.
SE	The SE pin must be held high for both normal LSSD scan operation and BIST scan initialization. The SE pin must be held low during BIST operation. For normal functional operation, the SE pin can be held high or low.
ENABLE[1]	The ENABLE input activates the STCLK (OSC) input to generate the internal test clocks. This allows the use of a single clock for testing in the system environment, instead of the two external BCLK and BISTCCLK as is done during manufacturing ABIST testing. **Note:** BISTCCLK and BCLK must be held high. See the datasheet for standard cell CLKSPL.
STCLK[1]	This pin is used to generate the internal test clocks in the system environment from a single clock input where LSSD clocks are not available.
ACLK	The ACLK (A clock) pin is used only during test operations, and not during array mode operation of the ROM. This pin must come from a primary input, but can be common with other LSSD A clocks on the chip. The ACLK is active high during scan operations, and must be held low during array mode operation.
BCLK	The BCLK (B clock) pin is used only during test operations, and not during array mode operation of the ROM. This pin must come from a primary input, but can be common with other LSSD B clocks on the chip. The BCLK is active high during scan operations and manufacturing ABIST testing, and must be held constant (high or low) during array mode operation.
CCLK	The CCLK pin initiates a read access of the ROM on its falling edge during normal operation. This pin must come from a primary input. This is not used during BIST.
BISTCCLK	BISTCCLK is used to generate the internal clocks used during manufacturing ABIST testing.

1. During manufacturing ABIST mode, ENABLE is held high and STCLK is held low.

Table 101. Pin Definitions (Continued)

Pin	Description
ARYSEL	The ARYSEL (array select) pin is active low. If held high, it will prevent read accesses of the array from being initiated. The ARYSEL pin can be used to select an array if there are multiple arrays on a chip driven by common clock and control lines. If not used, the ARYSEL pin must be tied low. It is disabled during test mode by TESTM1.
TESTM1	The TESTM1 pin is used to set the test state of the ROM. TESTM1 is held low for functional operation of the macro.
DOUT000–DOUT063	The data output pins are noninverting. Pins are used starting at DOUT000 and counting upwards. **The DOUT000 bit is always the most-significant bit.** If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read.
SCANOUT	The SCANOUT pin is a standard LSSD pin from the scannable latches internal to the ROM. The ROM can be placed in a scan path with other elements on a chip. The SCANOUT pin must be used to conform to LSSD test requirements.
DIAGOUT	The DIAGOUT (diagnostic output) pin is taken from the L2 stage of the least-significant data out latch, and must be routed to a primary output, but can be multiplexed with other outputs. This pin is used only for diagnostics, to observe the output data before it enters the compression circuitry.
ABDONE	The ABDONE (ABIST done) pin goes high when the last ABIST cycle has completed. This pin is available for system use, but is not required to be connected for test.

1. During manufacturing ABIST mode, ENABLE is held high and STCLK is held low.

Array Mode Functional Operation

Definition

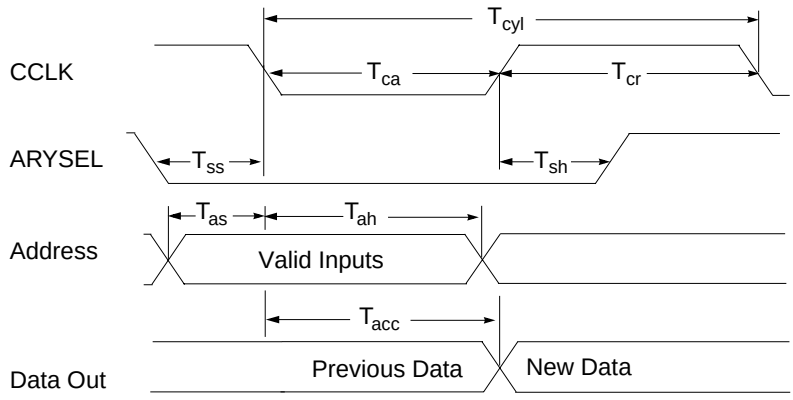
Array mode operation is the normal functional operation of the ROM, when the TESTM1 input is held low. The ACLK and BCLK pins must be controlled according to standard LSSD requirements.

Array Clocking Modes

Array Clocked Read

- CCLK falling initiates the access cycle.
- Data is read from the address in the array.
- Data appears at the data output pins after the access time has elapsed.
- Data output is valid until the next read cycle.

Figure 53. Array Clocked Read Timing



Delay Tables

Table 102 and Table 103 on page 237 show setup and hold times for representative “small” and “large” ROMLP arrays. An equivalent configuration ROMEP array would have similar timings.

Table 102. "Small" ROMLP00256X016D16

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	2.8
CCLK minimum restore time	T_{cr}	2.8
ARYSEL setup time	T_{ss}	0.34
ARYSEL hold time	T_{sh}	0.34
Address setup time	T_{as}	0.4
Address hold time	T_{ah}	0.4
Access time	T_{acc}	5.6
Cycle time	T_{cyl}	6.8

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 103. "Large" ROMLP32768X032D32

Timing Parameter	Abbreviation	Minimum (ns)
CCLK minimum active time	T_{ca}	3.9
CCLK minimum restore time	T_{cr}	3.9
ARYSEL setup time	T_{ss}	0.34
ARYSEL hold time	T_{sh}	0.34
Address setup time	T_{as}	0.4
Address hold time	T_{ah}	0.4
Access time	T_{acc}	11.3
Cycle time	T_{cyl}	14.3

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools available on this Web page allow the user to enter the desired word and bit counts for an array to obtain the physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a ROM for a particular application, use the following equation.

$$P = A_{read} \times C_{int} \times V^2_{dd} \times F_{ROM}$$

where:

- P = Power in microwatts
- C_{int} = Internal capacitance of that size ROM in pF, derived assuming a read access on every cycle. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read access is performed (a value between 0 and 1). In typical applications, the read activity factor can approach 1.0.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{ROM} = Clock frequency applied to the ROM, in MHz.

Array Area and Footprint

Figure 54 shows the general shape of the ROM, and the relative locations of the pins within it. The dimensions for a particular configuration can be obtained from the sizing routines available on the World Wide Web.

Figure 54. ROMLP or ROMEP Footprint

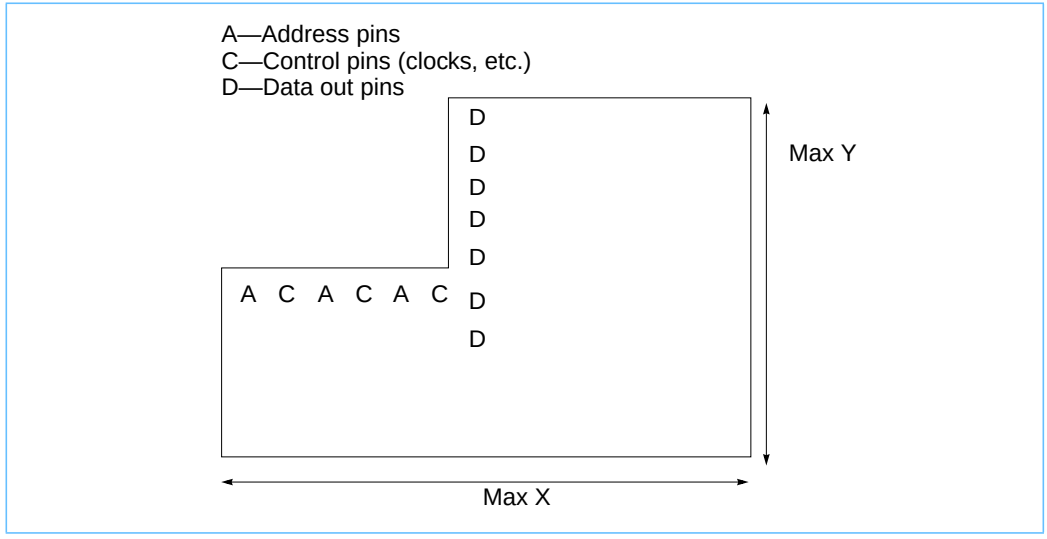


Table 104. ROMEP Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
1024 x 16	16	5.8	6.9	10	16523	443	46
1024 x 32	16	6.2	7.4	11	22289	443	77
1024 x 64	16	7.1	8.5	14	33635	443	138
4096 x 16	16	6.2	7.4	11	28115	695	46
4096 x 32	16	6.7	8.0	13	41693	695	77
4096 x 64	16	7.5	9.0	16	68411	695	138
16384 x 16	32	8.0	9.7	14	66859	1029	77
16384 x 32	32	8.9	11.1	16	113219	1029	138
16384 x 64	16	10.3	12.4	23	207515	1703	138
32768 x 16	32	10.4	12.3	19	118680	1702	77
32768 x 32	32	11.2	13.7	21	206093	1702	138

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Table 105. ROMLP Access Time, Internal Capacitance, and Physical Area Examples

Array Size	Decode	Access Time (ns)	Cycle Time (ns)	Read Internal Cap (pF)	Physical Area (cell units)	Max X Dimensions (cell units)	Max Y Dimensions (cell units)
1024 x 16	16	5.8	6.9	10	17995	475	46
1024 x 32	16	6.2	7.5	11	24753	475	77
1024 x 64	16	7.1	8.6	14	38051	475	138
4096 x 16	16	6.3	7.5	11	34003	823	46
4096 x 32	16	6.7	8.1	13	51549	823	77
4096 x 64	16	7.6	9.2	16	86075	823	138
16384 x 16	32	8.1	9.9	14	86571	1285	77
16384 x 32	32	9.1	11.5	16	148547	1285	138
16384 x 64	16	10.6	12.8	23	278171	2215	138
32768 x 16	32	10.5	12.8	19	158104	2214	77
32768 x 32	32	11.3	14.3	21	276749	2214	138

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (μW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}. Power assumes a read operation on every cycle.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 μm.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the scan chain is dependent on only the data width of the ROM, and can be calculated using the following equation:

Total latches = 86 + NBIT where: NBIT = number of data bits per word

Personalization Methodology

Personality File Format

The ROM personality file is a text (ASCII) file which must contain only the following:

- White space (spaces, new lines, tabs, and form-feeds).
- Comment type one: opening delimiter is '`/*`', closing delimiter is '`*/`'.
- Comment type two: opening delimiter is '`//`', closing delimiter is a new-line or form-feed character. **Everything to the right of the '`//`' is a comment.**
- Personality data: one field per line of binary numbers (consisting of zeros and ones), with no spaces or blanks between the numbers for the width of the word. Any unused address locations should be filled with zeros.

Binary numbers are separated by white space and/or comments. The first binary number in the file is assigned to address location 0 of the ROM, the second binary number is assigned to address location 1, etc. The left-most bit of each binary number is the most-significant bit, which corresponds to pin DOUT000 on the output; the right-most bit of each binary number is the least significant bit.

An example personality file for a 4-word by 8-bit ROM with personality would be:

```
/* Example personality for 4-word by 8-bit ROM. */
11110000 // This word is assigned to address 0.
11011011 // This word is assigned to address 1.
10100101 /* This word is assigned to address 2.*/
11100111 /* This word is assigned to address 3.*/

/* This personality data created 22 MAY 1998 15:47 PM EDT. */
```

CAMB—Binary Content Addressable Memory

Features

- Fully static array
- Two word depth configurations: 64 words and 512 words
- Data bit-width compilable from 8 bits to 64 bits
- Write, read, search, and reset operations; each edge triggered from a single clock
- Valid bit for each entry
- Blanket reset of valid bits
- Bit masking for search and write operations
- Data output latched until next read operation
- Address output latched until next search operation
- Multiple array built-in self-test
- Power reduction during search operations based on customizable hierarchical data compare
- Compiler option to build the CAM with or without an output address priority encoder:
  - With a priority encoder, a search operation produces a hit/miss flag which indicates if at least one matching entry was found, a multiple hit flag which indicates if multiple matches occurred, and the lowest matching address encoded on the output address pins until the next search operation
  - Without a priority encoder, a search operation produces all match-line results latched as outputs until the next search operation

The key features of the macro are summarized in Table 106.

Table 106. CAMB Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Array architecture	M2 bitlines
Maximum macro size for CAM with 512 words	32K (32,768) bits
Maximum macro size for CAM with 64 words	4K (4096) bits
Maximum data width for both CAMs	64 bits
Minimum data width for both CAMs	8 bits
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	0%
Global porosity on M3	42%

Keyword Definitions and Limits

The limits and conditions on the NWORD and NBIT options are shown in Table 107. This array will be a custom macro initially, where different configurations must be requested from the developers. There may be an eventual extension to fully-compilable support if there is sufficient customer interest in numerous configurations.

Table 107. CAMB Keyword Parameter Ranges

Keyword	Allowed Values	Description
NWORD	64 or 512	The total number of words in the array
NBIT	8–64	The number of bits per word in the array, valid sizes are increments of 1

Symbol Naming Conventions

The naming strategy for the CAM will be similar to that defined for the compilable memory arrays, where unique instance names can be created for each possible configuration. The first group of characters in the name defines the generic array type, after which are appended fields to define the various array options. Leading zeros are used in numerical fields to keep all instance names for a given array type the same length. This makes alphabetical listings of array instances appear in order. The names adhere to the following conventions:

CAMBeewwwXbbMmPppPppPppPpp

where:

CAMB = configurable binary CAM name

ee = output type:
- PE with priority encoder on match lines
- ML without priority encoder on match lines

www = total number of words–3 digits

bb = data width in bits–2 digits

m = timing mode–1 digit
- 1 array clocked mode

pp = personalization code for the four power savings bit positions: 2 digits All four bits must be unique and should be listed in ascending order from left to right for each of the four positions.

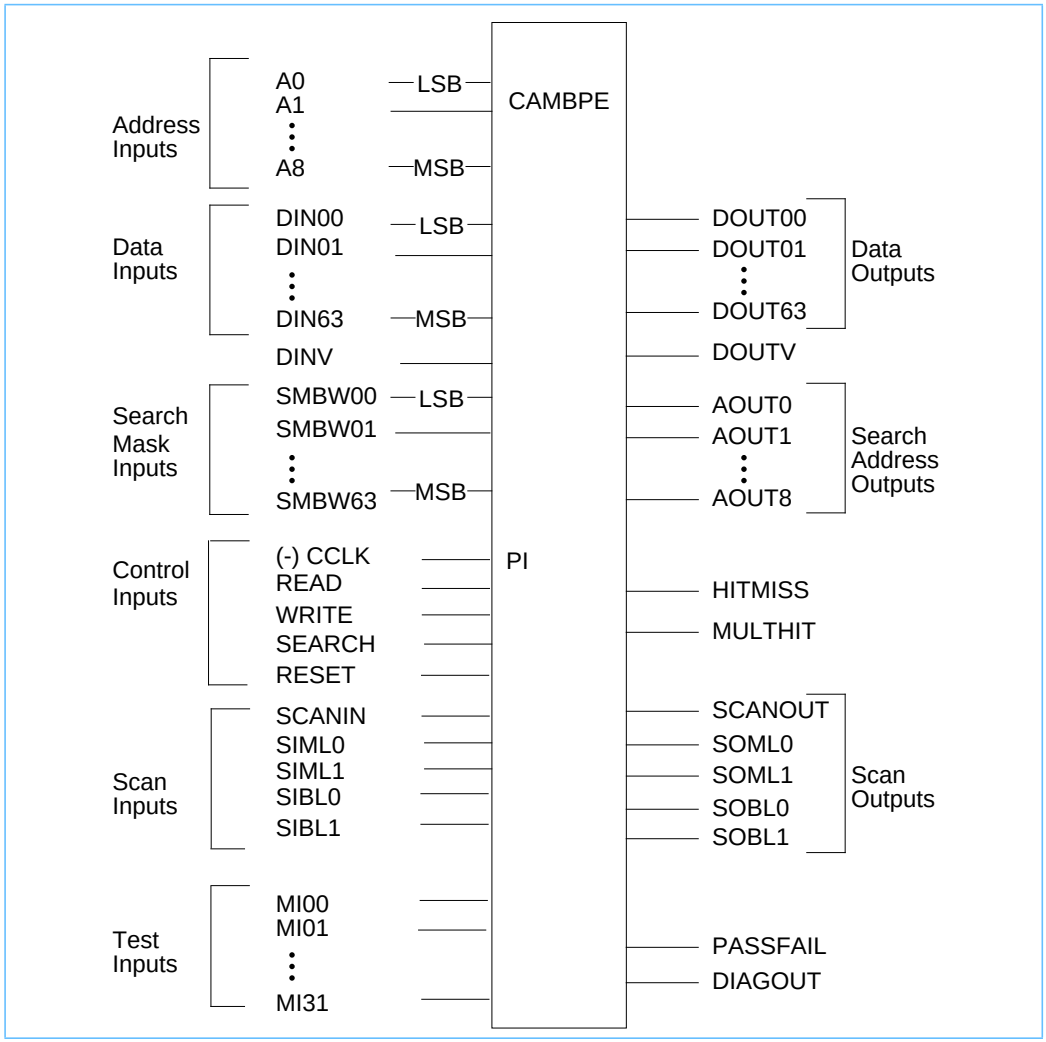
A representative example would be:

CAMBPE064X54M1P08P09P37P38	A 64-word x 54-bit CAM, with a priority encoder; the four power-saving pins located at 08, 09, 37, and 38, and with array clocked mode functional timing

Logical Description

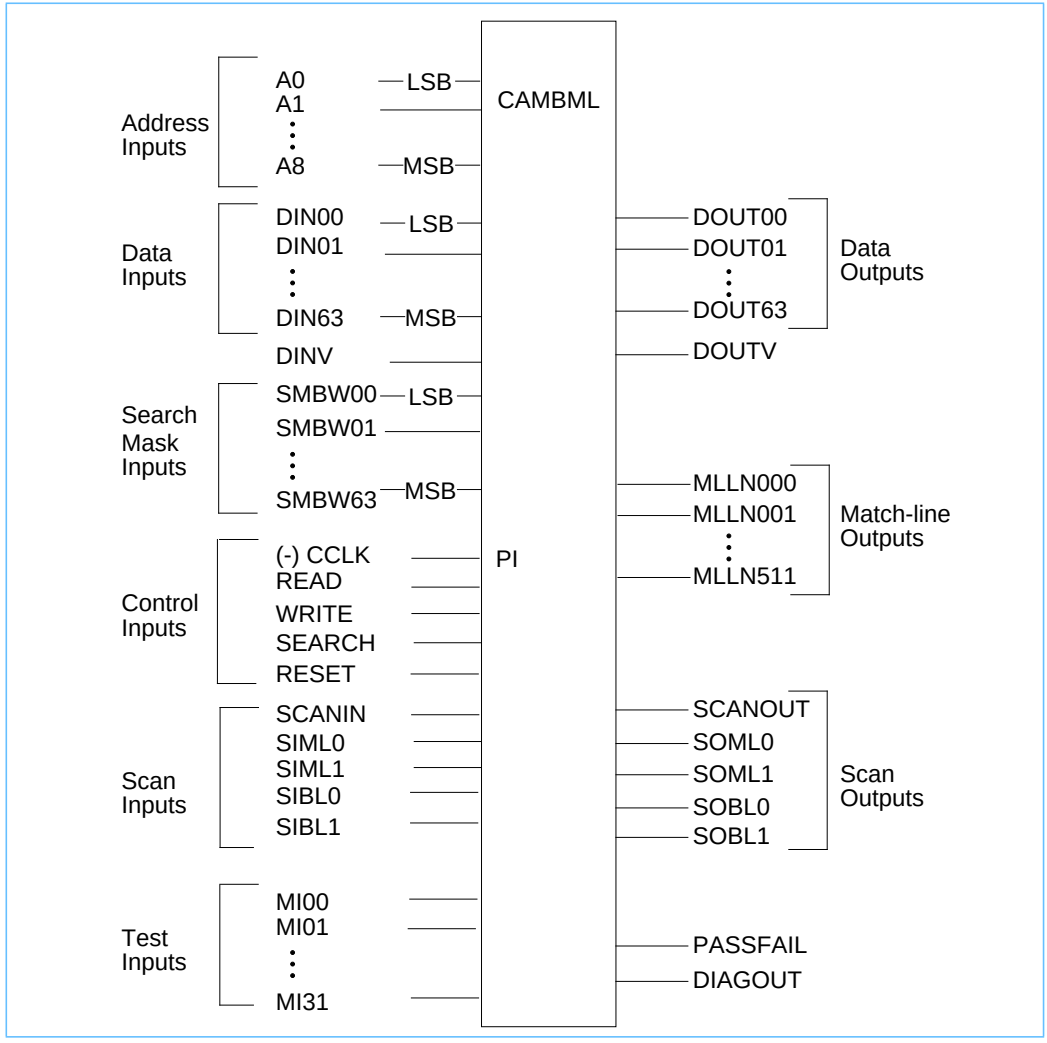
A symbolic representation of the CAM with priority encoder is shown in Figure 55.

Figure 55. CAMB Logic Symbol with Priority Encoder



A symbolic representation of the CAM without priority encoder is shown in Figure 56.

Figure 56. CAMB Logic Symbol without Priority Encoder



Pin Definitions

Table 108 summarizes the function and proper usage of the macro pins shown in Figure 55 on page 246 and Figure 56 on page 247. The control and input pins must be stable before the clocks initiate a read, write, search, or reset access of the array. Pin timing relationships are described later.

Table 108. Pin Definitions

Pin	Description
A0–A8	The address input pins define the address from or to which data will be read or written. The number used is dependent on the word count of the array selected. Pins are used starting at the A0 least significant bit and counting upwards. The 64 word configurations use A0–A5. The 512 word configurations use A0–A8.
DIN00– DIN63	The data input pins are noninverting, and the number used is dependent on the data bit count of the array selected. Pins are used starting at the DIN00 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
DINV	The data input valid pin inputs the valid bit during a write operation. Its operation and timings are the same as for the data-in pins. The valid bit should be set high if the CAM contents at that address are to be valid, or low if they are to be invalid. If the valid bit for an entry is set valid, that entry is included in a search operation. If it is invalid, a match of this entry during a search operation will be ignored, even if the other bits in the entry match the input data. During a search operation, the DINV pin must be held high, except for the special case when searching for the next available entry to write new data. For this case, DINV must be held low and the search mask pins held inactive.
SMBW00–SMBW63	The search mask/bit write input pins are active high, and one pin is required for each data input bit. These pins allow masking of the input data during search operations or write operations. During search operations, if the pin is held high, the corresponding data input bit is used during the search; if the pin is held low, the corresponding data input bit is ignored. During write operations, if the pin is held high, the corresponding data input bit is written into the array; if the pin is held low, the corresponding data input bit is ignored, and the array retains its previous contents for that bit. The search mask pins perform no function during a read of the array. Pins are used starting at the SMBW00 least significant bit and counting upwards. If a data input pin is not used, then the corresponding search mask/bit write pin will not appear in the logical or physical models either. However, a search mask pin is always allocated for every data input pin used. If search masking is not required, then these pins must be tied high.

Table 108. Pin Definitions (Continued)

Pin	Description
CCLK	The C clock pin initiates a read, write, search, or reset access of the CAM on its falling edge during functional mode operations. This pin must come from a primary input but may be common with other LSSD C clocks on the chip.
READ	The read pin causes a read of the CAM entry pointed to by the address input pins to be performed if held high when the C clock goes active. The contents of that entry appear on the data output pins.
WRITE	The write pin causes a write of the CAM entry pointed to by the address input pins to be performed if held high when the C clock goes active. The data on the data input pins is written into the entry. The DINV pin is normally held high during a write operation to set the valid bit for that entry to the valid state.
SEARCH	The search pin causes a search of the array to be performed if held high when the C clock goes active. Data on the data input pins is compared to all entries in the CAM which have their valid bit set to the high “valid” state. If the priority encoder is used, and if only one matching entry is found, the address of that entry will appear at the address output pins, the HITMISS pin will go high, and the MULTHIT pin will remain low. If more than one matching entry is found, the lowest of the matched entry addresses will appear at the address output pins, and both the HIT-MISS and MULTHIT pins will go high. If no match is found, the HITMISS and MULTHIT pins will go low, and the address out pins will all go high. If the priority encoder is not used, then the match results of all of the entries will appear on their respective match line latch output pins.
RESET	The reset pin causes a reset of the valid bits to their low “invalid” state for all of the CAM entries if held high when the C clock goes active. In other words, it is used as a blanket invalidation all of the entries in the CAM.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the CAM. The CAM can be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.
SIML0 and SIML1	SIML0 and SIML1 are the scan-in pins for the match line latches. These strings may be placed in a scan path with other elements on a chip, and must be used to conform to LSSD test requirements. The number of SIML pins required is a function of configuration. The 64-word configurations use SIML0 only. The 512-word configurations use SIML0 and SIML1. If the SIML1 pin is not required, it will not appear in the logical or physical mod-els; therefore, no tie-off procedure is required.
SIBL0 and SIBL1	SIBL0 and SIBL1 are the scan-in pins for the match line BIST compare latches. These strings may be placed in a scan path with other elements on a chip, and follow the same rules as for the SIML0 and SIML1 pins.

Table 108. Pin Definitions (Continued)

Pin	Description
MI00–MI31	The test interface pins must be connected to an accompanying CAMBBIST controller, and control the CAM during BIST testing. The MInn pins must not be connected to anything other than the CAMBBIST controller. The 64-word configurations use MI00–MI28. The 512-word configurations use MI00–MI31.
DOUT00–DOUT63	The data output pins are noninverting, and the number used is the same as the number of data input pins selected. Pins are used starting at the DOUT00 least significant bit and counting upwards. If a pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required. The results of a read of the array are latched in the output, therefore, the results of a read remain on the data output pins until the next read. Write operations do not affect the data output pins.
DOUTV	The data output valid pin outputs the valid bit for the entry being read during a read operation. Its operation and timings are the same as for the data-out pins.
AOUT0-AOUT8	When the priority encoder option is used, the match address output pins identify the matched address resulting from a search operation. The priority encoder generates the match address; if multiple CAM entries match the input data during a search operation, only the lowest of these addresses will appear on the match output address pins. If no match is found, the pins will go high. The number of pins used is the same as the number of address input pins, dependent on the word count of the array selected. Pins are used starting at the AOUT0 least significant bit and counting upwards. The 64-word configurations use AOUT0–AOUT5. The 512-word configurations use AOUT0–AOUT8. The results of a search of the array are latched in the output; therefore, the results of a search remain on the match address output pins until the next search operation. Read and write operations do not affect the match address output pins.
HITMISS	When the priority encoder option is used, the hit/miss pin will go high if one or more matching entries are found during a search operation. The pin will remain high until the next search operation which results in a “no match.”
MULTHIT	When the priority encoder option is used, the multiple hit pin will go high if more than one matching entries are found during a search operation. The pin will remain high until the next search operation which results in a “no match.”

Table 108. Pin Definitions (Continued)

Pin	Description
MLLN000–MLLN511	When the priority encoder option is not used, the output of each match line is routed directly to a match line latch output pin. During a search operation, the MLLN pins will go low for matching entries and high for non-matching entries. The number of pins used is the same as the word count of the array, so the 64-word configurations use MLLN000–MLLN063. The 512-word configurations use MLLN000–MLLN511. The results of a search of the array are latched in the output; therefore, the results of a search remain on the match latch output pins until the next search operation. Read and write operations do not affect the match latch output pins.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the CAM. The CAM can be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.
SOML0 and SOML1	SOML0 and SOML1 are the scan-out pins for the match line latches. These strings may be placed in a scan path with other elements on a chip, and must be used to conform to LSSD test requirements. The number of SOML pins required is a function of configuration. The 64 word configurations use SOML0 only. The 512 word configurations use SOML0 and SOML1. If the SOML1 pin is not required, it will not appear in the logical or physical models; therefore, no tie-off procedure is required.
SOBL0 and SOBL1	SOBL0 and SOBI1 are the scan-out pins for the match line BIST compare latches. These strings may be placed in a scan path with other elements on a chip, and follow the same rules as for the SOML0 and SOML1 pins.
PASSFAIL	The PASSFAIL pin is the pass/fail indicator during BIST testing and must be routed to the accompanying CAMBIST controller for the array. The PASSFAIL pin must not be connected to anything other than the CAMBIST controller. Note that this pin is “nonvalidated” and cannot be monitored directly to determine if there are fails in the array. The CAMBIST controller “validates” the results from this pin by observing it only during the valid BIST read cycles.
DIAGOUT	The diagnostic output pin is logically the same as the PASSFAIL pin, but is used for diagnostics to observe the pass/fail flag of individual arrays directly. The DIAGOUT must be routed to a primary output, but can be multiplexed with other outputs.

Array Functional Operation

Definition

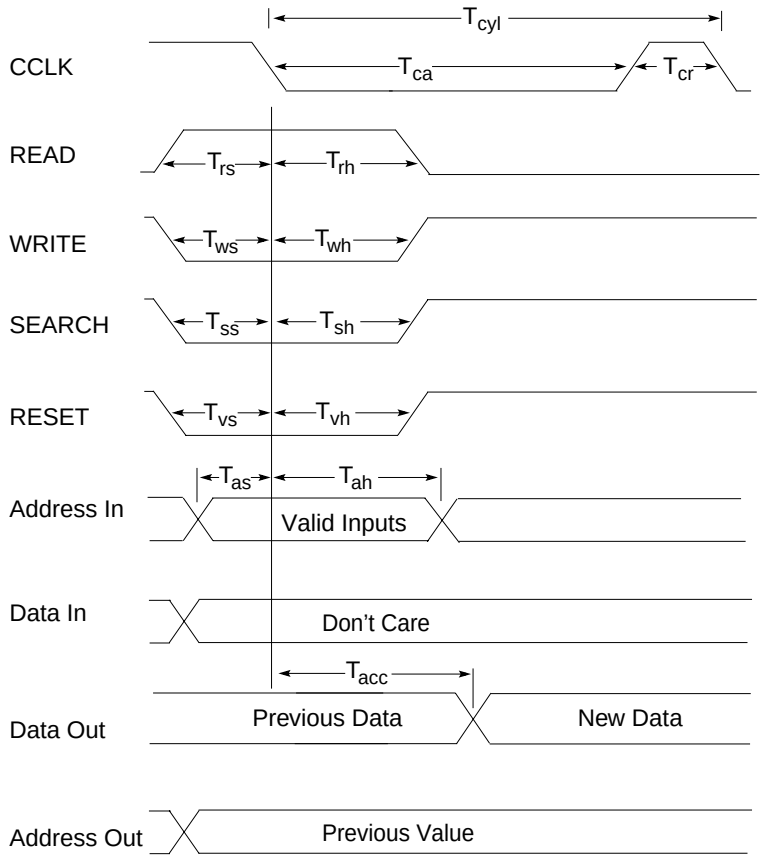
Array functional operation is the normal operation of the CAM when the BIST controller is inactive. Array functional operations include read, write, search, and reset. These operations are mutually exclusive, so only one of the READ, WRITE, SEARCH, or RESET pins may be active when the CCLK is activated. The CAM operations are similar to the array clocked mode operations of ASIC SRAMs and ROMs. The read, write, search, or reset operations are synchronized by activating the READ, WRITE, SEARCH, or RESET inputs before initiating the cycle by dropping the CCLK input. If none of the four operations is activated, the falling CCLK will not initiate an array access.

Array Clocking Modes

Array Clocked Read

- READ is held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data is read from the entry in the CAM indicated by the address input pins to the data out pins after the access time has elapsed.
- The valid bit for that entry is read to the DOUTV pin.
- Data out is valid until the next read cycle.

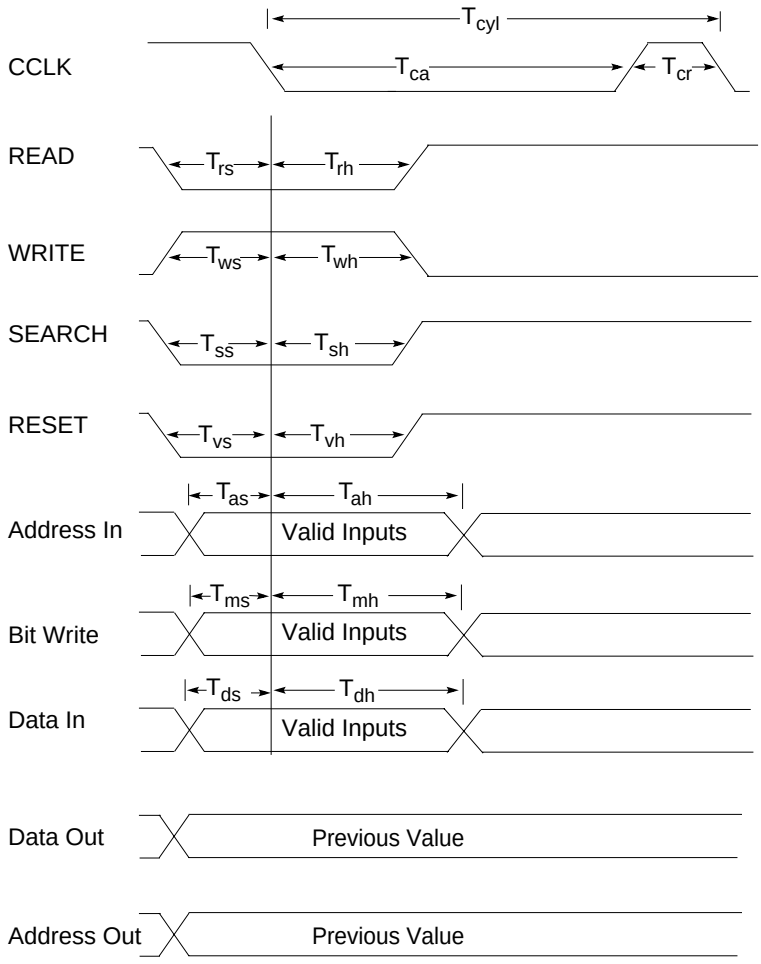
Figure 57. Array Clocked Read Timing



Array Clocked Write

- WRITE is held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data-in is written into the entry in the CAM indicated by the address input pins.
- Only data in pins whose corresponding bit write pins are active high are written to. Data in pins whose corresponding bit write pins are inactive low retain the previous contents of the array in those bits.
- The DINV pin value is written to the valid bit for that entry.
- The DINV pin is normally held high during a write operation, to set the valid bit for that entry to the valid state.
- Data out does not change during a write cycle.

Figure 58. Array Clocked Write Timing



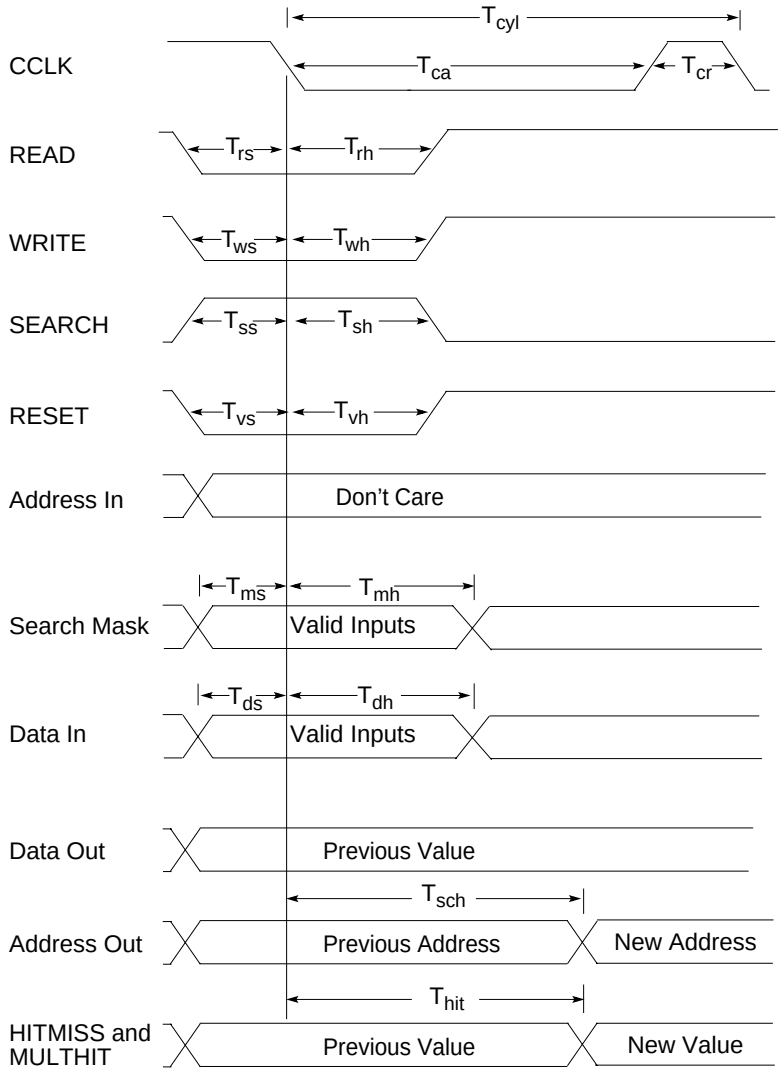
Array Clocked Search for Data with Priority Encoder

- SEARCH is held high or brought high before the CCLK edge.
- DINV is held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data in is compared to all entries in the CAM which have their valid bit set to the high “valid” state. Entries with their valid bit set to the low “invalid” state are ignored during the search operation.
- Only data in pins whose corresponding search mask pins are active high are used in the comparison. Data in pins whose corresponding search mask pins are inactive low are ignored during the search operation.
- If all of search mask pins are inactive low during the search operation, the address out pins will indicate the lowest entry with a valid bit equal 1 after the search time has elapsed.
- The HITMISS flag goes high if one or more matches are found, or low if no matches are found.
- The MULTHIT flag goes high if more than one matches are found, or low if one or no matches are found.
- If there is one match, the address of the matched entry appears at the address out pins after the search time has elapsed.
- If there is more than one match, the address of the lowest matched entry appears at the address out pins after the search time has elapsed.
- If there is no match, all of the address out pins will go high after the search time has elapsed.
- Data out does not change during a search cycle.
- The search cycle time is longer than the read, write, or reset cycle times.

Array Clocked Search for Next Available Empty Address with Priority Encoder

- SEARCH is held high or brought high before the CCLK edge.
- DINV is held low or brought low before the CCLK edge.
- All SMBW search mask pins held inactive low or brought low before the CCLK edge.
- CCLK falling initiates the access cycle.
- The HITMISS flag goes high if one or more empty addresses are found, or low if none are found.
- The MULTHIT flag goes high if more than one empty addresses are found, or low if one or none are found.
- The address of the lowest empty address (valid bit = 0) appears at the address out pins after the search time has elapsed.
- If there are no empty addresses, all of the address out pins will go high after the search time has elapsed; both HITMISS and MULTHIT go low.
- Data out does not change during a search cycle.
- The search cycle time is longer than the read, write, or reset cycle times.

Figure 59. Array Clocked Search Timing with Priority Encoder



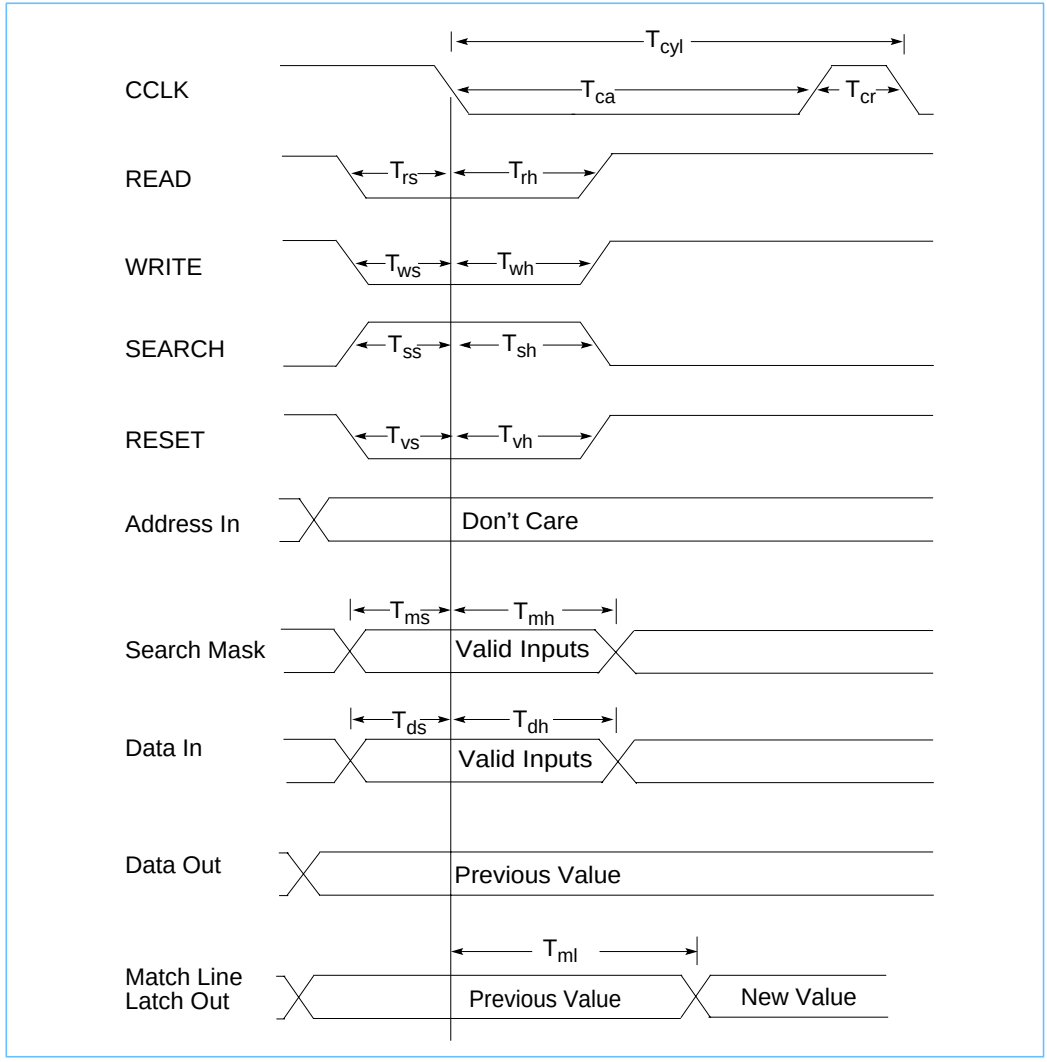
Array Clocked Search for Data without Priority Encoder

- SEARCH is held high or brought high before the CCLK edge.
- DINV is held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- Data in is compared to all entries in the CAM which have their valid bit set to the high “valid” state. Entries with their valid bit set to the low “invalid” state are ignored during the search operation.
- Only data in pins whose corresponding search mask pins are active high are used in the comparison. Data in pins whose corresponding search mask pins are inactive low are ignored during the search operation.
- If all of search mask pins are inactive low during the search operation, the match line out pins will indicate the lowest entry with a Valid Bit equal 1, after the search time has elapsed.
- The match line out pins will go low for every entry containing a match after the search time has elapsed. Non-matching pins will remain high.
- If there are no matches, all of the match line out pins will remain high after the search time has elapsed.
- Data out does not change during a search cycle.
- The search cycle time is longer than the read, write, or reset cycle times.

Array Clocked Search for Next Available Empty Address without Priority Encoder

- SEARCH is held high or brought high before the CCLK edge.
- DINV is held low or brought low before the CCLK edge.
- All BWSM search mask pins held inactive low or brought low before the CCLK edge.
- CCLK falling initiates the access cycle.
- The match line out pins will go low for every empty address (valid bit = 0) after the search time has elapsed. Pins for occupied locations will remain high.
- Data out does not change during a search cycle.
- The search cycle time is longer than the read, write, or reset cycle times.

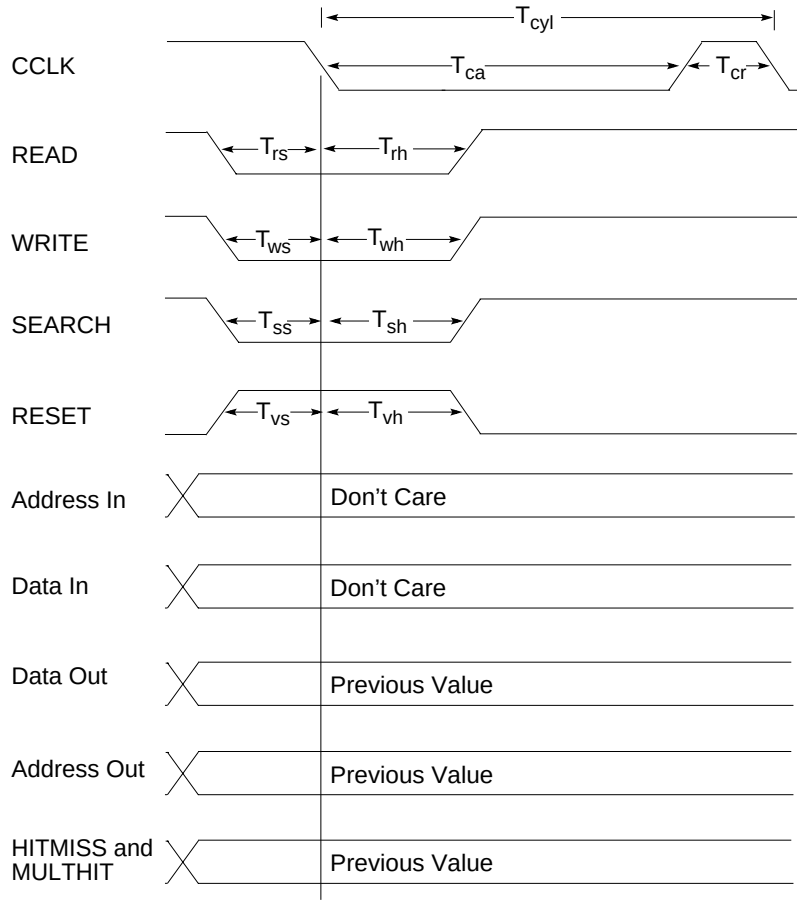
Figure 60. Array Clocked Search Timing without Priority Encoder



Array Clocked Reset

- RESET is held high or brought high before the CCLK edge.
- CCLK falling initiates the access cycle.
- The valid bit for every CAM entry is reset to the low “invalid” state, to blanket invalidate all of the entries in the CAM.
- The data out, address out, HITMISS, and MULTHIT pins do not change during a reset cycle.

Figure 61. Array Clocked Reset Timing



Delay Definitions

Table 109 on page 264 and Table 110 on page 265 show setup and hold times for representative “small” and “large” CAMBPE arrays. An equivalent configuration CAMBML array would have similar timings.

Table 109. "Small" CAMBPE0064X08M1

Timing Parameter	Abbreviation	Minimum (ns)
Array Clocked Mode		
CCLK minimum active time	T_{ca}	4.8
CCLK minimum restore time	T_{cr}	2.8
READ setup time	T_{rs}	0.4
READ hold time	T_{rh}	0.3
WRITE setup time	T_{ws}	0.4
WRITE hold time	T_{wh}	0.3
SEARCH setup time	T_{ss}	0.4
SEARCH hold time	T_{sh}	0.3
RESET setup time	T_{vs}	0.4
RESET hold time	T_{vh}	0.3
Address in setup time	T_{as}	0.5
Address in hold time	T_{ah}	0.6
Data in setup time	T_{ds}	0.1
Data in hold time	T_{dh}	0.1
Search mask or bit write in setup time	T_{ms}	0.1
Search mask or bit write in hold time	T_{mh}	0.1
Read access time	T_{acc}	3.3
Search access time to address out (with priority encoder)	T_{sch}	6.8
Search access time to match line out (without priority encoder)	T_{ml}	5.2

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 109. "Small" CAMBPE0064X08M1 (Continued)

Timing Parameter	Abbreviation	Minimum (ns)
Hit/miss flag access time (with priority encoder)	T_{hit}	6.8
Multi-hit flag access time (with priority encoder)	T_{mult}	6.8
Cycle time	T_{cyl}	6.9

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 110. "Large" CAMBPE0512X64M1

Timing Parameter	Abbreviation	Minimum (ns)
Array Clocked Mode		
CCLK minimum active time	T_{ca}	4.7
CCLK minimum restore time	T_{cr}	2.9
READ setup time	T_{rs}	0.5
READ hold time	T_{rh}	0.4
WRITE setup time	T_{ws}	0.5
WRITE hold time	T_{wh}	0.4
SEARCH setup time	T_{ss}	0.5
SEARCH hold time	T_{sh}	0.4
RESET setup time	T_{vs}	0.5
RESET hold time	T_{vh}	0.4
Address in setup time	T_{as}	0.5
Address in hold time	T_{ah}	0.8
Data in setup time	T_{ds}	0.0

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Table 110. "Large" CAMBPE0512X64M1 (Continued)

Timing Parameter	Abbreviation	Minimum (ns)
Data in hold time	T_{dh}	0.8
Search mask or bit write in setup time	T_{ms}	0.0
Search mask or bit write in hold time	T_{mh}	0.8
Read access time	T_{acc}	3.5
Search access time to address out (with priority encoder)	T_{sch}	8.5
Search access time to match line out (without priority encoder)	T_{ml}	5.6
Hit/miss flag access time (with priority encoder)	T_{hit}	8.5
Multi-hit flag access time (with priority encoder)	T_{mult}	8.5
Cycle time	T_{cyl}	7.6

Note: Timings quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125˚C, and process = slow.

Area, Timing, and Power Estimates

Web Compiler Data

Complete area, timing, and power consumption data for array instances can be calculated using tools available on the World Wide Web. To obtain access to these tools, contact your IBM ASICs representative. The tools allow the user to enter the desired word and bit counts for an array to obtain its physical dimensions, chip cell counts, delays, and effective capacitance for power calculations.

Power Dissipation Calculations

To estimate the power consumption of a CAMB for a particular application, use the following equation.

$$P = (A_{read} \times RC_{int} + A_{write} \times WC_{int} + A_{search} \times SC_{int} + A_{reset} \times TC_{int} + A_{no\text{-}op} \times NC_{int}) \times V_{dd}^2 \times F_{CAM}$$

where:

- P = Power in microwatts.
- RC_{int} = Internal capacitance for a read access of the CAM in pF. C_{int} values can be obtained from the World Wide Web estimator or an IBM ASICs representative.
- WC_{int} = Internal capacitance for a write to the CAM in pF.
- SC_{int} = Internal capacitance for a search access of the CAM in pF.
- TC_{int} = Internal capacitance for a reset of the CAM in pF.
- NC_{int} = Internal capacitance for a no-op of the CAM in pF, where no read, write, search, or reset operation is performed, but the CAM CCLK is activated.
- A_{read} = Read activity factor, which is the fraction of the total clock cycles that a read operation is performed (a value between 0 and 1).
- A_{write} = Write activity factor, which is the fraction of the total clock cycles that a write operation is performed (a value between 0 and 1).
- A_{search} = Search activity factor, which is the fraction of the total clock cycles that a search operation is performed (a value between 0 and 1).
- A_{reset} = Reset activity factor, which is the fraction of the total clock cycles that a reset operation is performed (a value between 0 and 1).
- $A_{no\text{-}op}$ = No-op activity factor, which is the fraction of the total clock cycles that no operation is performed (a value between 0 and 1).
- The sum of ($A_{read} + A_{write} + A_{search} + A_{reset} + A_{no\text{-}op}$) must be less than or equal to 1.
- V_{dd} = Power supply voltage of the chip in volts.
- F_{CAM} = Clock frequency applied to the CAM, in MHz.

Search Power Reduction

The CAMB has an architectural feature to reduce power dissipation during searches of the array. There are two levels of hierarchy in matching bits along each word. Four bits are sampled first; the remaining the bits are sampled only if all four of the sampled bits match. If the data stored in the four sampled bit positions is truly random in all of the entries in the CAM, then on average, only one out of sixteen match lines will dissipate the full search power on each search.

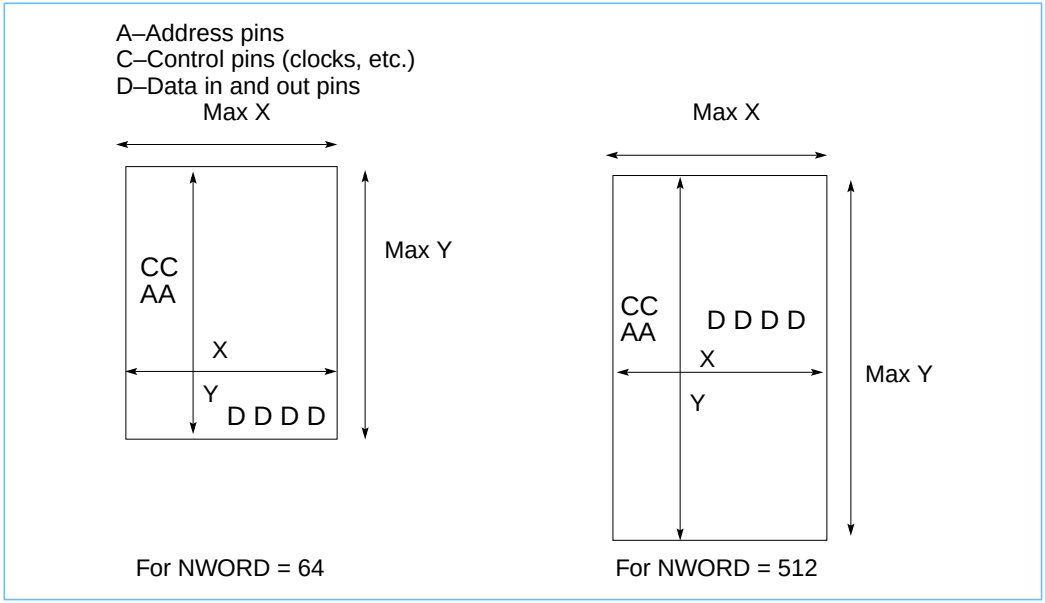
In order to achieve this power savings, select the four bit positions in the data field that will be most random—these bits should not be placed where there may be a common field in many entries. Four unique bit positions must be used, and these four will be coded in the “PppPppPppPpp” field of the instance name to distinguish this physical array from others. Since the power calculation for search operations assumes that this power reduction is being used, it is important that these bits are chosen carefully.

Note that there is no logical or timing model difference for these four bits. The only difference is in the logically transparent gating of the internal match line search circuitry.

Array Area and Footprint

Figure 62 on page 269 shows the relative locations of the pins within the rectangular shape of the CAM. The dimensions for representative configurations are shown in Table 111 on page 271 and Table 112 on page 272.

Figure 62. CAMB Footprint



Combining Arrays

While CAMB is limited to either 64 or 512 words per instance, and up to 64 data bits per word, it is possible to create larger arrays by combining instances. To create deeper word depths, multiple CAMBs of the desired width can be combined. For example, to create a 2048 x 32 array, four instances of 512 x 32 would be used. The data buses would be run to all four instances and to the common control lines. The lowest nine address lines would be connected to all four instances, and the two most significant address bits would drive a decoder to route the C clock to one of the four instances. If CAMBPE configurations are used, the address outputs of the four arrays would drive an external stage of priority encoder logic to create the combined output address. If CAMBML configurations are used, the match line outputs of all four arrays would be combined using whatever external logic the application requires.

To create a wider data width array, CAMBML configurations must be used. For exam-

ple, to create a 512 x 96 array, two instances of 512 x 48 would be used. The control lines, clocking, and address lines would be connected to both. The first 48 data lines would be run to the first instance, and the second 48 to the second. The corresponding match line output pins from the two arrays would be ANDed together and input to priority encoding logic. For example, MLLN000 from the first instance would be ANDed with MLLN000 from the second, and MLLN001 with MLLN001, and so on. Thus, the contents of both arrays would have to match to activate a match for that entry.

Additional documentation on how to combine CAM arrays is available from your IBM ASICs representative.

Scan Chain Definition

LSSD Latch Count Calculations

The total number of latches in the CAM is dependent on the configuration of the CAM, and can be calculated using the following equations for the four options:

64 words with priority encoder	Total latches = 157 + NBIT
512 words with priority encoder	Total latches = 1082 + NBIT
64 words without priority encoder	Total latches = 157 + NBIT
512 words without priority encoder	Total latches = 1082 + NBIT

where: NBIT = number of data bits per word

These latches are grouped into multiple scan chains within the CAM. The primary chain between the SCANIN and SCANOUT pins contains:

64 words with priority encoder	29
512 words with priority encoder	58
64 words without priority encoder	29
512 words without priority encoder	58

Separate chains are used for the match line latches and the match line compare latches, with a maximum of 256 latches per chain. These scan chains are used as follows:

SIML0, SOML0	always used
SIML1, SOML1	used if NWORD = 512
SIBL0, SOBL0	always used
SIBL1, SOBL1	used if NWORD = 512

Data Tables

Table 111. CAMBPE Timings, Internal Capacitance, and Physical Area Examples

Array Size	Read Access Time (ns)	Search Access Time (ns)	Read Cycle Time (ns)	Search Cycle Time (ns)	Read Internal Cap (pF)	Search Internal Cap (pF)	Physical Area (cell units)	Max X Dimension (cell units)	Max Y Dimension (cell units)
64 x 8	3.3	6.8	6.9	6.9	13	19	35068	437	99
64 x 64	3.5	7.0	7.6	7.6	58	57	66055	750	99
512 x 8	3.3	8.4	7.3	7.3	18	88	184764	471	400
512 x 64	3.5	8.5	7.4	7.4	65	229	309964	784	400

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Table 112. CAMBML Timings, Internal Capacitance, and Physical Area Examples

Array Size	Read Access Time (ns)	Search Access Time (ns)	Read Cycle Time (ns)	Search Cycle Time (ns)	Read Internal Cap (pF)	Search Internal Cap (pF)	Physical Area (cell units)	Max X Dimension (cell units)	Max Y Dimension (cell units)
64 x 8	3.3	5.2	6.9	6.9	13	17	33781	389	99
64 x 64	3.5	5.3	7.6	7.6	58	56	64768	702	99
512 x 8	3.3	5.5	7.3	7.3	18	85	165764	408	400
512 x 64	3.5	5.6	7.4	7.4	65	226	290964	721	400

Notes:

1. The access times, internal capacitances, and physical areas quoted above are for the sizes listed. These parameters vary with array size.
2. Access times are quoted for a clock input fall time = 250 ps, output pin load = 0.2 pF, V_{dd} = 1.65V, temperature = 125°C, and process = slow. Actual access times will vary with application and environmental conditions.
3. Power (µW) = Internal capacitance (pF) x operating frequency (MHz) x V^2_{dd}.
4. The arrays are nonrectangular. Maximum dimensions are given for a rectangle enclosing the entire array. Cell count is given for the number of cell units actually blocked by the outline of the array. A cell unit is 0.56 x 6.72 µm.

Soft Error Sensitivity

There is a very small probability that the state of an SRAM bit may be flipped if struck by a cosmic particle traveling through space or by an alpha particle emitted by the chip packaging materials. For applications storing mission-critical data in an SRAM, calculating this soft error rate (SER) is recommended. To obtain soft error rate specifications, contact your IBM representative.

CAMBBIST—BIST Controller for Binary CAMs

Features

- Complete test of all array functions
- Up to 16 arrays tested in parallel from one controller
- Optional search address result priority encoder

The key features of the macro are summarized in Table 113.

Table 113. CAMBBIST Controller Features

Feature	Capability
Supported V_{dd} range	0.90V–1.95V
Macro dimensions	479 x 19 chip unit cells
Macro area	9101 chip unit cells
DC test methodology	Multiple array BIST
AC test methodology	Cycle and access time
Global porosity on M1	0%
Global porosity on M2	50%
Global porosity on M3	75%

CAMBBIST Description

The CAMBBIST controller performs all of the necessary tests for the arrays during product test by applying addresses, data inputs, search mask, bit write, and read, write, search, reset controls to the array. The CAMBBIST control signals are multiplexed with the functional inputs for the address, data, and control signals, with minimal impact on the CAM access and setup and hold times.

Usage Requirements

Whenever one or more CAMB arrays are used in a chip design, one or more CAMBBIST controllers must also be used to generate the BIST test patterns required for veri-

fying the CAMs during product test. One CAMBBIST controller can be used to test up to 16 CAMB arrays of any data width. The same CAMBBIST controller for arrays both with and without the address priority encoder option.

The CAMBBIST must be scan or flush initialized to all zeroes before testing begins.

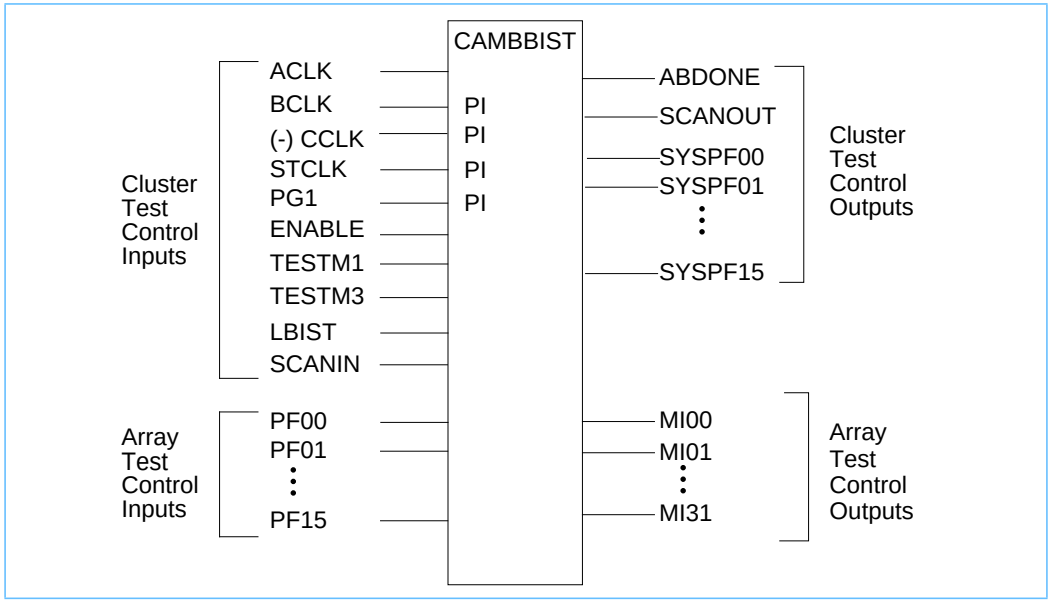
Symbol Naming Conventions

There are two CAM BIST controllers: **CAMBBIST064** is used to control the 64-word CAM, and **CAMBBIST512** is used to control the 512-word CAM.

Logical Description

A symbolic representation of the CAMBBIST is shown in Figure 63.

Figure 63. CAMBBIST Logic Symbol



Pin Definitions

Table 114 summarizes the function and proper usage of the macro pins shown in Figure 63 on page 274.

Table 114. CAMBBIST Pin Definitions

Pin	Description
CCLK	The C clock pin is used only during test operations, and not during array mode operation of the CAM.This pin is active high during BIST operations, and must come from a primary input but may be common with other LSSD C clocks on the chip. During array functional mode operation, the preferred state of this pin in “inactive” to reduce power consumption in the BIST logic.
ACLK	The A clock pin is used only during test operations, and not during array mode operation of the CAM. This pin must come from a primary input but may be common with other LSSD A clocks on the chip. The A clock is active high during scan operations and must be held low during array mode operation.
BCLK	The B clock pin is used only during test operations, and not during array mode operation of the CAM. This pin must come from a primary input but may be common with other LSSD B clocks on the chip. The B clock is active high during scan operations and must be held low during array mode operation.
STCLK	The system test oscillator clock pin is used only during test operations and not during array mode operation of the CAM. During array functional mode operation, the preferred state of this pin in “inactive” to reduce power consumption in the BIST logic.
PG1	The C clock gate pin is used to gate the CCLK signal. This pin is usually held high, unless it is used during LBIST operations.
ENABLE	The self-test clock enable pin is used to gate the STCLK signal. This pin is usually held high unless it is used during LBIST operations.
LBIST	The LBIST pin must be held high during system LBIST testing, to block the B clock to the CAMs, and must be held low during logic flush and scan operations.
TESTM1	The TESTM1 pin is used together with the TESTM3 pin to set the test state of the BIST controller and the attached CAMs. TESTM1 is held low for functional operation of the CAMs.
TESTM3	The TESTM3 pin is used together with the TESTM1 pin to set the test state of the BIST controller and the attached CAMs. TESTM3 is held low for functional operation of the CAMs, and must be routed from a chip primary input.
SCANIN	The scan-in pin is a standard LSSD pin for the scannable latches internal to the CAMBBIST. The CAMBBIST may be placed in a scan path with other elements on a chip. The scan-in pin must be used to conform to LSSD test requirements.

Table 114. CAMBBIST Pin Definitions (Continued)

Pin	Description
PF00–PF15	The PF pins are array test inputs which receive the pass/fail state of the arrays on each BIST test cycle. One PF pin is connected to each array being tested. Unused PF pins must be tied to ground.
MI00–MI31	The test interface pins are connected to the CAM(s) being controlled, and control the CAM(s) during BIST testing. The MInn pins must not be connected to anything other than CAMs. The 64-word configurations use MI00–MI28. The 512-word configurations use MI00–MI31.
SYSPF00–SYSPF15	The SYSPF pins are cluster test outputs which allow the CAMBBIST pass/fail bits to be observed by on-chip system test logic without requiring a scan operation. These pins are not required to be connected.
ABDONE	The ABDONE output pin will be high during BIST testing and will go low when the BIST testing is completed.
SCANOUT	The scan-out pin is a standard LSSD pin from the scannable latches internal to the CAMBBIST. The CAMBBIST may be placed in a scan path with other elements on a chip. The scan-out pin must be used to conform to LSSD test requirements.

Array Area and Footprint

The CAMBBIST controller is a rectangle, 479 unit cells wide by 19 cells high, resulting in a total area of 9101 unit cells.

Scan Chain Definition

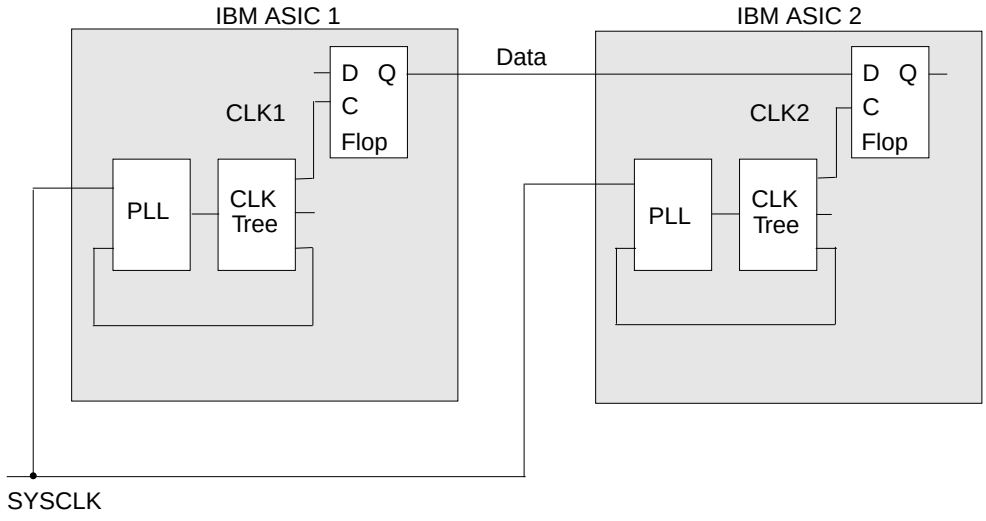
LSSD Latch Count Calculations

The total number of latches is fixed at 121.

Phase-Locked Loop

Phase-Locked Loop

PLL Utilization in ASICs



SYSCLK, CLK1, and CLK2 are all in phase

Phase-locked loops (PLLs) are used primarily for clock-tree deskewing in ASIC chips. For systems utilizing PLLs in every ASIC, the flip-flops in each chip will receive clock edges at the same time. The internal ASIC clocks are phase-aligned to a common system clock. Since all clocks in the system are common, high-speed synchronous data transmission is possible between ASICs. The accuracy to which the PLL can align clocks is determined to a large extent by the PLL's static phase-error and phase-jitter specifications.

In addition to the clock deskewing function, the PLL will also provide clock frequency multiplication. A lower speed external clock can be multiplied to obtain a higher speed clock on the ASIC. This feature takes advantage of the intrinsic speed of the ASIC silicon without creating complex board-wiring issues.

Phase-Locked Loop Highlights

- Two offerings:

PLL7SFLIBE	External reference clock, standard voltage
PLL7SFLIBI	Internal reference clock, standard voltage
PLL7SFLIBEDV	External reference clock, dual voltage
PLL7SFLIBIDV	Internal reference clock, dual voltage

- Synchronizes internal clocks to system clock
- Fully integrated mixed-mode PLL design
- Wide lock-in range: 33 MHz–1 GHz
- Programmable multiplication factor from 1 to 16
- Digital tuning bits for jitter minimization
- Three outputs:

PLLOUTA	Standard output
PLLOUTB	Selectable ratios of PLLOUTA
PLLOUTC	PLLOUTB shifted by 90˚

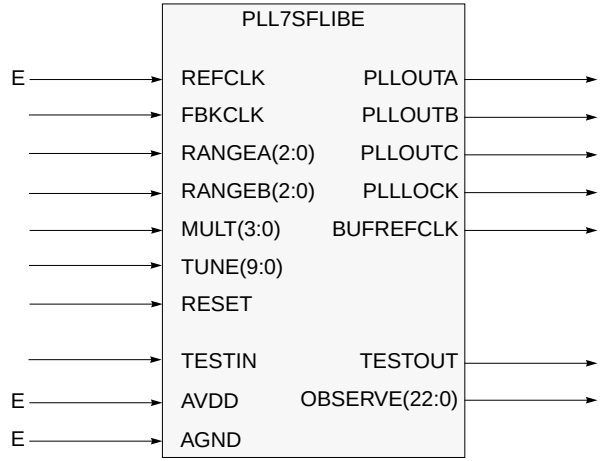
- Low jitter:

Cycle–cycle jitter	Less than ± 100 ps
Input–output jitter	Less than ± 200 ps

- Bypass mode
- Three I/Os (PLL7SFLIBE, PLL7SFLIBEDV); two I/Os (PLL7SFLIBI, PLL7SFLIBIDV)
- 117,348 internal cells (PLL7SFLIBE, PLL7SFLIBI); 125,552 internal cells (PLL7SFLIBEDV, PLL7SFLIBIDV)
- Up to four PLLs allowed per die
- Available on all SA-27E dies and packages

Macros: PLL7SFLIBE

Standard voltage (V_{dd} = analog V_{dd} = 1.8V)
External reference, internal feedback:
REFCLK is sourced off-chip.
FBKCLK is sourced on-chip.



Notes:

1. E = external pins.
2. External pins connect directly to I/O pads; no receiver is required.

PLL7SFLIBE Pin Definitions

Table 115. PLL7SFLIBE Input Pin Definitions

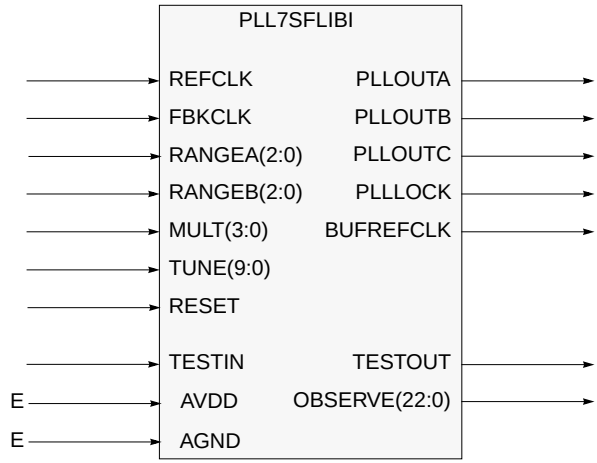
Pin	Definition
REFCLK	Reference clock
FBKCLK	Feedback clock
RANGEA(2:0)	PLLOUTA frequency selector
RANGEB(2:0)	PLLOUTB/C frequency selector
MULT(3:0)	Frequency multiplication factor
TUNE(9:0)	Loop stability tuning bits
RESET	Reset and bypass mode enable
TESTIN	Functional test enable
AVDD	Analog V_{dd}
AGND	Analog GND

Table 116. PLL7SFLIBE Output Pin Definitions

Pin	Definition
PLLOUTA	Primary PLL output
PLLOUTB	Secondary PLL output
PLLOUTC	90° phase-shifted output
PLLLOCK	Output indicating a *locked* state
BUFREFCLK	Buffered REFCLK
TESTOUT	Functional test output
OBSERVE(22:0)	LSSD observe points

Macros: PLL7SFLIBI

Standard voltage (V_{dd} = analog V_{dd} = 1.8V)
Internal reference, internal feedback:
REFCLK is sourced on-chip.
FBKCLK is sourced on-chip.



Notes:

1. E = external pins.
2. External pins connect directly to I/O pads; no receiver is required.

PLL7SFLIBI Pin Definitions

Table 117. PLL7SFLIBI Input Pin Definitions

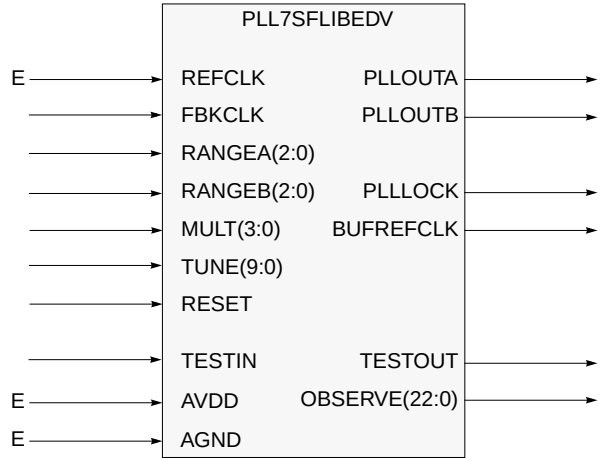
Pin	Definition
REFCLK	Reference clock
FBKCLK	Feedback clock
RANGEA(2:0)	PLLOUTA frequency selector
RANGEB(2:0)	PLLOUTB/C frequency selector
MULT(3:0)	Frequency multiplication factor
TUNE(9:0)	Loop stability tuning bits
RESET	Reset and bypass mode enable
TESTIN	Functional test enable
AVDD	Analog V_{dd}
AGND	Analog GND

Table 118. PLL7SFLIBI Output Pin Definitions

Pin	Definition
PLLOUTA	Primary PLL output
PLLOUTB	Secondary PLL output
PLLOUTC	90° phase-shifted output
PLLLOCK	Output indicating a *locked* state
BUFREFCLK	Buffered REFCLK
TESTOUT	Functional test output
OBSERVE(11:0)	LSSD observe points

Macros: PLL7SFLIBEDV

Dual voltage (V_{dd} = 1.5V, analog V_{dd} = 1.8V)
External reference, internal feedback:
REFCLK is sourced off-chip.
FBKCLK is sourced on-chip.



Notes:

1. E = external pins.
2. External pins connect directly to I/O pads; no receiver is required.

PLL7SFLIBEDV Pin Definitions

Table 119. PLL7SFLIBEDV Input Pin Definitions

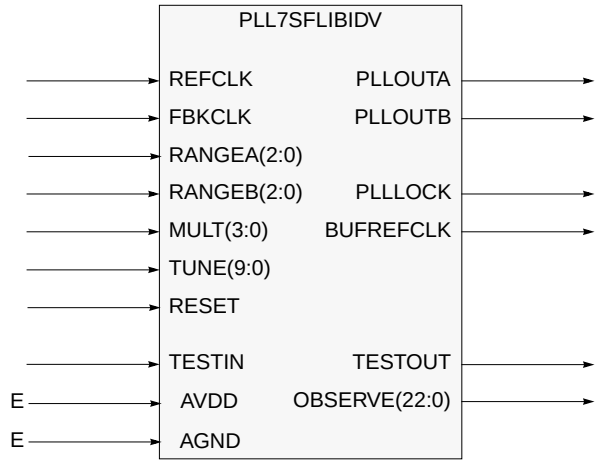
Pin	Definition
REFCLK	Reference clock
FBKCLK	Feedback clock
RANGEA(2:0)	PLLOUTA frequency selector
RANGEB(2:0)	PLLOUTB frequency selector
MULT(3:0)	Frequency multiplication factor
TUNE(9:0)	Loop stability tuning bits
RESET	Reset and bypass mode enable
TESTIN	Functional test enable
AVDD	Analog V_{dd}
AGND	Analog GND

Table 120. PLL7SFLIBEDV Output Pin Definitions

Pin	Definition
PLLOUTA	Primary PLL output
PLLOUTB	Secondary PLL output
PLLLOCK	Output indicating a *locked* state
BUFREFCLK	Buffered REFCLK
TESTOUT	Functional test output
OBSERVE(22:0)	LSSD observe points

Macros: PLL7SFLIBIDV

Dual voltage (V_{dd} = 1.5, analog V_{dd} = 1.8V)
Internal reference, internal feedback:
REFCLK is sourced on-chip.
FBKCLK is sourced on-chip.



Notes:

1. E = external pins.
2. External pins connect directly to I/O pads; no receiver is required.

PLL7SFLIBIDV Pin Definitions

Table 121. PLL7SFLIBIDV Input Pin Definitions

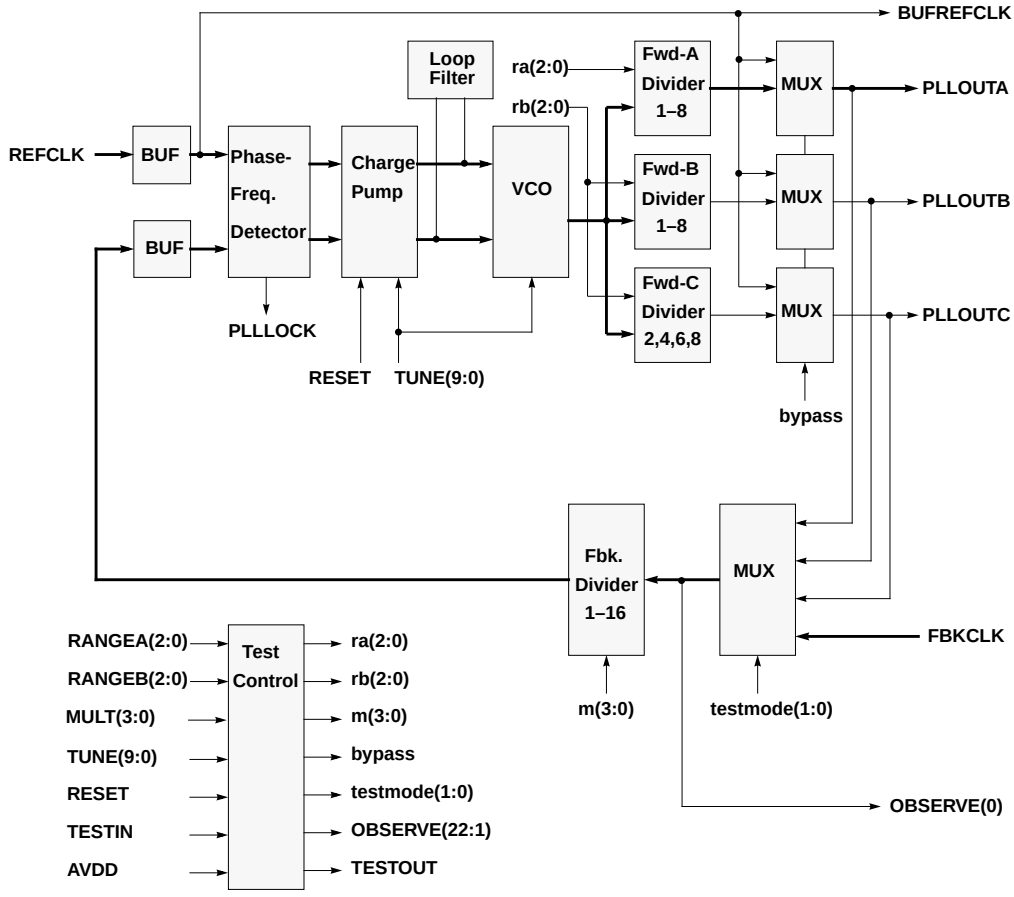
Pin	Definition
REFCLK	Reference clock
FBKCLK	Feedback clock
RANGEA(2:0)	PLLOUTA frequency selector
RANGEB(2:0)	PLLOUTB frequency selector
MULT(3:0)	Frequency multiplication factor
TUNE(9:0)	Loop stability tuning bits
RESET	Reset and bypass mode enable
TESTIN	Functional test enable
AVDD	Analog V_{dd}
AGND	Analog GND

Table 122. PLL7SFLIBIDV Output Pin Definitions

Pin	Definition
PLLOUTA	Primary PLL output
PLLOUTB	Secondary PLL output
PLLLOCK	Output indicating a *locked* state
BUFREFCLK	Buffered REFCLK
TESTOUT	Functional test output
OBSERVE(11:0)	LSSD observe points

Block Diagram and Truth Tables

Figure 64. PLL Low-Level Block Diagram



Notes:

1. Lower case signals are for PLL internal use only.
2. PLLOUTC is available on PLL7SFLIBE and PLL7SFLIBI only.

Table 123. PLL Mode Selection Truth Table

Conditions	REFCLK	FBKCLK PLLOUTA, B, or C	RESET	TESTIN	AVDD	AGND	PLLOUT A, B, C Frequency	PLLLOCK	BUFREFCLK	TESTOUT	OBSERVE 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
Normal Operation																																	
PLL Locked	X	OUT	0	0	1	0	REFCLK x MULT	1	REFCLK	0	0	RANGEA0	RANGEA1	RANGEA2	RANGEB0	RANGEB1	RANGEB2	MULT0	MULT1	MULT2	MULT3	TUNE0	TUNE1	TUNE2	TUNE3	TUNE4	TUNE5	TUNE6	TUNE7	TUNE8	TUNE9	RESET	AVDD+TESTIN
PLL Unlocked	X	≠OUT	0	0	1	0	X	0	REFCLK	0	0																						
LSSD Test Mode	X	X	X	X	0	0	REFCLK	0	REFCLK	0	FBKCLK																						
Reset/ Bypass Mode	X	X	1	0	X	0	REFCLK	0	REFCLK	0	FBKCLK																						
PLL Functional Test Mode	X	X	1	1	1	0	X	X	REFCLK	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 124. PLL Functional Modes Truth Table: PLLOUTA (External-Divider=1)

Conditions (Normal Operation)	REFCLK	FBKCLK	RANGEA			MULT				PLLOUTA Frequency
			2	1	0	3	2	1	0	
PLL Locked	X	PLLOUTA	0	0	0	X	X	X	X	65 MHz–125 MHz
PLL Locked	X	PLLOUTA	0	0	1	X	X	X	X	70 MHz–140 MHz
PLL Locked	X	PLLOUTA	0	1	0	X	X	X	X	83 MHz–166 MHz
PLL Locked	X	PLLOUTA	0	1	1	X	X	X	X	100 MHz–200 MHz
PLL Locked	X	PLLOUTA	1	0	0	X	X	X	X	125 MHz–250 MHz
PLL Locked	X	PLLOUTA	1	0	1	X	X	X	X	166 MHz–333 MHz
PLL Locked	X	PLLOUTA	1	1	0	X	X	X	X	250 MHz–500 MHz
PLL Locked	X	PLLOUTA	1	1	1	X	X	X	X	500 MHz–1000 MHz
PLL Locked	X	PLLOUTA	X	X	X	0	0	0	0	REFCLK x 16
PLL Locked	X	PLLOUTA	X	X	X	0	0	0	1	REFCLK x 1
PLL Locked	X	PLLOUTA	X	X	X	0	0	1	0	REFCLK x 2
PLL Locked	X	PLLOUTA	X	X	X	0	0	1	1	REFCLK x 3
PLL Locked	X	PLLOUTA	X	X	X	0	1	0	0	REFCLK x 4
PLL Locked	X	PLLOUTA	X	X	X	0	1	0	1	REFCLK x 5
PLL Locked	X	PLLOUTA	X	X	X	0	1	1	0	REFCLK x 6
PLL Locked	X	PLLOUTA	X	X	X	0	1	1	1	REFCLK x 7
PLL Locked	X	PLLOUTA	X	X	X	1	0	0	0	REFCLK x 8
PLL Locked	X	PLLOUTA	X	X	X	1	0	0	1	REFCLK x 9
PLL Locked	X	PLLOUTA	X	X	X	1	0	1	0	REFCLK x 10
PLL Locked	X	PLLOUTA	X	X	X	1	0	1	1	REFCLK x 11
PLL Locked	X	PLLOUTA	X	X	X	1	1	0	0	REFCLK x 12
PLL Locked	X	PLLOUTA	X	X	X	1	1	0	1	REFCLK x 13
PLL Locked	X	PLLOUTA	X	X	X	1	1	1	0	REFCLK x 14
PLL Locked	X	PLLOUTA	X	X	X	1	1	1	1	REFCLK x 15

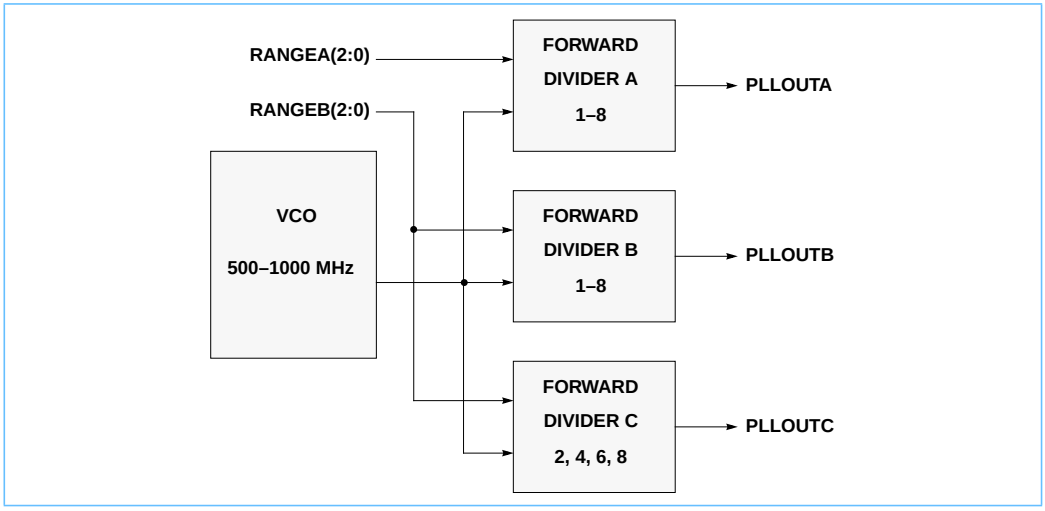
Table 125. PLL Functional Modes Truth Table: PLLOUTB, PLLOUTC (External-Divider=1)

Conditions (Normal Operation)	REFCLK	FBKCLK	RANGEAB			MULT				PLLOUTB Frequency	PLLOUTC Frequency
			2	1	0	3	2	1	0		
PLL Locked	X	PLLOUTB or C	0	0	0	X	X	X	X	65 MHz–125 MHz	65 MHz–125 MHz
PLL Locked	X	PLLOUTB	0	0	1	X	X	X	X	70 MHz–140 MHz	Logic ‘1’
PLL Locked	X	PLLOUTB or C	0	1	0	X	X	X	X	83 MHz–166 MHz	83 MHz–166 MHz
PLL Locked	X	PLLOUTB	0	1	1	X	X	X	X	100 MHz–200 MHz	Logic ‘1’
PLL Locked	X	PLLOUTB or C	1	0	0	X	X	X	X	125 MHz–250 MHz	125 MHz–250 MHz
PLL Locked	X	PLLOUTB	1	0	1	X	X	X	X	166 MHz–333 MHz	Logic ‘1’
PLL Locked	X	PLLOUTB or C	1	1	0	X	X	X	X	250 MHz–500 MHz	250 MHz–500 MHz
PLL Locked	X	PLLOUTB	1	1	1	X	X	X	X	500 MHz–1000 MHz	Logic ‘1’
PLL Locked	X	PLLOUTB or C	X	X	X	0	0	0	0	REFCLK x 16	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	0	0	1	REFCLK x 1	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	0	1	0	REFCLK x 2	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	0	1	1	REFCLK x 3	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	1	0	0	REFCLK x 4	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	1	0	1	REFCLK x 5	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	1	1	0	REFCLK x 6	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	0	1	1	1	REFCLK x 7	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	0	0	0	REFCLK x 8	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	0	0	1	REFCLK x 9	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	0	1	0	REFCLK x 10	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	0	1	1	REFCLK x 11	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	1	0	0	REFCLK x 12	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	1	0	1	REFCLK x 13	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	1	1	0	REFCLK x 14	PLLOUTB + 90°
PLL Locked	X	PLLOUTB or C	X	X	X	1	1	1	1	REFCLK x 15	PLLOUTB + 90°

PLL Internal Dividers

Since the PLLOUTA, PLLOUTB, and PLLOUTC outputs are programmed independently, several frequency ratios are possible among them. To understand this flexibility, consider the operation of the frequency dividers. Frequency dividers *Forward-Divider-A, Forward-Divider-B,* and *Forward-Divider-C* are driven from a common source, the voltage-controlled oscillator (VCO). The VCO is designed to operate between 500 MHz and 1000 MHz for all applications. The PLL output frequencies will be determined by the VCO frequency and the forward divider settings as programmed by the RANGEA(2:0) and the RANGEB(2:0) inputs. PLLOUTC is the same frequency as PLLOUTB for the 2, 4, 6, and 8 divide-by settings.

External dividers in the PLL feedback loop are allowed and are inserted between PLLOUT and FBKCLK. The existence of an external divider will affect the VCO frequency. All circuits in the PLL feedback must not be gated when the RESET=0. This is to prevent a VCO runaway condition initiated by a zero-frequency feedback clock.



To determine the VCO frequency, the feedback divider must be identified. The feedback divider truth table is shown in Table 130, “PLL Feedback Divider,” on page 297. If the FBKCLK input is derived from the PLLOUTA signal, then:

VCO frequency = REFCLK x Feedback-Divider x Forward-Divider-A x External-Divider

If PLLOUTB or PLLOUTC is the source of the FBKCLK input, then the same equation applies, except that *Forward-Divider-B* should be used. Assuming adherence to the functional mode truth tables, the resulting VCO frequency should be between 500 MHz and 1000 MHz.

With the wide range of programmability offered on the outputs, several integer and non-integer relationships can be realized between the PLLOUTA and PLLOUTB outputs by controlling the RANGEA(2:0) and RANGEB(2:0) inputs.

The frequency relationship is given as:

$$\frac{PLLOUTA}{PLLOUTB} = \frac{Divide-by-B}{Divide-by-A}$$

The PLLOUTA and PLLOUTB outputs will always be synchronized to the rising edge (that is, the PLLOUTA rising edge will coincide with the PLLOUTB rising edge at the start of the cycle). The rising edge of PLLOUTC will be delayed from the rising edge of PLLOUTB by 90˚. The divider truth tables are shown on page 295.

If phase alignment to the REFCLK is required, then the lowest frequency output should be used as the FBKCLK. As an example, assume REFCLK = 100 MHz, PLLOUTA = 200 MHz, and PLLOUTB = 100 MHz. If PLLOUTA is used as the source of the FBKCLK, then rising edge alignment of REFCLK to PLLOUTB will not be guaranteed. This is because two PLLOUTA edges in a single PLLOUTB period are possible candidates for phase lock with REFCLK as the PLL locks-in. In 50% of the cases, the PLL will lock to the rising edge of PLLOUTA that corresponds with the falling edge of PLLOUTB, and in 50% of the cases it will lock to the rising edge of PLLOUTA that corresponds with the rising edge of PLLOUTB. Hence rising edge alignment of REFCLK to PLLOUTB is not predictable. To avoid this situation, PLLOUTB should be used as the source of FBKCLK in which case PLLOUTB and PLLOUTA will always be rising edge aligned with REF-CLK.

As an example of the flexibility of the output relationships, assume that a relationship of PLLOUTA:PLLOUTB = 250 MHz:166.7 MHz is required. The feedback clock is derived from PLLOUTA and REFCLK = 125 MHz, so the multiplication factor (feedback divider) is 2. The determination of the RANGE inputs is calculated as follows:

1. Using the above equation along with "PLL Forward Divider A," Table 126 and "PLL Forward Dividers B and C," Table 127 to determine the available divider settings, there are two possibilities: *Divide-by-A = 4*, *Divide-by-B = 6*; and *Divide-by-A = 2*, *Divide-by-B = 3*.
2. Checking that the *Divide-by-A* settings do not violate the VCO frequency limits, the VCO output frequencies are calculated as 125 MHz x 2 x 4 = 1000 MHz, and 125 MHz x 2 x 2 = 500 MHz. Thus, both divider settings fall within the VCO range of 500 MHz–1000 MHz. (This is also done for the PLLOUTB frequency.)
3. Choosing the highest VCO frequency setting to minimize jitter, the forward divider settings are selected as *Divide-by-A = 4* and *Divide-by-B = 6*.
4. From the divider truth tables, the range settings are set to RANGEA(2:0) = ‘100’ and RANGEB(2:0) = ‘010’.

When PLLOUTB/PLLOUTC is not used, the *Divide-by-B* range bits should be set equal to the *Divide-by-A* range bits: RANGEB(2:0) = RANGEA(2:0).

Table 126. PLL Forward Divider A

RANGEA			Divide By	PLLOUTA Frequency
2	1	0		
0	0	0	8	65 MHz–125 MHz
0	0	1	7	70 MHz–140 MHz
0	1	0	6	83 MHz–166 MHz
0	1	1	5	100 MHz–200 MHz
1	0	0	4	125 MHz–250 MHz
1	0	1	3	166 MHz–333 MHz
1	1	0	2	250 MHz–500 MHz
1	1	1	1	500 MHz–1000 MHz

Table 127. PLL Forward Dividers B and C

RANGEB			Divide By	PLLOUTB Frequency	PLLOUTC Operation
2	1	0			
0	0	0	8	65 MHz–125 MHz	PLLOUTB + 90°
0	0	1	7	70 MHz–140 MHz	Logic ‘1’
0	1	0	6	83 MHz–166 MHz	PLLOUTB + 90°
0	1	1	5	100 MHz–200 MHz	Logic ‘1’
1	0	0	4	125 MHz–250 MHz	PLLOUTB + 90°
1	0	1	3	166 MHz–333 MHz	Logic ‘1’
1	1	0	2	250 MHz–500 MHz	PLLOUTB + 90°
1	1	1	1	500 MHz–1000 MHz	Logic ‘1’

If PLLOUTB and PLLOUTC are not used, then RANGEB(2:0) should be set to the same values as the RANGEA(2:0) inputs. PLLOUTC is only available on PLL7SFLIBE and PLL7SFLIBI.

Tuning Bit Settings

The PLL tuning bits, TUNE(9:0), are used to modify the PLL loop parameters by modifying the internal gains of the charge pumps. This external control allows the PLL to be stable over a wide range of frequencies and multiplication factors. Another benefit of the tuning bits is that they enable fine tuning of the PLL to compensate for either high levels of noise or input jitter. **It is strongly recommended that the tuning bit inputs be accessible and programmable in all designs.** Programmability will ensure proper PLL operation with no hardware impact should changes be required. At a minimum, TUNE(3:1) should be accessible and programmable.

The default values shown in Table 128 on 297 will allow the loop to be stable under all conditions and meet the jitter specifications. In some cases, jitter can be reduced further by modifying the TUNE(9:0) settings. In this fashion, the PLL becomes *tuned* to specific applications. For example, an application with a high amount of input jitter would be tuned differently than an application where the jitter is caused primarily by noise. Experimentation by measuring the impact that the tuning bits have on output jitter is the best

way to determine the optimal TUNE(9:0) settings. This measurement requires off-chip access to the PLL output clock. If a change of more than 1 LSB is desired, please contact your IBM representative.

Table 128. PLL Tuning Bit Recommended Default Settings

Product of Forward and Feedback Dividers (*M* = Fwd x Fbk)	Tune									
	9	8	7	6	5	4	3	2	1	0
2 ≤ M ≤ 3	0	1	—	0	1	1	0	0	1	1
3 < M ≤ 6	0	1	—	0	1	1	0	1	0	0
6 < M ≤ 10	0	1	—	0	1	1	1	0	0	0
10 < M ≤ 14	0	1	—	0	1	1	1	1	0	0
14 < M ≤ 40	1	0	—	0	1	1	1	1	1	0

Table 129. PLL Tuning Bit 7 Settings

VCO Frequency	Tune									
	9	8	7	6	5	4	3	2	1	0
500 MHz ≤ VCO Frequency ≤ 800 MHz	—	—	0	—	—	—	—	—	—	—
800 MHz < VCO Frequency ≤ 1000 MHz	—	—	1	—	—	—	—	—	—	—

Table 128 references a variable, *M*, to be used in determining the tuning bit settings. The value of *M* is determined from the product of the forward and feedback dividers in the loop. The truth tables for these dividers can be found in Table 126, “PLL Forward Divider A,” on page 295, Table 127, “PLL Forward Dividers B and C,” on page 296, and "PLL Feedback Divider," Table 130.

Table 130. PLL Feedback Divider

MULT				Divide By
3	2	1	0	
0	0	0	0	16
0	0	0	1	1
0	0	1	0	2

Table 130. PLL Feedback Divider (Continued)

MULT				Divide By
3	2	1	0	
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

As an example in calculating the default TUNE(9:0) settings, assume that the PLL is programmed to multiply a 100 MHz REFCLK by 4 to provide a 400 MHz PLLOUTA frequency (VCO = 800 MHz). In this case, RANGEA(2:0) ='110' (divide = 2), MULT(3:0) = '0100' (divide = 4), so *M* = 8 and the default setting is TUNE(9:0) = '0100101000'.

Spread-Spectrum Applications

Spread spectrum clock generation (SSCG) is becoming increasingly popular in applications where electromagnetic interference is a problem. In essence, a spread spectrum clock is simply a frequency modulated signal. By modulating the carrier frequency with a lower speed signal, the energy of the resultant clock is 'spread' across a frequency band. The amplitude of this energy is lower than it would be otherwise, thus reducing the EMI characteristics of the signal.

Several vendors offer SSCG modules. The designs are all similar in that they modulate

the output clock at a frequency between 30 kHz–60 kHz with programmable modulation amplitude, or spread. For instance, a part may allow the spread to be either 0.5% or 1% of the carrier frequency. With a 1% spread on a 100 MHz clock, the output clock will modulate between 99 MHz–101 MHz at a frequency of 30 kHz.

Another way of looking at SSCG is that it creates a controllable amount of long-term jitter or drift. In order for a receiving PLL to operate in this environment, it must be able to accurately track the input clock drift. The SSCG vendors recommend that the downstream PLLs from the spread clock have bandwidths of 4 MHz or greater. In general, PLLs with loop bandwidths below this specification will filter the modulating input. PLLs with loop bandwidths above this spec will track the modulating input.

The accuracy to which the SA-27E PLLs can track the input clock modulation is defined as tracking skew. Tracking skew is a function of PLL programming, SSCG modulation frequency, and SSCG modulation amplitude. When performing system timing analysis, the tracking skew must be added to the input-output jitter and static-phase-error to determine maximum deviation of the PLL output clock with respect to the reference clock.

The PLL tracking skew will vary over a range of 50 ps–1 ns depending on the application. Contact your IBM representative for more information on SSCG tracking skew.

RESET Operation

The PLL requires a reset operation to initialize internal circuits and the RESET input pin is provided for this purpose. When RESET is asserted (logic ‘1’) the PLL is in a bypass mode where PLLOUTA/PLLOUTB/PLLOUTC are buffered versions of REFCLK. Once RESET is de-asserted (logic ‘0’) the PLL switches from bypass mode to functional mode. During this switch, it is possible that the PLL output may glitch as the VCO output is switched in. The PLL output clocks immediately after the switch will be operating at very low frequencies. As the PLL begins it lock-in behavior, the output clocks will slowly increase in frequency until they are near the target frequency. The output clock phase is then adjusted slightly until phase alignment and frequency lock are achieved between REFCLK and FBKCLK. This will occur in less than 100 µs after RESET is de-asserted.

Due to the unpredictable nature of the PLL’s operation during the lock-in period, usage of the PLLOUT signals is not recommended until the PLL lock-in time has elapsed. Only at this time are the frequency and phase of the PLL outputs valid.

PLL Electrical Specifications

Table 131. PLL Electrical Specifications

Standard voltage supply	1.65–1.95 volts (PLL7SFLIBE/PLL7SFLIBI)
Dual voltage digital supply (AVDD = 1.65–1.95 V)	1.40–1.60 volts (PLL7SFLIBEDV/PLL7SFLIBIDV)
Temperature range	-40°C to 125°C
Synchronizing edge	Rising
Multiplication factor	x1 through x16
Static phase error	± 100 ps maximum
Insertion delay	8 ns (from PLLOUT to FBKCLK) maximum
Lock time	100 µs maximum
Power dissipation	30 mW typical 50 mW maximum
PLLOUTA, PLLOUTB, PLLOUTC	
Frequency ranges (programmable)	65 MHz–1000 MHz
Duty ratio	48%–52% (65 MHz–500 MHz) maximum 45%–55% (500 MHz–1000 MHz) maximum
Phase jitter	± 100 ps (cycle-cycle) maximum ± 200 ps (input-output) maximum
PLLOUTB skew with respect to PLLOUTA	± 50 ps maximum
PLLOUTC skew with respect to PLLOUTB	90° ± 100 ps maximum (PLL7SFLIBE/PLL7SFLIBI)
REFCLK	
Frequency	33 MHz–490 MHz
Pulse width (positive or negative)	600 ps minimum
Voltage levels (external REFCLK)	LVTTL, MPDL = 0.8V. LPUL = 2.0V Maximum input = 3.8V
Slew rate (external REFCLK)	2V/ns minimum (through 0.8–2.0 volts)
Rise time (internal REFCLK)	500 ps maximum
Phase jitter	± 150 ps (cycle-to-cycle) maximum
FBKCLK	
Frequency	33 MHz–1000 MHz
Pulse width (positive or negative)	400 ps minimum
Rise time	500 ps maximum

PLL Pin Descriptions

This section describes the normal and test mode requirements for each PLL input and output pin. In the descriptions that follow, “primary” refers to a signal that is available at a chip I/O. “AC test” refers to a signal that is located in one of the 64 full-function test I/O slots. “DC test” refers to a signal that is located in one of the 56 limited function test I/O slots.

REFCLK

Description: Required AC test input
Suggested Name: PLL_REFCLK
Nontest Value: Clock
Test Value: Clock

This is the reference clock to which the feedback clock will be aligned. The rising edge is used for alignment. To maintain the static phase-error specification, restrictions are placed on the slope of the rising edge. Refer to Table 131, “PLL Electrical Specifications,” on page 300 for specifications. The REFCLK frequency must be stable before the PLL can begin to lock. Changes in the REFCLK frequency after lock is established can result in the PLL becoming unlocked. When using PLL7SFLIBE or PLL7SFLIBEDV, REFCLK connects directly to a chip pad. When using PLL7SFLIBI or PLL7SFLIBIDV, REFCLK typically connects to the output of a receiver. Any receiver in the library can be used (differential or single-ended) provided that it is located in a test I/O slot. The minimum REFCLK frequency is 33 MHz. The maximum REFCLK frequency is 490 MHz.

During LSSD test, REFCLK is buffered through the PLL to the PLLOUTA, PLLOUTB, and PLLOUTC outputs. During PLL functional test mode, REFCLK must be controllable from an AC test I/O slot.

FBKCLK

Description: Required input
Suggested Name: PLL_FBKCLK
Nontest Value: Clock
Test Value: Logic ‘X’

This is the feedback clock to the PLL that will be aligned with the reference clock. As is the case with REFCLK, some restrictions are necessary on the rising-edge transition rate to maintain the static phase-error specification. The insertion delay (defined as the time from PLLOUT to FBKCLK) must be kept below 8 ns. The path from PLLOUT to FBKCLK must be enabled (no gating) prior to RESET being de-asserted.

During LSSD test, FBKCLK is buffered through the PLL to the OBSERVE(0) output. During PLL functional test, FBKCLK is not used.

RANGE and MULT

Description: Required inputs
Suggested Name: PLL_RANGE, PLL_MULT
Nontest Value: Programmable
Test Value: Logic ‘X’

These programmable inputs are used to choose the output frequency of the PLL. They can be sourced from receivers, internal pull-up or pull-down cells, flip-flops, or logic. The logic state of these inputs must be stable before the PLL can begin to lock. Refer to Table 124, “PLL Functional Modes Truth Table: PLLOUTA (External-Divider=1),” on page 291 and Table 125, “PLL Functional Modes Truth Table: PLLOUTB, PLLOUTC (External-Divider=1),” on page 292 for the operation of these pins. If PLL-OUTB and PLLOUTC are not used, then RANGEB should be set to the same value as RANGEA.

During LSSD test, the RANGE and MULT inputs are buffered through the PLL to the OBSERVE(10:1) outputs. During PLL functional test, the RANGE and MULT inputs are not used.

TUNE (9:0)

Description: Required inputs
Suggested Name: PLL_TUNE
Nontest Value: Programmable
Test Value: Logic ‘X’

These programmable inputs are used to optimize the PLL stability and jitter. They can be sourced from receivers, registers, or logic. The logic state of these inputs must be stable before the PLL can begin to lock. Table 128, “PLL Tuning Bit Recommended Default Settings,” on page 297 and Table 129, “PLL Tuning Bit 7 Settings,” on page 297 define the recommended logic levels for these inputs. **It is strongly recommended that the tuning bit inputs be accessible and programmable in all designs.** At a minimum, TUNE(3:1) should be accessible and programmable. If controlled by on-chip registers, the registers must **NOT** be clocked from a signal that is derived from PLLOUTA, PLLOUTB, or PLLOUTC. BUFREFCLK can be used instead.

During LSSD test, the TUNE inputs are buffered through the PLL to the OBSERVE(20:11) outputs. During PLL functional test, the TUNE inputs are not used.

RESET

Description: Required input
Suggested Name: PLL_RESET
Nontest Value: Pulse
Test Value: Logic ‘X’

The RESET signal serves three purposes. First, it holds the PLL in a reset state by forcing the VCO to operate at its minimum frequency. Second, it puts the PLL in bypass mode so that PLLOUTA, B, C will be buffered versions of REFCLK. Third, it initializes the phase alignment of PLLOUTA/PLLOUTB/PLLOUTC. RESET should be held active (high) during power-on until *all* of the following condition are met:

1. All PLL inputs are stable and at their final values.
2. REFCLK is stable at or below the target frequency.
3. Any gating in the feedback path is removed.
4. AVDD and V_{dd} are at their final values.

Failure to hold the PLL in reset (RESET = high) during power-on can result in *VCO run-away*. In this mode, output clocks are not present and the PLL can be recovered only by pulsing the RESET or AVDD pins. A reset is also required should **any** of the PLL inputs change after power-on. The minimum pulse width of RESET is 100 ns.

During LSSD test, RESET is buffered through the PLL to the OBSERVE(21) output. During PLL functional test, RESET must be controllable and held high.

TESTIN

Description: Required AC test input
Suggested Name: PLL_TESTIN
Nontest Value: Logic ‘0’
Test Value: Logic ‘1’

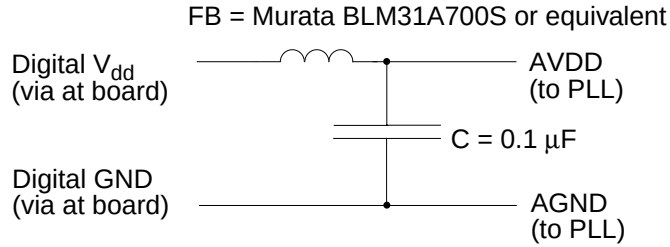
The TESTIN input is used to program the PLL to perform parametric testing at the wafer and module level. It needs to be driven from a receiver that occupies one of the 64 test I/Os. It is possible that the receiver output can be shared with another function, but TESTIN must be kept low during normal PLL operation.

During LSSD test, TESTIN is ORed with AVDD and is sent to the OBSERVE(22) output. During PLL functional test, TESTIN must be controllable from an AC test I/O slot.

AVDD, AGND

Description: Required DC test inputs
Suggested Name: PLL_AVDD, PLL_AGND
Nontest Value: Power supply
Test Value: Power supply

AVDD and AGND are the voltage supply pins to the analog circuits in the PLL. AVDD must be in range of **1.65–1.95 volts** for both the standard and low-voltage PLLs. Noise on these signals will cause phase jitter at the output of the PLL. To provide isolation from the noisy internal digital V_{dd} and GND signals, AVDD and AGND are brought to package pins. If little noise is expected at the board level, then AVDD can be connected directly to the digital V_{dd} plane. In most circumstances, however, it is prudent to place a filter circuit on AVDD as shown below. AGND should be brought out from the package and connected to the digital GND plane at the AVDD capacitor. All wire lengths should be kept as short as possible to minimize coupling from other signals.



The impedance of the ferrite bead should be much greater than that of the capacitor at frequencies where noise is expected. Some applications have found that a resistor instead of a ferrite bead does a better job of reducing jitter. The resistor should be kept to a value lower than 2 Ω . Circuit simulation and experimentation is the best way to determine the optimal filter design for a specific application.

On the die, AVDD and AGND can connect directly to fat-wire I/O cells (AINSD_PM_A) or a voltage regulator, all of which must reside in IODCTEST slots.

During LSSD test, AVDD is held to logic ‘0’, is ORed with TESTIN, and is sent to the OBSERVE(22) output. During PLL functional test, AVDD is held to logic ‘1’ and must be controllable from a DC test I/O slot. AGND is held to logic ‘0’ at all times.

PLLOUTA, PLLOUTB, PLLOUTC

Description: One required output, others are optional outputs
Suggested Name: PLL_PLLOUT
Nontest Value: Clock
Test Value: Clock

These signals are the PLL clock outputs that will typically drive the base of a clock tree. Only one of the three PLL outputs is required to be connected within the chip. The maximum capacitive loading is dependent on the electromigration characteristics of the wire connected to the PLL output pins. The PLL outputs support both single and double-wide wires. When PLL outputs are not in use, they should be set to the same frequency as the PLL output in use (RANGEB = RANGEA). If jitter measurements are desired, then one of these outputs should be viewable at a chip pin. If REFCLK stops switching, then PLLOUTA/B/C will either slow down to a very low frequency or stop oscillating. PLLOUTC is only available on PLL7SFLIBE and PLL7SFLIBI. Under worst case conditions, the PLLOUT signals can still drive a 1pF load with 0.2ns slew rates.

The rising edge of PLLOUTB is phase aligned with the rising edge of PLLOUTA. When active, the rising edge of PLLOUTC is delayed by 90˚ from the rising edge of PLLOUTB. A RESET pulse is required to initialize these output phase relationships. When alignment of both PLLOUTA and PLLOUTB to REFCLK is desired, the lowest frequency output clock should be used as the source for FBKCLK.

During LSSD test, PLLOUTA/B/C are buffered outputs of the REFCLK input. During PLL functional test, PLLOUTA/B/C do not need to be monitored.

BUFREFCLK

Description: Optional output
Suggested Name: PLL_BUFREFCLK
Nontest Value: Clock
Test Value: Clock

This signal is a buffered version of the REFCLK input to the PLL. Its use is optional, but is available for applications that need the REFCLK signal for other functions.

During LSSD test, BUFREFCLK is a buffered output of the REFCLK input. During PLL functional test, BUFREFCLK does not need to be monitored.

PLLLOCK

Description: Required AC test output
Suggested Name: PLL_PLLLOCK
Nontest Value: Logic ‘1’
Test Value: Logic ‘0’

PLLLOCK should be used only for manufacturing test. This signal indicates when the FBKCLK input is close to alignment with the REFCLK input. While RESET is high (reset), PLLLOCK will be low. Following reset, PLLLOCK will stay low until lock is achieved. The PLLLOCK signal will go high less than 100 μs after:

1. The REFCLK signal is stabilized at a constant frequency.
2. The FBKCLK input is derived from PLLOUT.
3. The RANGE and MULT inputs are at their final states.
4. The AVDD input is at the rail.

PLLLOCK will return to a low state if the PLL loses lock with the reference clock.

During LSSD test, PLLLOCK is at logic ‘0’. During PLL functional test, the PLLLOCK output must be monitored by the tester to verify the PLL lock operation. PLLLOCK must be connected to a driver that occupies one of the 64 AC test I/O slots. The PLLLOCK signal can be multiplexed with another function so that an additional I/O is not required.

OBSERVE(0)

Description: Required output
Suggested Name: PLL_OBSERVE
Nontest Value: Logic ‘0’
Test Value: FBKCLK

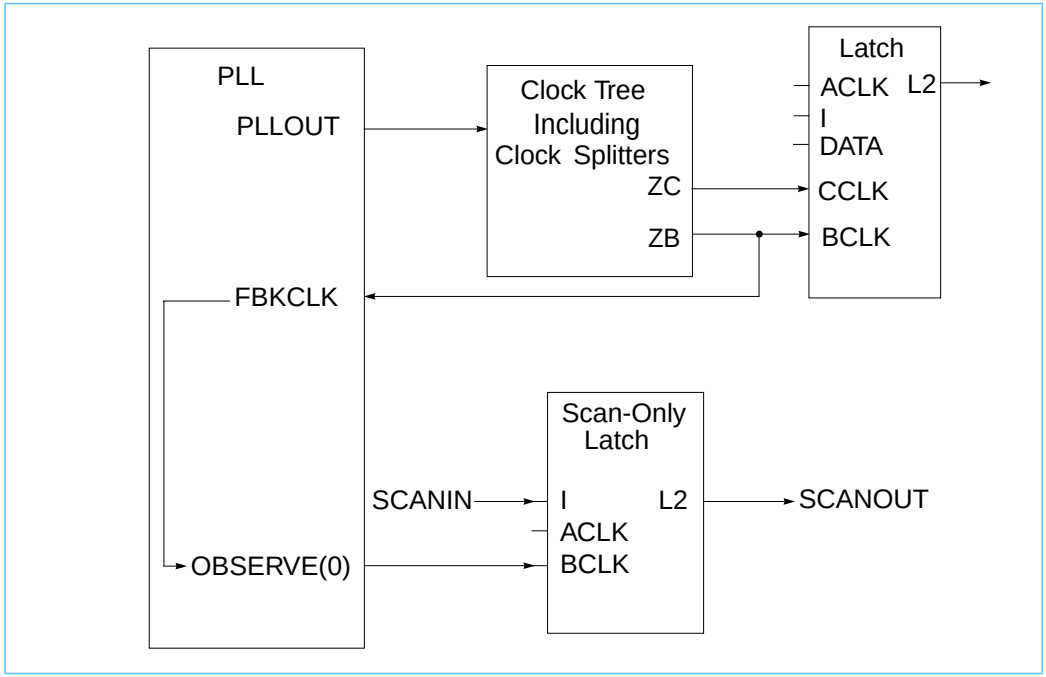
During normal operation, OBSERVE(0) is at logic ‘0’.

For LSSD test, OBSERVE(0) must be connected to a flip-flop in the scan chain to assure complete PLL test coverage. The OBSERVE(0) signal is the output of a buffer fed by FBKCLK. Since FBKCLK does not get tested during the PLL functional test at wafer and module test, it is necessary to test it during LSSD test. Since the FBKCLK is usually a clock function, the OBSERVE(0) pin should be connected to the appropriate clock input of a scan-only latch in the scan chain as shown in Figure 65 on page 308.

However, if the clock splitter is not included in the feedback path, then the OBSERVE(0) output should be connected to the data input of a latch in the scan chain, as shown in Figure 66 on page 309.

During PLL functional test, OBSERVE(0) does not need to be monitored.

Figure 65. PLL OBSERVE(0) Usage



OBSERVE (22:1)

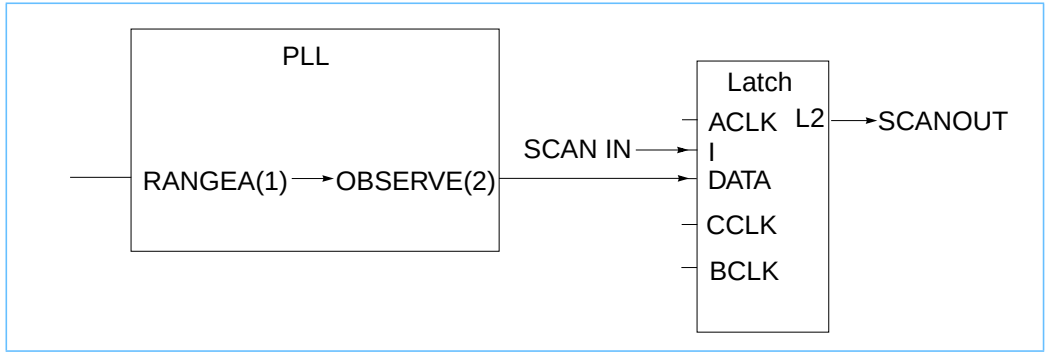
Description: Required outputs
Suggested Name: PLL_OBSERVE
Nontest Value: RANGE, MULT, TUNE, TESTIN, AVDD
Test Value: RANGE, MULT, TUNE, TESTIN, AVDD

Like OBSERVE(0), these outputs are not usually used in normal operation but should be connected to assure complete test coverage. They are buffered versions of the

RANGE, MULT, TUNE, TESTIN, and AVDD inputs. OBSERVE(22:1) should be connected to the data inputs of latches in the scan chain. A typical connection is shown in Figure 66.

During PLL functional test, OBSERVE(22:1) do not need to be monitored.

Figure 66. PLL OBSERVE(22:1) Usage



TESTOUT

Description: Required AC test output
Suggested Name: PLL_TESTOUT
Nontest Value: Logic ‘0’
Test Value: Clock

During normal operation, TESTOUT is at logic ‘0’.

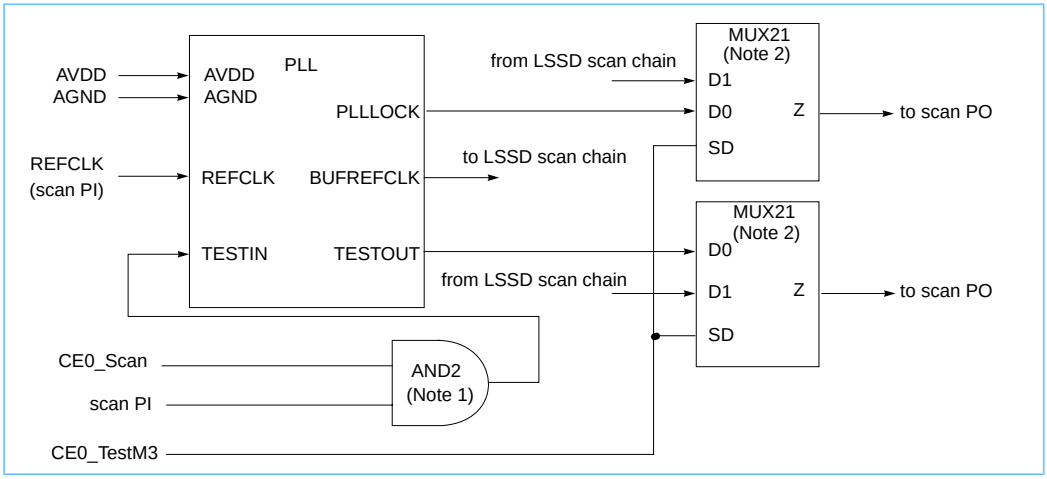
During LSSD test, TESTOUT is at logic ‘0’.

During PLL functional test, the TESTOUT output must be monitored by the tester to verify the PLL output frequency. The maximum frequency at the TESTOUT pin will be 15 MHz. Like PLLLOCK, the TESTOUT signal must be connected to a driver that occupies one of the 64 AC test I/O slots. TESTOUT can be multiplexed with another function so that an additional I/O is not required. TESTOUT is low during LSSD mode.

Recommended PLL Test Pin Connections

The recommended connections for REFCLK, BUFREFCLK, TESTIN, PLLLOCK, and TESTOUT are shown Figure 67. REFCLK is used as a scan data input pin; scan data is propagated through the BUFREFCLK pin to an LSSD scan chain. PLLLOCK and TESTOUT are observable at output pins that also serve as LSSD scan data output pins. Note that scan data output pins can be shared with system-functional input, output, or bidirectional signals. Contact your IBM representative for more information on pin sharing.

Figure 67. PLL Test Signal Usage



Notes:

1. If using IBM's pad ring insertion tool, IOSpecDFT (version 5), the AND gate can be automatically inserted into the design by specifying MT_in=<PLL_TESTIN_NetName> and comp_enab=0 in the IOSpecList record for the scan PI. The gating signal is identified in the IOSpecList using the test_use=SI keyword. If using IOSpecDFT version 4, the AND gate must be manually instantiated in the design (or in the connections file).
2. If using IOSpecDFT version 5, the MUXes can be automatically inserted into the design by specifying MT_out=<PLL_output_NetName> in the IOSpecList record for the scan PO. The mux control signal is identified in the IOSpecList using the test_use=M3 keyword. If using IOSpecDFT version 4, the MUXes must be manually instantiated in the design (or in the connections file).

Observability of the PLL outputs and control of the PLL TESTIN pin is provided by chip-level test signals CE0_Scan and CE0_TestM3. CE0_Scan is also used to enable all LSSD scan data paths and scan clocks. CE0_TestM3 is also used as the signal controlling the TESTM3 pins of any SRAM BIST macro.

Table 132. Test Signal Attributes

Signal	Test Attribute
CE0_Scan	TB_KFLAG = +SG
CE0_TestM3	TB_KFLAG = +SG, TB_WRP_DC = +TI
REFCLK, scan PI	TB_KFLAG = SI, TB_OFLAG = BDY
Scanout POs	TB_KFLAG = SO, TB_OFLAG = BDY

Physical Placement

This section describes the details concerning the PLL placement on the chip.

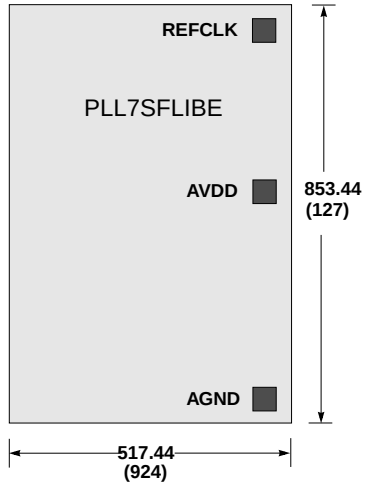
PLL7SFLIBE and PLL7SFLIBEDV

PLL7SFLIBE and PLL7SFLIBEDV are rectangular cores utilizing three I/Os. They occupy 117,348 and 125,552 cells respectively and use metallization up to Metal-3. No porosity is provided on Metal-3, but all levels above are open.

When used on flip-chip area array I/O dies, the three PLL I/O connections are realized by placing the PLL directly under the two corresponding pads for AVDD and AGND, and letting the wire router via straight up with no lateral wiring. Select the REFCLK C4 near the PLL to keep lateral wiring short. By using direct C4 vias and short lateral wiring, the jitter and static phase error will be minimized.

When used on peripheral I/O dies, the three PLL I/O connections are realized by utilizing special fat-wire receiver cells and global wiring. Lateral wiring on AVDD, AGND, and REFCLK should be minimized to reduce the jitter and static phase error.

Figure 68. PLL7SFLIBE and PLL7SFLIBEDV Size



PLL7SFLIBE

Internal area = 117,348 cells
(924 x 127)

0.442 mm^2 wafer

PLL7SFLIBEDV

Internal area = 125,552 cells
(924 x 133)

0.472 mm^2 wafer

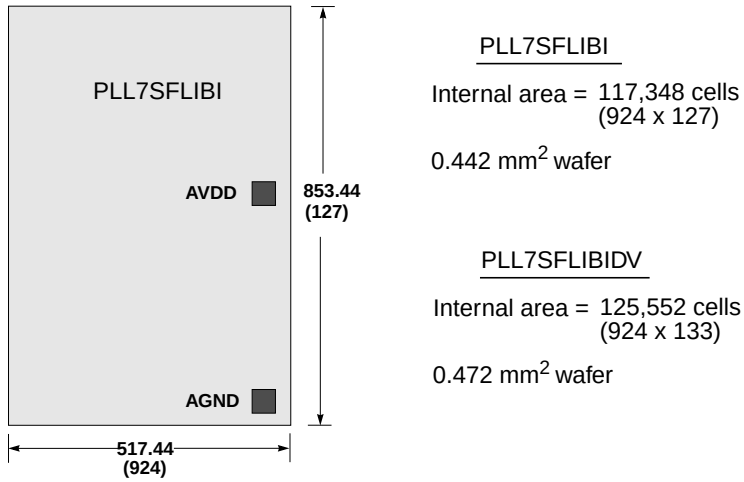
PLL7SFLIBI and PLL7SFLIBIDV

PLL7SFLIBI and PLL7SFLIBIDV are rectangular cores utilizing two I/Os. They occupy an area of 117,348 cells and 125,552 cells respectively and use metallization up to Metal-3. No porosity is provided on Metal-3, but all levels above are open.

When used on area array I/O dies, the two PLL I/O connections are realized by placing the PLL directly under the two corresponding pads for AVDD and AGND, and letting the wire router via straight up with no lateral wiring. By using direct C4 vias, the jitter will be minimized.

When used on peripheral I/O dies, the two PLL I/O connections are realized by utilizing special fat-wire receiver cells and global wiring. Lateral wiring on AVDD and AGND should be minimized to reduce the jitter and static phase error.

Figure 69. PLL7SFLIBI and PLL7SFLIBIDV Size



Placement Restrictions: Flip-Chip Area Array I/O Dies

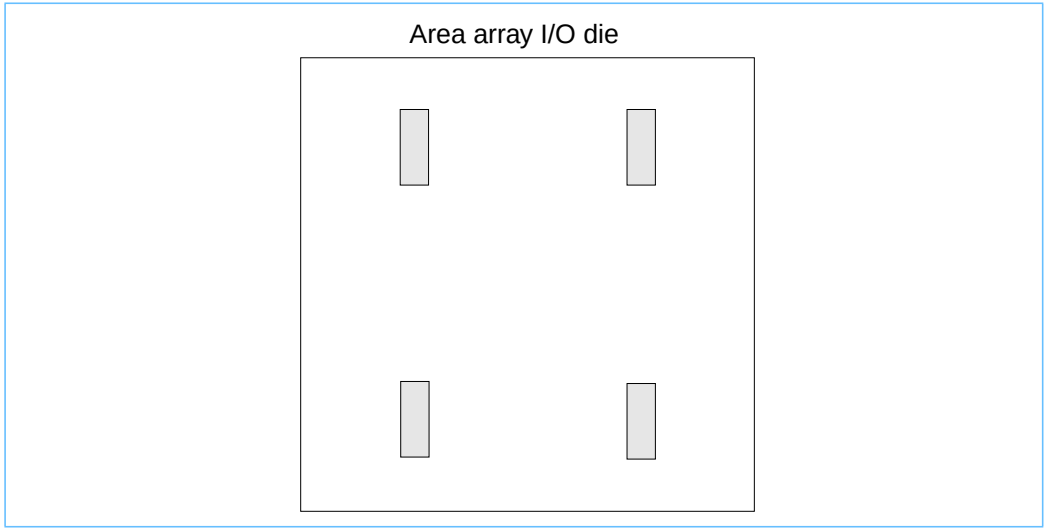
There are four required PLL placements per die. The advantages of using the required placements are listed below:

1. In a *required placement,* the AVDD and AGND pins will via directly to their corresponding DC test C4s with no lateral wiring. Lateral wiring can increase jitter by exposing the signals to coupled noise from other on-chip nets. REFCLK should be routed to the nearest AC test C4.
2. In a *required placement,* the AVDD and AGND pins are shielded in the package by adjacent ground traces to minimize noise coupling from other package nets. Furthermore, all attempts are made to route the AVDD and AGND nets to outside package rows, thus reducing the risk of noise coupling on the card between the package pins and the AVDD/AGND filter.

The four required placements are approximately shown in Figure 70 on page 314. PLL rotation (180˚) and mirroring are allowed for floorplanning flexibility.

PLLs that are not put in the required placements must be reviewed with an IBM representative. In most cases an increased jitter specification will be the result.

Figure 70. PLL Placement Example on SA-27E Flip-Chip Area Array I/O Die

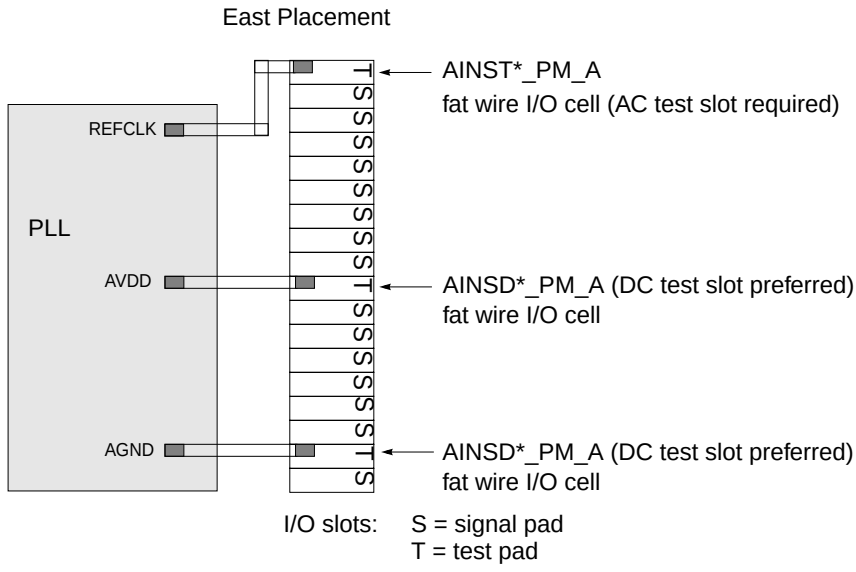


Placement Restrictions: Flip-Chip Peripheral I/O Dies

There are four required PLL placements per die. There are two on the east side and two on the west side of the die. Special fat wire I/O cells must be used to connect the PLL's AVDD, AGND, and REFCLK signals to the chip pins. The lateral fat wire lengths should be minimized by placing the PLLs directly next to the corresponding fat wire I/O cells. These must reside in test I/O slots. Keeping these wire lengths short will reduce jitter and static phase error.

PLLs that are not put in the required placements must be reviewed with an IBM representative. In most cases an increased jitter specification will be the result.

Figure 71. PLL Placement Example on SA-27E Flip-Chip Peripheral I/O Die



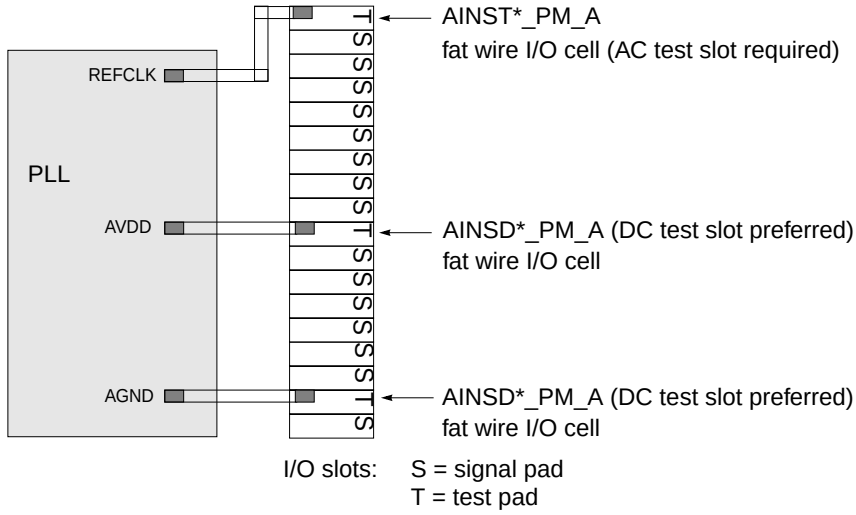
Note: See “Generic Fat Wire I/Os” on page 323 for more information.

Placement Restrictions: Wire Bond Peripheral I/O Dies

There are no absolute placement restrictions with the SA-27E PLLs when used on wire bond peripheral I/O dies. They can be placed anywhere along the east or west edges of the chip and lateral fat wires can be used to connect the AVDD, AGND, and REFCLK pins. Follow the guidelines below when determining the PLL placements:

1. The PLLs can be placed on either the east or west edges of the chip.
2. The lateral fat wire lengths should be minimized by placing the PLLs directly next to the corresponding fat wire I/O cells. These must reside in test I/O slots. Keeping these wire lengths short will reduce jitter and static phase error.
3. Since the wire bond packages provide no shielding for AVDD and AGND, only non-switching signals should be used in the I/O slots adjacent to the AVDD and AGND slots. A review of the wiring from the I/O slots to the package pins must be performed to ensure that no switching nets are adjacent to the AVDD and AGND signals as they route through the package.

Figure 72. PLL Placement Example on SA-27E Wire Bond Peripheral I/O Die



Note: See “Generic Fat Wire I/Os” on page 323 for more information.

Static Phase Error and Phase Jitter Definitions

As a phase synchronizer, the PLL will align the rising edges of the REFCLK and the FBKCLK. The accuracy to which the PLL can perform this alignment is defined in the static phase error and phase jitter specifications found in Table 131, “PLL Electrical Specifications,” on page 300.

Static phase error is a fixed skew between the rising edges of the synchronized signals (REFCLK and FBKCLK). It does not change on a cycle-to-cycle basis. It is caused by:

1. Differences in the rising edge rates of the two input signals
2. Differences in the path delays from the receivers to the phase/frequency detector inside the PLL
3. Process, voltage, and temperature variations

Phase jitter is a random variation of the output signal's phase. It is caused primarily by AVDD and substrate noise perturbing the voltage-controlled oscillator (VCO) within the

PLL. It can also be caused by excessive jitter on the REFCLK input. Phase jitter is defined in three ways: cycle-cycle, input-output, and long-term jitter.

Cycle-Cycle Jitter

This specification refers to the *deviation from ideal* between the PLLOUT rising edge and the subsequent PLLOUT rising edge. The cycle-cycle jitter specification is ± 100 ps.

Input-Output Jitter

This specification refers to the *deviation from ideal* between the FBKCLK rising edge and the corresponding REFCLK rising edge (not including the static phase error). The input-output jitter specification is ± 200 ps.

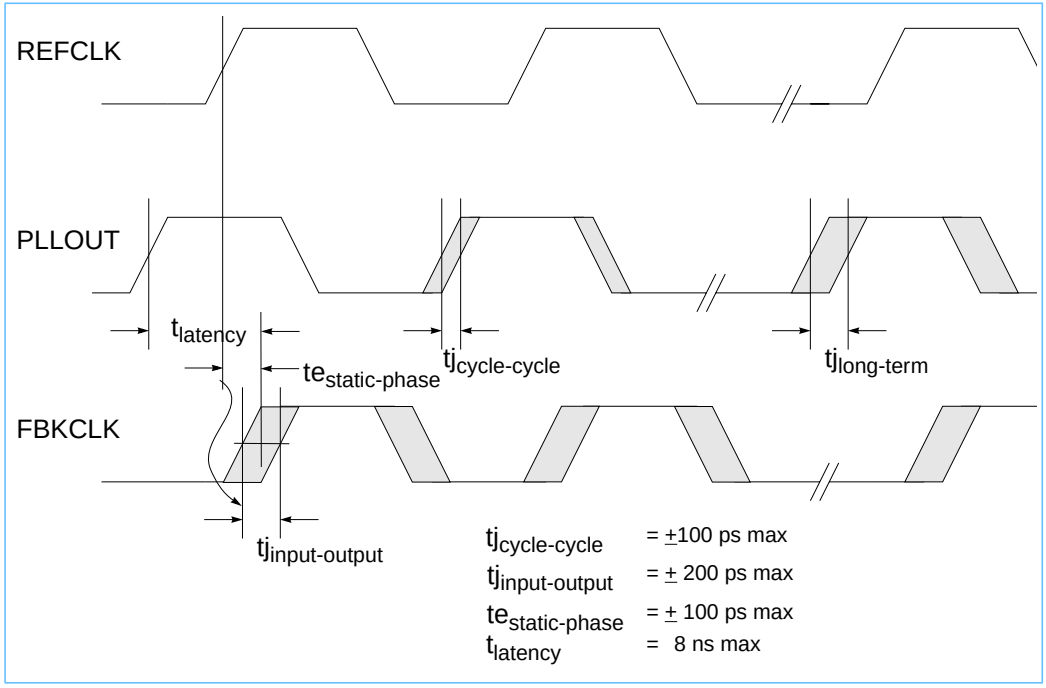
Long-Term Jitter

This specification refers to the *deviation from ideal* between the PLLOUT rising edge and a subsequent PLLOUT rising edge, usually several thousand clocks later. The long-term jitter is not specified for this PLL. The value will be similar to the input-output jitter specification when the input clock does not exhibit any long-term drift.

Chip-to-chip timings are affected by static phase error and input-output phase jitter. These parameters represent the uncertainty of where the internal clock edge will occur with respect to the REFCLK. Static phase error is added to input-output phase jitter to determine the phase difference of the internal clock. In this case, the FBKCLK can be offset by ± 300 ps from the REFCLK.

Internal flip-flop to flip-flop timings are not affected by static phase error or input-output phase jitter, but will be affected by cycle-cycle phase jitter. This is due to the clock period changing slightly from one clock to the next. The PLL cycle-cycle phase jitter is ± 100 ps. A timing diagram is shown in Figure 73 on page 318.

Figure 73. PLL Phase Error and Jitter



Phase Jitter Measurement

The PLL phase jitter specifications are based on hardware measurements on a test chip. The measurement technique can have a significant bearing on the final jitter results. The technique used in the IBM Microelectronics ASICs laboratory is meant to represent a typical operating environment (that is, significant internal and I/O switching activity). The actual jitter measured in other designs can vary based on measurement techniques and V_{dd}/GND noise.

Care must be taken when measuring jitter to assure that spurious noise events in the test setup and equipment do not affect the PLL jitter measurement. Additionally, jitter from the reference clock must be taken into account when determining the jitter contribution of the PLL.

To measure cycle-cycle jitter, the output clock is used to trigger a digitizing oscilloscope, and 10,000 samples are taken of the first edge of the output clock after the trigger. The endpoints of the resulting histogram are used to define the peak-to-peak jitter (for example, 150 ps peak-to-peak jitter = ± 75 ps jitter).

The technique used for measuring input-output jitter is to trigger the oscilloscope with the reference clock and obtain 10,000 samples of the output clock edge. The resulting input-output jitter indicates how far the internal clock will deviate from the reference clock. Again, the endpoints of the resulting histogram are used to define the peak-to-peak jitter.

The technique for measuring long-term jitter is similar to that used for the cycle-cycle jitter measurement. The trigger is the same, but the measured output clock is 10,000 cycles delayed from the trigger. A low-jitter reference clock is required for this measurement since drift on the reference clock will manifest itself as increased long-term jitter. The long-term jitter will be very similar to the input-output jitter when the reference clock does not drift.

PLL Restrictions/Guidelines

Stability

To assure proper operation, care must be taken when imbedding the PLL into a design. The PLL comprises a linear feedback system whose stability is assured only under certain conditions. Restrictions on the ‘open-loop’ parameters are necessary for maintaining adequate phase margin.

Phase margin is a measure of the stability of a linear feedback system. A precise definition can be found in most texts that deal with this topic. Most variables that affect the phase margin are controlled within the PLL; however, two are under the user's control. They are:

- Insertion delay
- External dividers

To assure stability for all potential applications, a maximum insertion delay is specified. This delay should not be exceeded without approval from IBM Microelectronics ASICs.

External dividers in the PLL loop are allowed provided that the TUNE (9:0) bits are properly reprogrammed. Since an external divider represents a third divider in the loop, its divide value must be multiplied by the product of the forward and feedback dividers when determining the tuning bit values (in Table 128, “PLL Tuning Bit Recommended Default Settings,” on page 297, M = Fwd × Fbk × External).

False Unlock Indications

The primary purpose of the PLLLOCK signal is to enable PLL functional testing during manufacturing.The lock indicator circuit is designed to detect a PLL locked condition when the REFCLK maintains a defined phase relationship with the FBKCLK over time. If this phase difference is outside the lock indicator limits, then the PLLLOCK signal will go low. This situation can be inadvertently caused by excessive input jitter (REFCLK phase not stable) or excessive output jitter caused by noise (FBKCLK phase not stable). Since the magnitudes of these two variables are not usually known until late in the design cycle, any use of the PLLLOCK signal should include a contingency for the case where PLLLOCK indicates an unlocked condition while the PLL is still operating within specifications.

The PLL will require 100 µs to lock following PLL reset. Instead of using the PLLLOCK signal to indicate that lock is complete, a 100 µs counter is recommended. The BUFREFCLK output can be used to clock this counter since it will be stable whenever REFCLK is stable.

Guidelines to Minimize Jitter

Under normal circumstances, the PLL will meet the advertised jitter specifications. There are other measures that should be taken to minimize jitter. They are:

- Minimize noise on the AVDD signal by adding an external filter as described on page 305. Verify through simulation that it will be effective at filtering out both the high and low frequency noise sources expected in the system. The PLL is most sensitive to noise near its loop bandwidth which varies between 200 kHz- 10 MHz. Noise on the AVDD and AGND signals should be kept to less than 200mV.
- Do not place noisy or fast off-chip drivers near the PLL. Noise at the PLL’s power ring on V_{dd} and GND must be kept below 200 mV.

- Use the I/O slots near the PLL for quiet signals, test-only signals, or programmable V_{dd}/GND cells. If unused I/Os are available, use them as programmable grounds to buffer the PLL on each side from other I/Os.
- Do not allow overshoot/undershoot on drivers or receivers near the PLL.
- Do not place potentially noisy internal circuits near the PLL internal circuits. In general, higher frequency signals generate more noise than lower frequency signals. Also, high-power level cells create more noise than low-power level cells. Keep compilable RAMs and register arrays away from the PLL, if possible.
- Create “dead” space of at least 100 µm between the PLL and all other circuits. Physical space is a good way to reduce noise transmission through the chip substrate.
- Provide a low-jitter REFCLK signal. The maximum input jitter is ± 150 ps cycle-to-cycle. At higher magnitudes of input jitter, the output jitter will increase. The modulation frequency of the input jitter should be lower than 100 kHz (to allow the PLL to track it) or higher than 20 MHz (to allow the PLL to filter it). Eliminate overshoot/undershoot by proper termination.
- Minimize on-card V_{dd} and ground noise by using adequate chip decoupling capacitors for high and low frequency noise.
- Operate the VCO as close to the top of its range as possible. The maximum VCO frequency is 800 MHz or 1000 MHz depending on the TUNE(7) setting. For example, if the PLL target output frequency is 166 MHz, use the 83 MHz–166 MHz range instead of the 166 MHz–333 MHz range.
- If PLLOUTB and PLLOUTC are not used, then RANGEB(2:0) should be set to the same value as RANGEA(2:0).
- The AVDD signals must have dedicated filters. Experimentation has shown severe PLL degradation when AVDD signals are shared between PLLs.
- Allow programmability of the TUNE(9:0) inputs to the PLL through chip pins or programmable registers. This will enable fine-tuning of the PLL loop parameters to minimize jitter if necessary. The PLL output should be accessible at a chip pin to monitor the jitter.

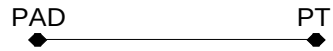
References

For details about the architecture and circuits used in this PLL design, refer to the 1995 *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp.112–113, the *IEEE Journal of Solid-State Circuits*, Nov. 1995, pp. 1259–1266, and the following United States Patents: 5,495,207; 5,513,225; 5,525,932; 5,541,442; 5,546,052; 5,619,161.

Generic Fat Wire I/Os

Cell: ABxSxn_PM_A

Function: Generic Analog Fat Wire Bidirectional I/O



Description:

Noninverting bidirectional fat wire I/O for use with analog cores. Cell is required in order to connect analog signals or analog core power supplies from a chip PAD pin to a core pin in perimeter I/O packages.

PT	Internal bidirectional (pass-through)
PAD	External bidirectional

Cell units: 1 cell

Sixty cells are described in the naming convention below:

Naming Conventions

Character	Description
Third	ESD characteristics.ESD diodes terminate to VDD. To avoid latchup concerns it is essential that VDD is powered before power/signal is applied to PAD. ESD versions cannot be used on parts where VDD ≠ 1.8V. N No ESD C ESD for 1.8V signals P ESD for 2.5V signals Q ESD for 3.3V signals
Fourth	Shielding S Shielded
Fifth	I/O socket type A Any wired I/O D DC test I/O T Test I/O
Sixth	For physical design only; specifies which second supply passes through the cell. 0 For single supply chips only 1 VDD150 (1.5V) 2 VDD250 (2.5V) 3 VDD330 (3.3V) 4 VDDAGP supply

Receiver Truth Table

Input	Output
PAD	PT
-	PAD

Driver Truth Table

Input	Output
PT	PAD
-	PT

Cell: AIxSxn_PM_A

Function: Generic Analog Fat Wire Receiver

Description:

Noninverting input fat wire receiver for use with analog cores. Cell is required in order to connect analog signals or analog core power supplies from a chip PAD pin to a core pin in perimeter I/O packages.

PAD External input

PT Internal output (pass-through)

Cell units: 1 cell

Sixty cells are described in the naming convention below:

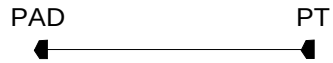
Naming Conventions

Character	Description
Third	ESD characteristics.ESD diodes terminate to VDD. To avoid latchup concerns it is essential that VDD is powered before power/signal is applied to PAD. ESD versions cannot be used on parts where VDD ≠ 1.8V. N No ESD C ESD for 1.8V signals P ESD for 2.5V signals Q ESD for 3.3V signals
Fourth	Shielding S Shielded
Fifth	I/O socket type A Any wired I/O D DC test I/O T Test I/O
Sixth	For physical design only; specifies which second supply passes through the cell. 0 For single supply chips only 1 VDD150 (1.5V) 2 VDD250 (2.5V) 3 VDD330 (3.3V) 4 VDDAGP supply

Receiver Truth Table

Input	Output
PAD	**PT**
-	PAD

Cell: AOxSxn_PM_A
Function: Generic Analog Fat Wire Driver



Description:
Noninverting output fat wire driver for use with analog cores. Cell is required in order to connect analog signals or analog core power supplies from a chip PAD pin to a core pin in perimeter I/O packages.

PAD External output

PT Internal input (pass-through)

Cell units: 1 cell

Sixty cells are described in the naming convention below:

Naming Conventions

Character	Description
Third	ESD characteristics.ESD diodes terminate to VDD. To avoid latchup concerns it is essential that VDD is powered before power/signal is applied to PAD. ESD versions cannot be used on parts where VDD ≠ 1.8V. N No ESD C ESD for 1.8V signals P ESD for 2.5V signals Q ESD for 3.3V signals
Fourth	Shielding S Shielded
Fifth	I/O socket type A Any wired I/O D DC test I/O T Test I/O
Sixth	For physical design only; specifies which second supply passes through the cell. 0 For single supply chips only 1 VDD150 (1.5V) 2 VDD250 (2.5V) 3 VDD330 (3.3V) 4 VDDAGP supply

Driver Truth Table

Input	Output
PT	PAD
-	PT

Glossary

ABIST	Array built-in self-test used in compilable SRAMs.
AFR	Average failure rate (0.0 hours to 40 kPOH) in FITs.
ASIC	Application-specific integrated circuit.
boundary-scan	A design methodology to allow testability of high pin count packages with a low number of primary inputs and outputs.
burn-in	Exercising the circuitry in a high temperature and voltage environment.
cell unit	A unit of area. A cell unit is 1 x 12 wiring channels for non-I/O cells; 120 x 576 for area array I/O cells or 96 x 576 for perimeter I/O cells. Each wiring channel is 0.56 µm wide.
compilable SRAM	A static random access memory circuit that can be compiled to fit size requirements.
DFT	Design-for-test.
DP	Data path.
DSF	Deterministic stuck-fault test.
EFR	Early failure rate (0.0 hours to 1 year of use) in FITs.
EOL	End of life.
FIT	Failures in time; equivalent to ppm/kPOH.
GA	Gate array, an array of background cells that are personalized using only the metal levels of the process.
HyperBGA	High-performance ball grid array

I_{ddq}	Quiescent power supply current.
I/O	Input or output.
internal cells	All cells except I/Os. This includes all primitive cells, all complex cells, all unique cells, and all latch cells. Also referred to as *internal logic.*
JTAG	Joint Test Action Group. Consortium of companies and universities that defined the IEEE 1149.1 boundary scan standard.
lead	A package input or output.
library	The collection of cells and macros representing the circuits offered by SA-27E.
lm	Last level metal.
LSSD	Level-sensitive scan design: a test methodology supported by SA-27E designs.
macro	A large circuit that can be placed on the chip image; a *compilable SRAM* or *compilable register array*, for example.
mz	Last level metal.
nontest I/O	A chip input or output buffer that must be connected to a latch for boundary-scan.
pad	In an input/output cell, the output pin of a driver, and/or the input to the receiver.
pin	A terminal or I/O port on a cell, or a package lead.
PLL	Phase-locked loop.
POH	Power on hours.
RPCT	Reduced pin count testing.
SC	Standard cell, a circuit personalized with diffusion and metal.

test I/O	A chip input or output buffer that does not need to be connected to a latch. This includes all test I/O used for boundary-scan test.
WRP	Weighted random pattern (for test).

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