Jonathan Ragan-Kelley

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Education

2014	PhD in Electrical Engineering & Computer Science, Massachusetts Institute of Technology Thesis: *Decoupling algorithms from the organization of computation for high performance image processing.* Advisors: *Frédo Durand & Saman Amarasinghe*
2007	SM in Electrical Engineering & Computer Science, Massachusetts Institute of Technology
2004	BS in Computer Science, Stanford University

Areas of specialization

Computer Graphics • Compilers • Domain-Specific Languages • High-Performance Systems

Work experience

2014-present	Stanford University. Postdoctoral Researcher.
2004-2014	Massachusetts Institute of Technology. Research assistant.
2012	Adobe Research. Research intern, leading Halide work.
2010	NVIDIA Research. Research intern, studying graphics pipeline scheduling primitives.
2008-2009	Intel (ART). Graphics architecture intern, researched Larrabee graphics pipeline, data parallel compilers.
2006-2007	Industrial Light & Magic. R&D intern, leading design of Lightspeed preview system.
2006	ATI Research. GPU architecture intern, studying decoupled sampling for graphics pipelines.
2004-2007	Tippett Studio. R&D consultant.
2002	NVIDIA. Rendering systems intern.
2001-2004	Stanford University. Research assistant, computer graphics.

Teaching Experience

Fall 2015	Stanford University. Instructor, *Domain Specific Languages for Graphics, Imaging, and Beyond (CS448h).*
Summer 2015	ACM SIGGRAPH 2015. Instructor, *Writing Fast Image Processing Code with Halide.*
Summer 2015	CVPR 2015. Instructor, *Fast Image Processing with Halide.*
Spring 2011	Massachusetts Institute of Technology. TA, *Digital and Computational Photography (6.815/6.865).*
Fall 2010	Lund University. Lecturer, 12 hour graduate seminar series on graphics architectures.

Honors

2008-2011	Intel Foundation PhD Fellowship
2007	MIT William A. Martin Award for Best Master's Thesis in Computer Science
2006-2008	NVIDIA Graduate Fellowship
2005-2007	National Science Foundation Graduate Research Fellowship
2004	Stanford University Best Undergraduate Thesis in Computer Science
2004	Stanford University Firestone Medal for Research
2000	Stanford University President's Scholarship

References

Frédo Durand
Professor, Electrical Engineering & Computer Science, Massachusetts Institute of Technology
fredo@csail.mit.edu

Saman Amarasinghe
Professor, Electrical Engineering & Computer Science, Massachusetts Institute of Technology
saman@csail.mit.edu

Pat Hanrahan
CANON USA Professor, Computer Science & Electrical Engineering, Stanford University
hanrahan@cs.stanford.edu

Mark Horowitz
Yahoo Founder's Professor, Electrical Engineering & Computer Science, Stanford University
horowitz@stanford.edu

Kayvon Fatahalian
Assistant Professor, Computer Science, Carnegie Mellon University
kayvonf@cs.cmu.edu

Refereed Publications

Simit: a Language for Physical Simulation.
Fredrik Kjølstad, Shoaib Kamil, **Jonathan Ragan-Kelley**, David Levin, Shinjiro Sueda, Desai Chen, Etienne Vouga, Danny Kaufman, Gurtej Kanwar, Wojciech Matusik, Saman Amarasinghe.
ACM Transactions on Graphics *(to appear)*.

Transform Recipes for Efficient Cloud Photo Enhancement.
Michaël Gharbi, YiChang Shih, Gaurav Chaurasia, **Jonathan Ragan-Kelley**, Sylvain Paris, Frédo Durand.
ACM Transactions on Graphics 34(6) *(Proc. SIGGRAPH Asia 2015)*.

Helium: Lifting High-Performance Stencil Kernels from Stripped x86 Binaries to Halide DSL Code.
Charith Mendis, Jeffrey Bosboom, Kevin Wu, Shoaib Kamil, **Jonathan Ragan-Kelley**, Sylvain Paris, Qin Zhao, Saman Amarasinghe.
SIGPLAN Notices 50(6) *(Proc. PLDI 2015)*.

Compiling High Performance Recursive Filters.
Gaurav Chaurasia and **Jonathan Ragan-Kelley** and Sylvain Paris and George Drettakis and Frédo Durand.
Proceedings of High-Performance Graphics 2015.

Darkroom: Compiling High-Level Image Processing Code into Hardware Pipelines.
James Hegarty, John Brunhaver, Zachary DeVito, **Jonathan Ragan-Kelley**, Noy Cohen, Stephen Bell, Artem Vasilyev, Mark Horowitz, Pat Hanrahan.
ACM Transactions on Graphics 33(4) *(Proc. SIGGRAPH 2014)*.

OpenTuner: An Extensible Framework for Program Autotuning.
Jason Ansel, Shoaib Kamil, Kalyan Veeramachaneni, **Jonathan Ragan-Kelley**, Jeffrey Bosboom, Una-May O'Reilly, Saman Amarasinghe.
International Conference on Parallel Architectures and Compilation Techniques *(PACT 2014)*.

OpenFab: A Programmable Pipeline for Multi-Material Fabrication.
Kiril Vidimče, Szu-Po Wang, **Jonathan Ragan-Kelley**, Wojciech Matusik.
ACM Transactions on Graphics 32(4) *(Proc. SIGGRAPH 2013)*.

Optimizing Parallelism, Locality, and Recomputation in Image Processing Pipelines.
Jonathan Ragan-Kelley, Connelly Barnes, Andrew Adams, Sylvain Paris, Frédo Durand, Saman Amarasinghe.
SIGPLAN Notices 48(6) *(Proc. PLDI 2013)*.

Portable Performance on Heterogeneous Architectures.
Phitchaya Phothilimthana, Jason Ansel, **Jonathan Ragan-Kelley**, Saman Amarasinghe.
SIGARCH Computer Architecture News 41(1) *(Proc. ASPLOS 2013)*.

Decoupling Algorithms from Schedules for Easy Optimization of Image Processing Pipelines.
Jonathan Ragan-Kelley, Andrew Adams, Sylvain Paris, Marc Levoy, Saman Amarasinghe, Frédo Durand.
ACM Transactions on Graphics 31(4) *(Proc. SIGGRAPH 2012)*.

Decoupled Sampling for Graphics Pipelines.
Jonathan Ragan-Kelley, Jaakko Lehtinen, Jiawen Chen, Michael Doggett, Frédo Durand.
ACM Transactions on Graphics 30(3) *(presented at SIGGRAPH 2011)*.

A Hierarchical Volumetric Shadow Algorithm for Single Scattering.
Ilya Baran, Jiawen Chen, **Jonathan Ragan-Kelley**, Frédo Durand, Jaakko Lehtinen.
ACM Transactions on Graphics 29(6) *(Proc. SIGGRAPH Asia 2010)*.

The Lightspeed Automatic Interactive Lighting Preview System.
Jonathan Ragan-Kelley, Charlie Kilpatrick, Brian Smith, Doug Epps, Paul Green, Christophe Hery, Frédo Durand.
ACM Transactions on Graphics 26(3) *(Proc. SIGGRAPH 2007)*.

Ongoing Work

A DSL for non-linear least squares on GPUs. *(In preparation, draft available by request)*
Automatic scheduling for Halide programs. *(In preparation, draft available by request)*
A systematic approach to blocking convolutional neural networks. *(In review, draft available by request)*

Select Invited Talks

Decoupling algorithms from the organization of computation for high-performance graphics & imaging.
University of California, Berkeley, Mar. 2013; Stanford University, Apr. 2013; Microsoft Research, Jun. 2013; Carnegie Mellon University, Dec. 2014.

Keeping many cores busy: scheduling the graphics pipeline.
SIGGRAPH 2010 & 2011 course, Beyond Programmable Shading.

Decoupled sampling for real-time graphics pipelines.
SIGGRAPH 2010 course, Beyond Programmable Shading; NVIDIA Research Helsinki, Oct. 2010.

Why graphics is fast, and what it can teach us about parallel programming.
Harvard University, Nov. 2009; University College London, Dec. 2009.

Professional Activities

Program Committees

ACM PLDI *External Review Committee Member, 2016*
ACM SIGGRAPH Asia *Papers Committee Member, 2015*
High Performance Graphics *Papers chair, 2014*
High Performance Graphics *PC member (2010, 2011, 2012, 2013)*

Reviewer

ACM SIGGRAPH *(2006-2015)*
ACM SIGGRAPH Asia *(2008, 2009, 2011-2014)*
ACM Transactions on Graphics *(2005, 2006)*
ACM PLDI *(2010, 2011, 2014)*
Computer Graphics Forum *(2012)*
Eurographics *(2008, 2009)*
Eurographics Symposium on Rendering *(2007-2009)*
High Performance Graphics *(2009)*
SIGGRAPH Graphics Hardware Workshop *(2008)*
SIGGRAPH Symposium on Interactive 3D Graphics *(2011)*
IEEE International Conference on Computational Photography *(2009)*

Personal

Born: March 21, 1982—Palo Alto, CA *(US Citizen)*