Chapter 26
Modular System for High-Speed 24-Bit Data Acquisition of Triaxial MEMS Accelerometers for Structural Health Monitoring Research

Brianna Klingensmith, Stephen R. Burgess, Thomas A. Campbell, Peter G. Sherman, Michael Y. Feng, Justin G. Chen, and Oral Buyukozturk

Abstract A hardware system has been developed to obtain data from multiple MEMS triaxial accelerometers for structural health monitoring research. The system can be easily configured for a single accelerometer or up to as many as 120 triaxial accelerometers with 24-bit data sampled up to a 2 kHz rate simultaneously. The system is modular where each module consists of an electrical board that supports up to eight accelerometers. Each module powers the accelerometers, conditions the analog output from the accelerometers, and performs analog-to-digital conversion. In addition, the module has an FPGA that timestamps and packetizes the digital data. The data from each module is transmitted to a host computer using serial communication through a USB virtual COM port. A LabVIEW application on a host computer logs and processes the data, although any software that can perform serial communication and data parsing, e.g. MATLAB, can be utilized. In the case of a single module with eight accelerometers, a single laptop computer can be used for both electrical power and user interaction making an ideal setup for measurements in the field.

Keywords MEMS accelerometer • Distributed sensor network • 24-bit resolution • Synchronization • LabVIEW

26.1 Introduction

The Massachusetts Institute of Technology Energy Initiative (MITEI) Distributive Sensing program is a collaboration between MIT CSAIL and MIT Civil Engineering and Draper Lab to develop a cutting edge structural health monitoring system for the oil and gas industry.

Draper's role was to implement a ~100 MEMS accelerometer network for a laboratory-scale structure. The MIT teams focused on damage detection algorithms and helped develop the requirements for the accelerometer network such as sampling rate. MEMS accelerometers were chosen over integrated electronic piezoelectric (IEPE) accelerometers for their low cost and low power. The laboratory-scale structure is shown in Fig. 26.1, and the Draper accelerometer package is shown in Fig. 26.2.

This paper will focus on the MEMS accelerometer network.

26.2 Requirements and Network Architecture

The MEMS accelerometers were the STMicro LIS344ALH triaxial accelerometer incorporated into a Draper designed and built package. This accelerometer had a specified noise density of 50 $\mu g/\sqrt{Hz}$; we chose a 1 kHz bandwidth (0–1 kHz), so the noise would be 1.6 mg which dictated a 24-bit analog-to-digital resolution requirement. Based on the

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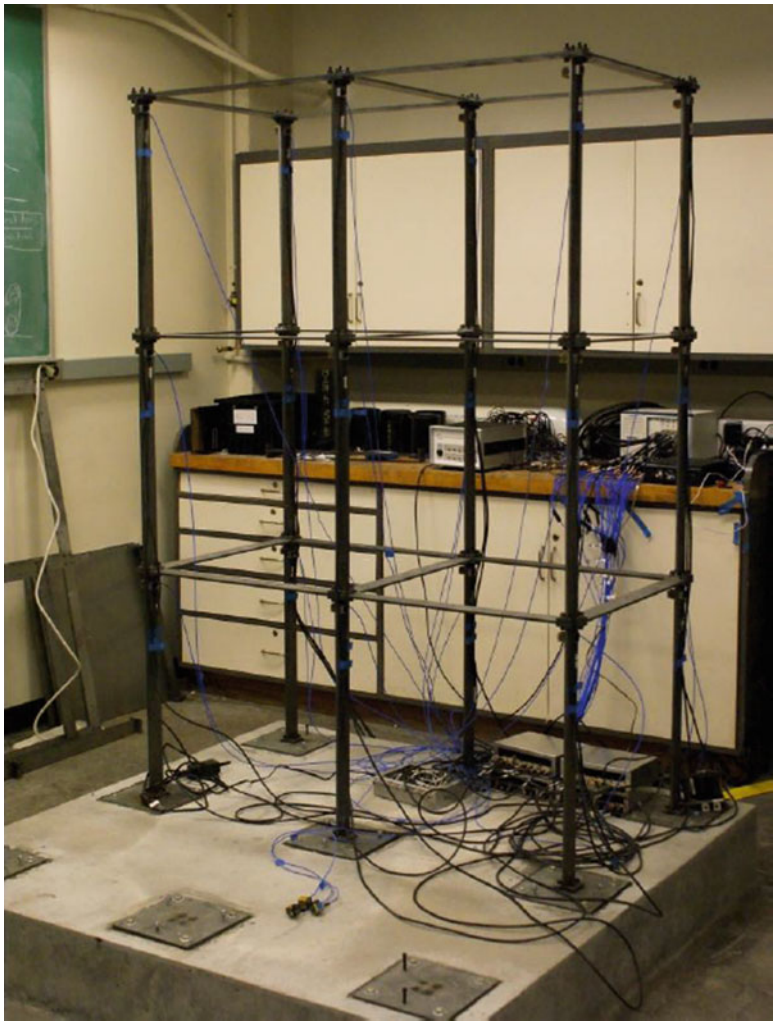

Fig. 26.1 Laboratory-scale structure with MEMS accelerometer network installed. Each structural member is 60 cm in length; therefore, the structure's dimensions are 180 cm height by 120 cm width by 60 cm depth

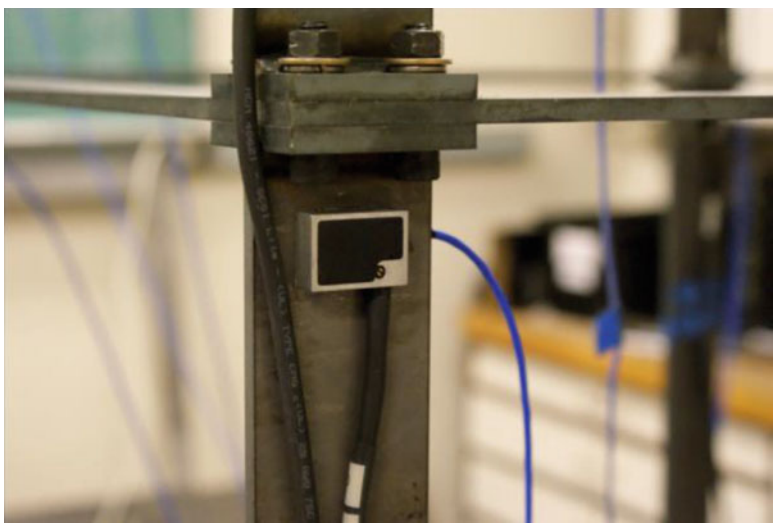

Fig. 26.2 Draper accelerometer assembly installed on lab structure

largest laboratory structure configuration planned, the network had to accommodate up to 120 triaxial accelerometers. To measure the propagation of waves through the structure, accelerometer outputs were synchronized to within 0.1 ms. Lastly, the MIT CEE team established the requirement to monitor structural modes up to 1 kHz necessitating a sampling rate of at least 2 kHz per channel. These requirements are summarized in Table 26.1.

Table 26.1 Requirements

	Value	Driver
ADC resolution	24-bit	ADC resolution to be below noise floor of accelerometer
Sampling frequency	2,000 Hz	Sense modal frequencies up to 1 kHz
# of triaxial accelerometers	120	Size of laboratory structure
Data synchronization	0.1 μs	Sense mechanical wave propagation across structure

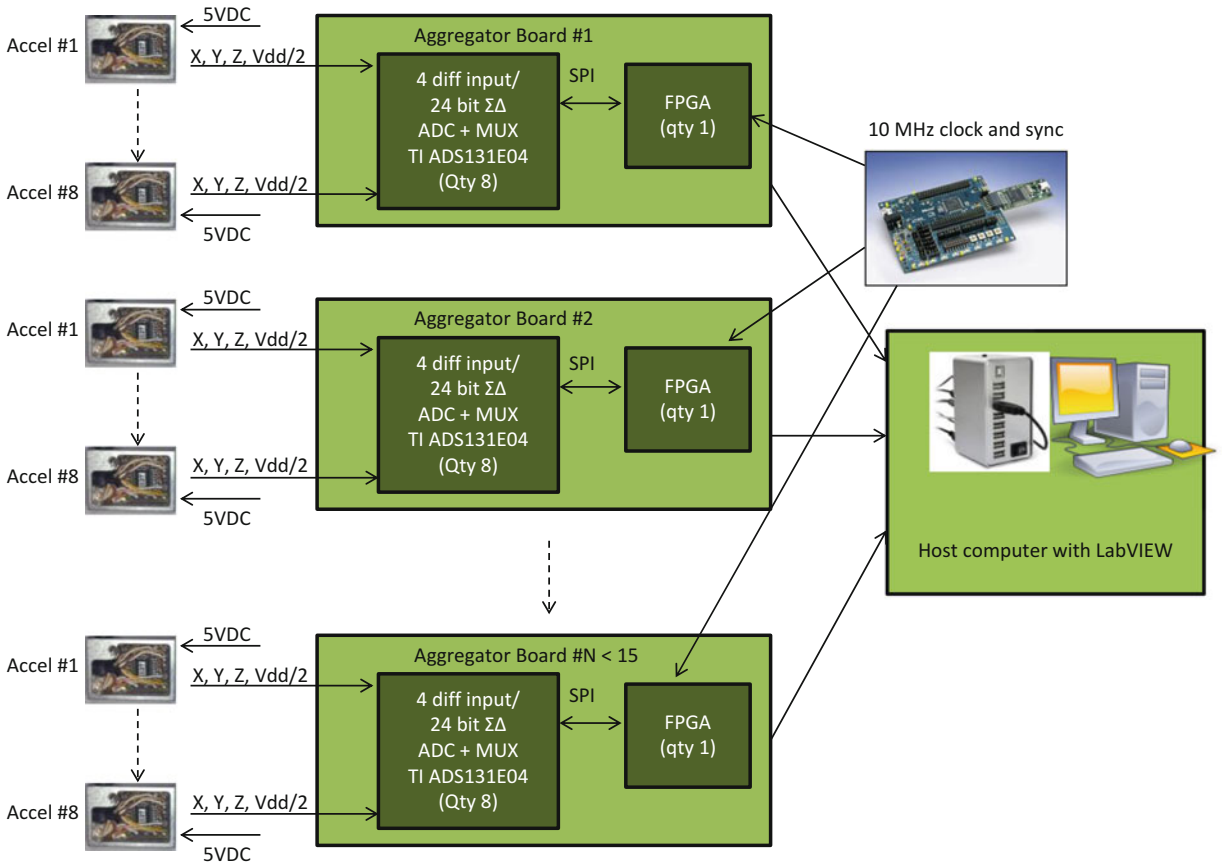

Fig. 26.3 Modular architecture for accelerometer network. Each aggregator board accommodates eight accelerometers and can be added to grow the size of the network. Single clock for data synchronization is also shown

To meet these requirements, we developed a modular architecture where the basic building block was a custom electronics board called the MITEI Aggregator Board. The MITEI Aggregator Board conditions and digitizes 3-axis analog accelerometer signals from up to eight accelerometers. The digitized accelerometer data is then time stamped, packetized, and transmitted via USB 2.0 to a host PC for analysis. To network more than eight accelerometers, two or more aggregator boards are timed with a single 10 MHz clock for synchronization, and each aggregator board connects to the host PC separately via an individual USB2.0 cable. We tested a network size of 15 aggregator boards, i.e. 120 accelerometers, although this is not necessarily the upper limit. However, USB limitations and PC limitations on handling the data flow, i.e. writing the data to files quickly enough, eventually limit the network size. This architecture is depicted in Fig. 26.3.

26.3 Aggregator Board Overview

The fundamental building block of the modular network system is the aggregator board which is comprised of three sections:

- an analog front end section,
- an analog-to-digital converter (ADC) section,
- and a digital section composed of an FPGA and a UART/USB bridge.

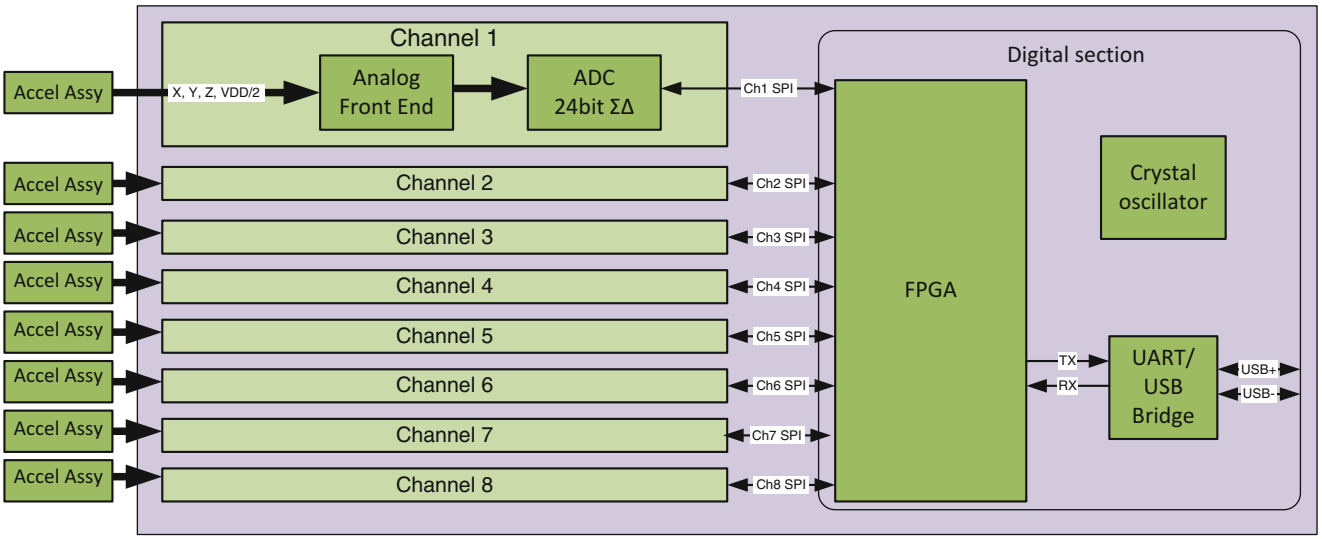

Fig. 26.4 MITEI aggregator board functional block diagram

Each of these sections is shown in the functional block diagram in Fig. 26.4.

There are eight individual subsections of the analog front end channel, one per accelerometer assembly. Each front end subsection receives signals from each axis (X, Y, Z) as well as a common reference signal (Vdd/2) from its respective accelerometer assembly. It provides scaling, single ended to differential conversion, and filtering of each signal.

There are also eight individual subsections of the ADC section. Each subsection consists of a 4-channel, differential, 24 bit delta-sigma, simultaneous sampling analog-to-digital converter integrated circuit (IC) along with supporting electronics. Each subsection digitizes the analog signals output from the front end.

Lastly, the digital section consists of one FPGA, its supporting electronics, a crystal oscillator and a UART/USB bridge IC. This section is responsible for controlling analog-to-digital conversion, aggregating, and transmitting the outputs from all eight ADC subsections to a PC via USB 2.0.

26.4 Front End Section Design

The main requirement of the front end circuitry is the conditioning of the incoming accelerometer signals to take advantage of the full dynamic range of the ADC as well as to filter out as much noise as possible The LIS344ALH accelerometers can sense up to ±6 g and have a nominal scale factor of 0.22 V/g. This means that the full range of the accelerometer output is from 0.33 V (−6 g) to 2.97 V (+6 g), with 0 g at 1.65 V. The ADC IC, the ADS131E04, only accepts inputs between 0 V and 2.5 V.

To fit the accelerometer output into the ADC input range, the front end section scales the accelerometer output. In addition, the front end circuitry provides the inverse of the accelerometer output for use in the differential input to the ADC. This also makes 0 g correspond to 0 V input at the ADC.

Assuming the nominal scale factor of 0.22 V, the front end circuitry converts the acceleration, a, with units of g's to an analog voltage input to the ADC section, $INP - INN$, as follows:

$$INP - INN = 0.3636a$$

which provides an input range of −2.18 V to 2.18 V to the ADC section corresponding to −6 g to +6 g.

26.5 ADC Section Design

The ADC section was based on the Texas Instruments ADS131E04 analog-to-digital converter IC. The ADS131E04 contains four separate converters that simultaneously sample its four analog inputs. It is a 24 bit delta-sigma converter that allows selectable data rates from 1 up to 64 kHz, contains a programmable gain amplifier, and operates off of a single 3.3 V supply. It is configured and sampled through a Serial Peripheral Interface (SPI).

26.6 Digital Section Design

The digital section consists of an FPGA (Actel IGLOO AGLN250V2-VQG100), its supporting electronics, a 20 MHz crystal oscillator and a high speed UART/USB bridge (Exar XR21V1410). The FPGA provides sample timing and control to all eight ADC's and processes and packages all accelerometer samples. The FPGA then transmits the packaged data at a predetermined rate in RS422 format to the UART/USB bridge. The UART/USB bridge retransmits the data in USB 2.0 format to a USB hub connected to a PC.

The digital section can use the 20 MHz on-board crystal oscillator as the clock when only one aggregator board is in use or a separate 10 MHz off-board clock that is shared by multiple aggregator boards for data synchronization.

26.7 Noise Measurements

To assess the noise of the system and ensure that all components of the MITEI Aggregator Board remain below the noise floor of the LIS344ALH, the following tests were completed:

26.7.1 Front End Breadboard Noise

Before fabricating the MITEI Aggregator Board, a quick-turn breadboard was designed to assess the pieces of the front end circuitry used to tailor the accelerometer output to the ADC input; it did not include the anti-alias stage. Two sets of noise measurements were taken on the output of each axis of the breadboard. The accelerometer was connected to the inputs of each axis for the first set of measurements and then was disconnected for the second. Figure 26.5 shows the two noise measurements for the X-axis. The Y and Z axis were comparable to X, therefore, they are not shown in the following figure:

The resonant frequency of the accelerometer is 1.8 kHz, and the accelerometer package has a low pass filter with a front 1 kHz cutoff on the accelerometer output. Therefore, the noise was examined at 1 kHz. It is believed that the noise spike near 8 kHz on the breadboard is due to the fact that the op-amps used in the front circuitry are auto-zeroing chopper-stabilizer parts that utilize an oscillator in order to perform the auto-zeroing function. This spike should be greatly attenuated when the anti-alias stage is in place.

The LIS344ALH accelerometer has a nominal noise density of 50 $\mu g/\sqrt{Hz}$ which corresponds to 11 $\mu V/\sqrt{Hz}$ when multiplying by the 0.22 V/g scale factor. The actual test data shows a lower value of 7 $\mu V/\sqrt{Hz}$. This demonstrates that the noise of the front end electronics (excluding the anti-alias stage) should not reach the noise floor of the accelerometer outputs and, therefore, not introduce additional noise into the measured signals.

26.7.2 MITEI Aggregator Board Noise

For the complete MITEI Aggregator Board, two accelerometers were connected to channels 1 and 2 of a single Aggregator Board; both accelerometers were fixed to a mechanically isolated stone slab to minimize input acceleration. Channel 0's X, Y, and Z inputs were shorted to Vdd/2 (1.65 V) corresponding to 0 g. In this configuration, 10 minutes of data were recorded from these three channels at 2 kHz. The noise density values were calculated for channels with and without a sensor attached and are shown in Table 26.2.

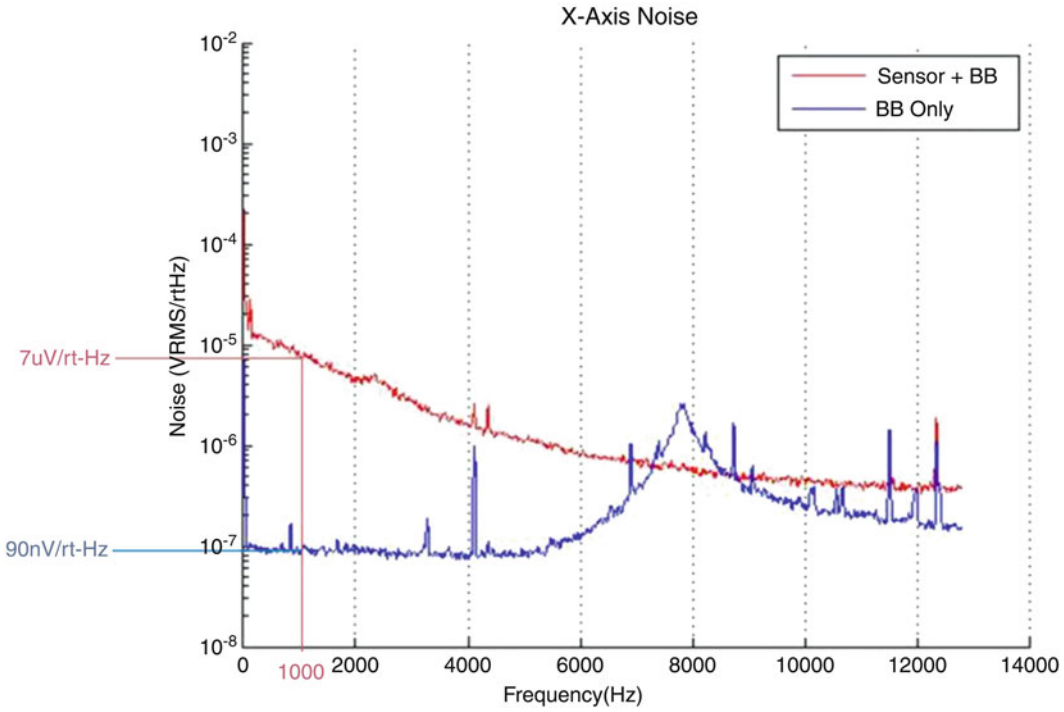

Fig. 26.5 Breadboard front end X-axis noise. *BB*: breadboard

Table 26.2 Calculated noise measurements

System component	Noise density
Breadboard	90 nV/$\sqrt{\text{Hz}}$
Breadboard + sensor	7 μV/$\sqrt{\text{Hz}}$
Sensor (based on datasheet)	11 μV/$\sqrt{\text{Hz}}$
Aggregator board (channel 0)	112.3 nV/$\sqrt{\text{Hz}}$
Aggregator board + sensor (ch 1 or 2)	4.17 μV/$\sqrt{\text{Hz}}$

For the full aggregator board, the calculated noise density with the sensor disconnected from the electronics is over an order of magnitude lower than with the sensor connected. This demonstrates that the noise of Aggregator electronics (Sects. 26.4–26.6) will not exceed the noise floor of the accelerometer outputs and, therefore, not add noise into the measured signals (Table 26.2).

26.8 Power

The aggregator board only needs 5VDC for power. This can be done in two ways: a power jack that accepts an AC-DC power supply or a modified USB cable plugged into an eight pin connector on the board. The modified USB cable enables a laptop to simultaneously power and host a single aggregator board making it ideal for field use. The following table lists power measurements for a single aggregator board with and without its full complement of eight sensors (Table 26.3).

26.9 LABVIEW GUI for Host PC

Each aggregator board is connected to a single host PC via USB2.0 cables and is recognized as a virtual COM port on the PC. A LabVIEW program reads the data packets being streamed from each aggregator board as serial data and then writes the data to files on the hard drive. Because the aggregator board transmits the data to the host PC as serial data, any software package capable of serial communicable, e.g. MATLAB, can be used on the host PC. The MIT team then accesses the data files on the host PC. Figure 26.6 shows the LabVIEW GUI.

Table 26.3 Power measurements

System component	Power
Aggregator board	775 mW
Aggregator board + eight accelerometers	800 mW

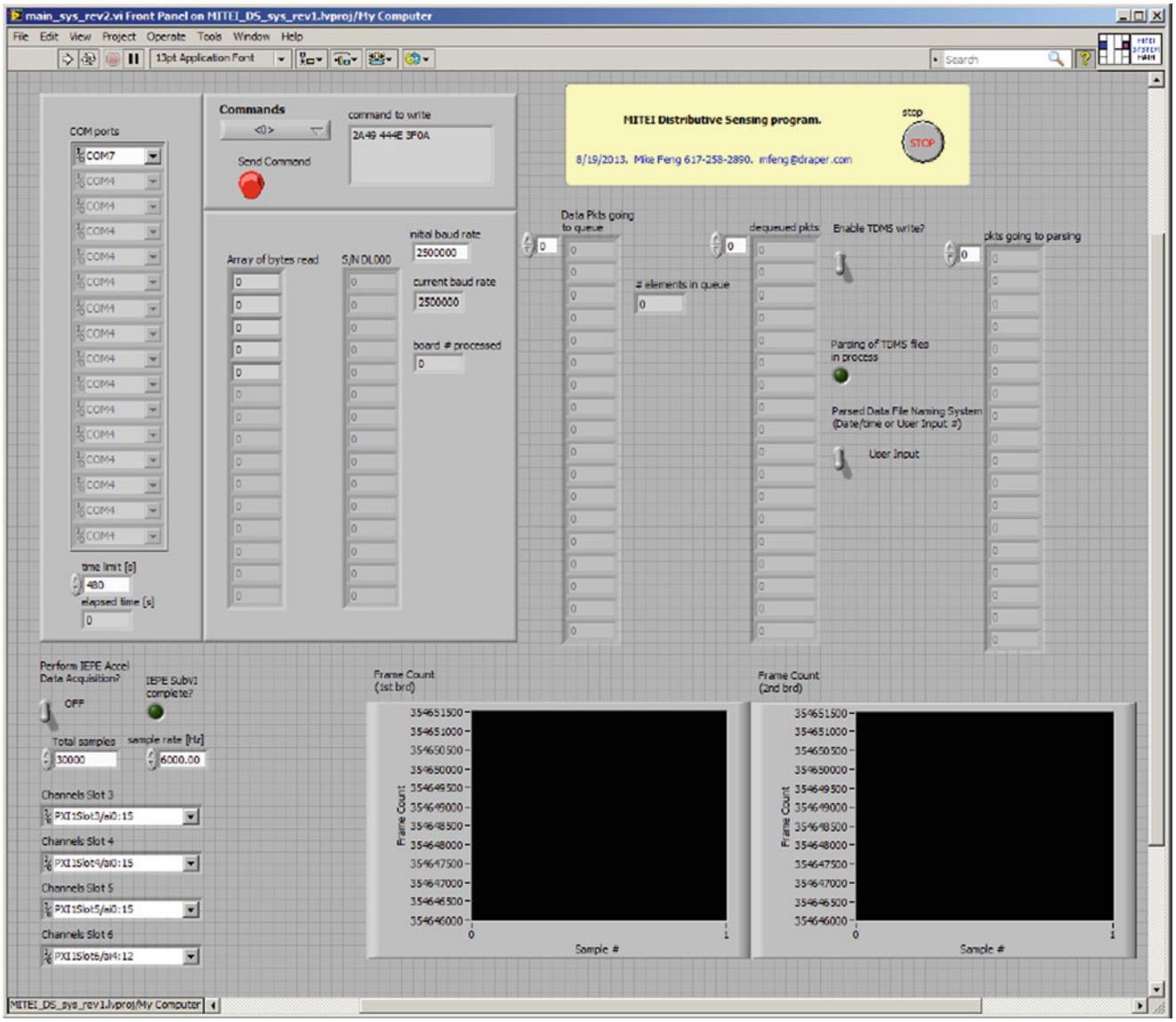

Fig. 26.6 LabVIEW GUI for host PC. Each aggregator board is a separate COM port (*upper left corner*)

26.10 Conclusions

A modular network of up to 120 MEMS accelerometers has been developed around a custom electronics board that features very high 24-bit ADC resolution and 0.1 microsecond synchronization. The selected ADC component also provides simultaneous sampling of all channels. Testing has shown overall noise is only limited by the noise inherent in the MEMS accelerometers. When only a single aggregator board accommodating up to eight accelerometers is in use, a single laptop can supply power and serve as the host PC which is useful for field work. For networks of greater than eight accelerometers,

the network is easily extended by adding multiple aggregator boards up to a total of 120 accelerometers. The aggregator board(s) streams the data to a single host computer where any number of software packages can be used to read the data and write it to a file for postprocessing.

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