

Kunal Agrawal

Work Address

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Cambridge, MA 02139
kunal@csail.mit.edu

Home Address

24 Magazine Street #3
Cambridge, MA 02139
(650) 704 3274

Education

Massachusetts Institute of Technology

Ph.D. Candidate, Computer Science and Engineering

2003—July 2009 [Expected]

Cumulative GPA: 5.0/5.0 Thesis Topic: Scheduling and Synchronization for Multicore Processors

National University of Singapore, Singapore-MIT Alliance

S.M., Computer Science

July 2001—June 2002

Cumulative GPA: 5.0/5.0

Ramrao Adik Institute of Technology, Mumbai University

Bachelors of Engineering, Electronics Engineering

July 1997—June 2001

Graduated with Distinction

Interests

Parallel Computing, Algorithms, Scheduling, Transactional Memory, Synchronization Mechanisms, Dynamic Multithreading, Stream Programming, Cache-Efficient Algorithms, Memory Models.

Experience

MIT CSAIL, Supercomputing Technologies Group

Cambridge, MA

August 2003—present

Research Assistant. Worked on scheduling, synchronization and locality issues for parallel processors. In the domain of scheduling, my contributions include provably efficient algorithms for adaptive scheduling for dynamic multithreaded languages like Cilk and complexity results of scheduling workflow applications. In addition, I implemented an adaptive scheduler in the Cilk runtime system. In the domain of synchronization, I have primarily worked on transactional memory semantics and design. In the domain of locality, I am working on provably good cache-efficient schedulers for streaming applications.

Adviser: Prof. Charles E. Leiserson.

VMWare Inc.

Palo Alto, CA

June 2006—August 2006

Software Intern. Developed and evaluated algorithms for load balancing and resource allocation for virtual machines on a cluster of computers.

Mentor: Minwen Ji

Singapore-MIT Alliance, National University of Singapore

Singapore

June 2002—June 2003

Research Assistant. Implemented a page-level distributed shared memory system using MPI and C.

Advisor: Prof. Wong Weng Fai

MIT LCS, Compilers Group

Cambridge, MA

Feb 2003—April 2003

Visiting Scholar. Implemented bit packing optimizations in the Streamit Compiler using Java.

Advisor: Saman Amarasinghe

Kent Ridge Digital Labs

Singapore

January 2002—June 2002

Research Intern. Worked on two bioinformatics projects called “Splice-Site Recognition using Support Vector Machines” and “Use of Self Organizing Neural Networks as Filters of Clean Start Codon.”

Advisor: Dr. Vladimir Bajic

Bhabha Atomic Research Center

Mumbai, India

July 2000—June 2001

Research Intern. Worked on design and implementation of microcontroller interface to measure reactor fluid levels. The project involved hardware design using VHDL programming.

Advisor: Dr Patil.

Teaching

MIT EECS Department

Cambridge, MA

Spring 2005, Fall 2005, Spring 2007

Teaching Assistant. Assisted for the introductory algorithms course.

MIT EECS Department, Women's Technology Program

Cambridge, MA

Summer 2004

Mathematics Instructor. Independently designed and taught a condensed course on Discrete Mathematics in a summer program for talented high school girls.

Singapore-MIT Alliance, National University of Singapore

Singapore

Fall 2002

Teaching Assistant. Assisted for the compilers course.

Conference Publications

1. Safe Open-Nested Transactions Using Ownership

Kunal Agrawal, Angelina Lee and Jim Sukha. In the *Proceedings of the ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)* 2009.

2. Mapping Linear Workflows with Computation/Communication Overlap

Kunal Agrawal, Anne Benoit and Yves Robert. In the *Proceedings of International Conference on Parallel and Distributed Systems (ICPADS)* 2008.

3. Nested Parallelism in Transactional Memory.

Kunal Agrawal, Jeremy Fineman, and Jim Sukha. In the *Proceedings of the ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)* 2008.

4. Worst Page-Replacement Strategy.

Kunal Agrawal, Michael Bender and Jeremy Fineman. In the *Proceedings of the Fourth International Conference on Fun with Algorithms (FUN)* 2007.

5. Work Stealing with Parallelism Feedback.

Kunal Agrawal, Yuxiong He, and Charles E. Leiserson. In the *Proceedings of the ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)* 2007.

6. Memory Models for Open-Nested Transactions.

Kunal Agrawal, Charles E. Leiserson, and Jim Sukha. In the *Proceedings of the ACM/SIGPLAN Workshop on Memory Systems Performance and Correctness (MSPC)* 2006.

7. An Empirical Evaluation of Work Stealing with Parallelism Feedback.

Kunal Agrawal, Yuxiong He, and Charles E. Leiserson. In the *Proceedings of the International Conference on Distributed Computing Systems (ICDCS)* 2006.

8. Adaptive Scheduling with Parallelism Feedback.

Kunal Agrawal, Yuxiong He, Wen Jing Hsu, and Charles E. Leiserson. In the *Proceedings of ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)* 2006.

9. Mapping Pipelined Filtering Services with Communication Cost.

Kunal Agrawal, Anne Benoit, Fanny Defosse, and Yves Robert. *Submitted for Publication.* 2009.

Journal Publications	<ol style="list-style-type: none"> 1. Adaptive Work Stealing with Parallelism Feedback Kunal Agrawal, Yuxiong He, Wen Jung Hsu, and Charles Leiserson. <i>ACM Transactions on Computer Systems (TOCS)</i> 2008. 2. The Worst Page Replacement Strategy Kunal Agrawal, Michael Bender and Jeremy Fineman. <i>Theory of Computer Systems</i> 2008. 																
Conference Talks	<ol style="list-style-type: none"> 1. Safe Open-Nested Transactions Through Ownership. <i>ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)</i> 2009. 2. Nested Parallelism in Transactional Memory. <i>ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)</i> 2008. 3. Worst Page-Replacement Strategy. <i>International Conference on Fun with Algorithms (FUN)</i> 2007. 4. Work Stealing with Parallelism Feedback. <i>ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)</i> 2007. 5. An Emprical Evaluation of Work Stealing with Parallelism Feedback. <i>International Conference on Distributed Computing Systems (ICDCS)</i> 2006. 6. Adaptive Scheduling with Parallelism Feedback <i>ACM/SIGPLAN Symposium on the Principles and Practices of Parallel Programming (PPOPP)</i> 2006. 																
Invited Talks	<p>Adaptive Scheduling with Parallelism Feedback.</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>University of Paris 6</i></td> <td style="text-align: right;">2008.</td> </tr> <tr> <td><i>Microsoft</i></td> <td style="text-align: right;">2007.</td> </tr> <tr> <td><i>Stanford University</i></td> <td style="text-align: right;">2006.</td> </tr> </table> <p>Feedback Driven Adaptive Scheduling</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>NSF-NGS workshop held in conjunction with IPDPS</i></td> <td style="text-align: right;">2007</td> </tr> </table>	<i>University of Paris 6</i>	2008.	<i>Microsoft</i>	2007.	<i>Stanford University</i>	2006.	<i>NSF-NGS workshop held in conjunction with IPDPS</i>	2007								
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Patent	<p>Computing the Processor Desires of Jobs in an Adaptively Parallel Scheduling Environment</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>Co-authored with Charles E. Leiserson, Yuxiong He, and Wen Jing Hsu (Under Review)</i></td> <td style="text-align: right;">2007</td> </tr> </table>	<i>Co-authored with Charles E. Leiserson, Yuxiong He, and Wen Jing Hsu (Under Review)</i>	2007														
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Grant	<p>Feedback Driven Adaptive Scheduling</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>NSF grant proposal co-authored with Charles E. Leiserson (Funded for \$484,000 over 3 years)</i></td> <td style="text-align: right;">2006</td> </tr> </table>	<i>NSF grant proposal co-authored with Charles E. Leiserson (Funded for \$484,000 over 3 years)</i>	2006														
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Professional Service	<p>Program Committee Chair and Organizer.</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>The Fourth CSAIL Student Workshop</i></td> <td style="text-align: right;">2008</td> </tr> </table> <p>Program Committee Member and Volunteer.</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>CSAIL Student Workshop</i></td> <td style="text-align: right;">2005, 2006, 2007</td> </tr> </table> <p>Reviewer.</p> <table border="0" style="width: 100%;"> <tr> <td style="width: 80%;"><i>Symposium on Paralellism in Algorithms and Architectures</i></td> <td style="text-align: right;">2009</td> </tr> <tr> <td><i>Symposium on Paralellism in Algorithms and Architectures</i></td> <td style="text-align: right;">2007</td> </tr> <tr> <td><i>European Conference on Parallelism</i></td> <td style="text-align: right;">2005</td> </tr> <tr> <td><i>International Conference on High Performance Computing</i></td> <td style="text-align: right;">2005</td> </tr> <tr> <td><i>Journal of Discrete Algorithms</i></td> <td></td> </tr> <tr> <td><i>Parallel Computing</i></td> <td></td> </tr> </table>	<i>The Fourth CSAIL Student Workshop</i>	2008	<i>CSAIL Student Workshop</i>	2005, 2006, 2007	<i>Symposium on Paralellism in Algorithms and Architectures</i>	2009	<i>Symposium on Paralellism in Algorithms and Architectures</i>	2007	<i>European Conference on Parallelism</i>	2005	<i>International Conference on High Performance Computing</i>	2005	<i>Journal of Discrete Algorithms</i>		<i>Parallel Computing</i>	
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Honors	Merit award for outstanding performance in SMA5503: Design of Algorithms	2002
	Merit award for outstanding performance in SMA5506: Computer Systems Engineering.	2002
	2 nd among 120 students in the class in Bachelors of Electronics Engineering.	2001
	Finalist, Indian National Mathematics Olympiad	1996

References

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|---|---|
| 1. Charles E. Leiserson
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| 3. Yves Robert
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Fax: (+33) 4 72 72 88 06
Yves.Robert@ens-lyon.fr | 4. Srinivasa Devadas
Voice: (617) 253-0454
Fax: (617) 253-6652
devadas@mit.edu |