Michel A. Kinsy

Curriculum Vitae

Department of Electrical and Computer Engineering, Boston University
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Research Interests

Computer architecture, with particular emphasis on: secure architecture design, hardware security, neural network acceleration, network-on-chip (NoC) routing, self-aware polymorphic architecture design, and large-scale, hard real-time, secure, distributed computer systems architecture.

Education

2013   **Ph.D., Electrical Engineering and Computer Science**.
Massachusetts Institute of Technology, Cambridge, MA.
Thesis: "Many-core Architectures with Time Predictable Execution Support for Hard Real-time Applications"
Thesis advisor: Srinivas Devadas
Minor in Finance, Sloan School of Management.

2009   **M.S., Electrical Engineering and Computer Science**.
Massachusetts Institute of Technology, Cambridge, MA.
Thesis Title: "Application-Aware Deadlock-Free Oblivious Routing"
Thesis advisor: Srinivas Devadas.

2007   **B.S.E, Computer Systems Engineering**, *Arizona State University*, Tempe, AZ.
Magna Cum Laude.

2007   **B.S., Computer Science**, *Arizona State University*, Tempe, AZ.
Magna Cum Laude.

Appointments

2016–present   Assistant Professor,
Department of Electrical and Computer Engineering, Boston University.
Director of the Adaptive and Secure Computing Systems (ASCS) Laboratory

Lead the laboratory's research efforts in hardware security, emerging adaptive architectures and artificial neural network acceleration.

2014–2016   Assistant Professor,
Department of Computer and Information Science, University of Oregon.
Director of the Computer Architecture and Embedded Systems Laboratory

2014–2016   Research Affiliate,
Computer Science and Artificial Intelligence Laboratory (CSAIL),
Massachusetts Institute of Technology.

2013–2014 Technical Staff,
Lincoln Laboratory (FFRDC)
Massachusetts Institute of Technology.

Advanced Computer Concepts: Photonically Optimized Embedded Microprocessors (POEM) to demonstrate the integration of photonics technologies within embedded microprocessors for seamless, energy-efficient, high-capacity communications.

Self-Aware Secure Architectures: Cognitive and adaptive architectures that are able to reason about the trade-off between the precision of results and the computational time and enforce execution security policies.

2010–2013 Research Assistant, Institute for Soldier Nanotechnologies, MIT.
Ivan Celanovic Group

MARTHA Project: Work in this laboratory focuses on advanced nanotechnology research to improve the survival of future soldiers. One of the mission areas is next generation high-performance computing. I led the design efforts for a prototype time-predictable computer architecture for cyber-physical systems, called MARTHA (Multicore Architecture for Real-Time Hybrid Applications).

2007–2013 Research Assistant, Computer Science and Artificial Intelligence Laboratory, MIT.
Computation Structures Group
Srinivas Devadas Group

Research Activities: Emerging computing models and technologies: reconfigurable multicore substrate, networks-on-chip (NoCs), systems-on-chip (SoCs), embedded systems, hardware security, heterogeneous systems, and high performance computing.

2006–2007 Undergraduate Research Assistant, ASU.
VLSI Electronic Design Automation Laboratory
Sarma Vrudhula Group

Hybrid Energy Project: Hydrogen based fuel cell and Li-ion batteries hybrid energy source prototype for usage in portable electronic devices. The system includes a fuel processor, a PEMFC stack and its controller, and a charge management subsystem.

1/2007– 5/2007 Undergraduate Research Assistant, ASU.
Web and Semi-structured Database Group
Chen Yi Group & Zoe Lacroix Group

Workflow Project: Workflows analysis and adaptation in Scientific Explorations. We examined the problem of effectively reproducing the results of exploratory scientific workflow.

Awards and Honors

Schloss Dagstuhl - NSF Support Grant for Junior Researchers, *2018*.

MWSCAS The Myril B. Reed Best Paper Award, *2018*.

DFT Best Paper Nominee, *2017*.

DFT Best Student Paper Award, *2017*.

FPL Tools and Open-Source Community Service Award, *2011*.

MIT Presidential Fellowship, *2007*.

Publications & Presentations

Peer-reviewed Journals

[J10] L. Bu, M. Karpovsky and M. A. Kinsy: "Bulwark: Securing Implantable Medical Devices Communication Channels." **Computers and Security**, Elsevier, 2018.

[J9] L. Bu, M. Karpovsky and M. A. Kinsy: "Design of Reliable Storage and Compute Systems with Lightweight Group Testing Based Non-Binary Error Correction Codes." In the Institution of Engineering and Technology (**IET**) - Computers and Digital Techniques, 2018.

[J8] T. Yang, Y. Wei, Z. Tu, H. Zeng, M. Kinsy, N. Zheng and P. Ren: "Design Space Exploration of Neural Network Activation Function Circuits." In the Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD**), 2018.

[J7] L. Bu, J. Dofe, Q. Yu and M. Kinsy: "SRASA: A Generalized Theoretical Framework for Security and Reliability Analysis in Computing Systems." Journal of Hardware and Systems Security (**HaSS**) - Special Issue on Hardware Solutions for Cyber Security, 2018.

[J6] S. M. Sebt, A. Patooghy, H. Beitollahi and M. Kinsy: "Circuit Enclaves Susceptible to Hardware Trojans Insertion at Gate-Level Designs." In the Institution of Engineering and Technology (**IET**) - Computers and Digital Techniques, 2018.

[J5] L. Bu, M. Isakov and M. Kinsy: "A Secure and Robust Scheme for Sharing Confidential Information in IoT Systems." In the Elsevier Journal of **Ad Hoc Networks**, 2018.

[J4] M. Kinsy, L. Bu, M. Isakov, M. Mark: "Designing Secure Heterogeneous Multicore Systems from Untrusted Components." In **Cryptography**, June 2018.

[J3] P. Ren, M. Kinsy, and N. Zheng: "Fault-Aware Load-Balancing Routing for 2D-Mesh and Torus On-Chip Network Topologies." In the Transactions on Computers (**TC**), March 2016.

[J2] P. Ren, X. Ren, S. Sane, M. Kinsy, and N. Zheng: "Deadlock-Free and Connectivity-Guaranteed Methodology for Achieving Fault-tolerance in On-chip Networks." In the Transactions on Computers (**TC**), February 2016.

[J1] M. Kinsy, M. H. Cho, T. Wen, M. Lis , G. E. Suh, M. Dijk, and S. Devadas: "Optimal and Heuristic Application-Aware Oblivious Routing." In the Transactions on Computers (**TC**), January 2013.

Peer-Reviewed Conferences

[C37] A. Ehret, M. Isakov, and M. A. Kinsy: "Towards a Generalized Reconfigurable Agent Based Architecture: Stock Market Simulation Acceleration." In the 2018 International Conference on Reconfigurable Computing and FPGAs (**ReConFig**), December 2018.

[C36] M. Isakov, L. Bu, H. Cheng, and M. A. Kinsy: "Preventing Neural Network Model Exfiltration in Machine Learning Hardware Accelerators." In the 2018 Asian Hardware Oriented Security and Trust Symposium (**AsianHOST**), December 2018.

[C35] M. Isakov and M. A. Kinsy: "NoSync: Particle Swarm Inspired Distributed DNN Training." The 27th International Conference on Artificial Neural Networks (**ICANN'18**), October 2018.

[C34] L. Bu, H. Cheng, and M. A. Kinsy: "Hardware Assisted Adaptive Authentication Based on Lorenz Chaotic Systems." 2018 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT**), October 2018.

[C33] M. Isakov, A. Ehret, M. A. Kinsy: "Chameleon: A Generalized Reconfigurable Open-Source Architecture for Deep Neural Network Training." 2018 IEEE High Performance Extreme Computing Conference (**HPEC'18**), September 2018 Best Student Paper Candidate.

[C32] H. Cheng, L. Bu, and M. Kinsy: "Adaptive and Dynamic Device Authentication Based on Lorenz Chaotic Systems." In the 61st International Midwest Symposium on Circuits and Systems (**MWSCAS**), August 2018.

[C31] L. Bu and M. A. Kinsy: "Weighted Group Decision Making Using Multi-identity Physical Unclonable Functions." International Conference on Field-Programmable Logic and Applications (**FPL2018**), August 2018.

[C30] M. Isakov, A. Ehret and M. A. Kinsy: "ClosNets: Batchless DNN Training with On-Chip A Priori Sparse Neural Topologies." International Conference on Field-Programmable Logic and Applications (**FPL2018**), August 2018.

[C29] L. Bu, M. Mark and M. A. Kinsy: "A Short Survey at the Intersection of Reliability and Security in Processor Architecture Designs." IEEE Computer Society Annual Symposium on VLSI (**ISVLSI'18**), July 2018.

[C28] S. Kashi, A. Patooghy, D. Rahmati, M. Fazeli and M. A. Kinsy: "Application Specific Networks-on-Chip Synthesis: An Energy Efficient Approach." IEEE Computer Society Annual Symposium on VLSI (**ISVLSI'18**), July 2018.

[C27] E. Aerabi, A. Patooghy, H. Rezaei, M. Mark, M. Fazeli and M. Kinsy: "Mystic: Mystifying IP Cores Using an Always-ON FSM Obfuscation Method." IEEE Computer Society Annual Symposium on VLSI (**ISVLSI'18**), July 2018.

[C26] A. Ehret, P. Jamieson and M. A. Kinsy: "Scalable Open-Source Reconfigurable Architecture for Bacterial Quorum Sensing Simulations." International Symposium on Highly Efficient Accelerators and Reconfigurable Technologies (**HEART'18**), June 2018.

[C25] Bu and M. Kinsy: "Hardening AES Hardware Implementations Against Fault and Error Inject Attacks." In the 28th edition of the ACM Great Lakes Symposium on VLSI (**GLSVLSI**), May 2018.

[C24] K. Soleimani, A. Patooghy, N. Soltani, L. Bu, M. A. Kinsy: "Crosstalk Free Coding Systems to Protect NoC Channels Against Crosstalk Faults." In 2017 IEEE 35th International Conference on Computer Design (**ICCD**), November 2017.

[C23] J. R. Doppa, R. G. Kim, M. Isakov, M. A. Kinsy, H. Kwon and T. Krishna: "Adaptive Manycore Architectures for Big Data Computing." In the International Symposium on Networks-on-Chip (**NOCS**), October 2017

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[C22] L. Bu, H. D. Nguyen, and M. A. Kinsy: "RASSS: A perfidy-aware protocol for designing trustworthy distributed systems." In the 2017 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (**DFT**), October 2017 Best Student Paper Award and Best Paper Candidate.

[C21] E. Taheri, M. Isakov, A. Patooghy, and M. Kinsy: "Advertiser Elevator: a Fault Tolerant Routing Algorithm for Partially Connected 3D Network-on-Chips." In the 60th International Midwest Symposium on Circuits and Systems (**MWSCAS**) Aug 2017.

[C20] H. Hosseinzadeh, M. Isakov, M. Darabi, A. Patooghy, and M. Kinsy: "Janus: An uncertain cache architecture to cope with side channel attacks." In the 60th International Midwest Symposium on Circuits and Systems (**MWSCAS**) Aug 2017 The Myril B. Reed Best Paper Award.

[C19] M. Kinsy, S. Khadka and M. Isakov: "PreNoc: Neural Network based Predictive Routing for Network-on-Chip Architectures." In the 27th edition of the ACM Great Lakes Symposium on VLSI (**GLSVLSI**), May 2017.

[C18] M. Kinsy, S. Khadka, M. Isakov and A. Farrukh: "Hermes: Secure Heterogeneous Multicore Architecture Design." In the IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**), May 2017.

[C17] P. Ren, M. Kinsy, M. Zhu and N. Zheng: "Towards Connectivity-Guaranteed Power-gating Large-scale On-chip Networks", The 7th International Green and Sustainable computing conference (**IGSC**), Nov 7-9, 2016.

[C16] J. Mohr and M. Kinsy: "Securitas: Multi-Tenant Secure Computer Architecture." In the 40th Government Microcircuit Applications and Critical Technology Conference (**GOMACTech-15**), April, 2015.

[C15] M. Kinsy and S. Devadas: "Low-Overhead Hard Real-time Aware Interconnect Network Router." In IEEE High Performance Extreme Computing (**HPEC**), September, 2014.

[C14] M. Kinsy and S. Devadas: "Algorithms for Scheduling Task-based Applications onto Heterogeneous Many-core Architectures." In IEEE High Performance Extreme Computing (**HPEC**), September, 2014.

[C13] M. Kinsy, I. Celanovic, O. Khan, and S. Devadas: "MARTHA: Architecture for Control and Emulation of Power Electronics and Smart Grid Systems." In IEEE International Conference on Design, Automation and Test in Europe (**DATE**), March, 2013.

[C12] M. Kinsy, M. Pellauer, and S. Devadas: "Heracles: A Tool for Fast RTL-Based Design Space Exploration of Multicore Processors." In Proceedings of the 21st International Symposium on Field-Programmable Gate Arrays (**FPGA**), February 2013.

[C11] J. Poon, M. Kinsy, N. Pallo, S. Devadas, and I. Celanovic: "Hardware-in-the-loop testing for electric vehicle drive applications." In Proceedings of the 27th Annual IEEE Applied Power Electronics Conference and Exposition (**APEC**), February 2012.

[C10] M. Kinsy, O. Khan, I. Celanovic, M. Dusan, N. Celanovic, and S. Devadas: "Time-Predictable Computer Architecture for Cyber-Physical Systems: Digital Emulation of Power Electronics Systems." In Proceedings of the 32nd Real-Time Systems Symposium (**RTSS**), December 2011.

[C9] M. Kinsy, M. Pellauer, and S. Devadas: "*Heracles*: Fully Synthesizable Parameterized MIPS-Based Multicore System." In Proceedings of the 21st International Conference on Field Programmable Logic and Applications (**FPL**), September 2011. Tools and Open-Source Community Service Award

[C8] M. Lis, K. S. Shim, M. H. Cho, C. Fletcher, M. Kinsy, I. Lebedev, O. Khan, and S. Devadas: "Brief Announcement: Distributed Shared Memory based on Computation Migration." In Proceedings of the 23rd Symposium on Parallelism in Algorithms and Architectures (**SPAA**), June 2011.

[C7] M. Kinsy, D. Majstorovic, P. Haessig, J. Poon, N. Celanovic, I. Celanovic, and S. Devadas: "High-Speed Real-Time Digital Emulation for Hardware-in-the-Loop Testing of Power Electronics: A New Paradigm in the Field of Electronic Design Automation (EDA) for Power Electronics Systems." In Proceedings of the 2011 International Exhibition & Conference for Power Electronics, Intelligent Motion, Power Quality (**PCIM Europe**), May 2011.

[C6] M. Pellauer, M. Adler, M. Kinsy, A. Parashar, and J. Emer: "HAsim: FPGA-based high-detail multicore simulation using time-division multiplexing." In Proceedings of the 17th International Symposium on High Performance Computer Architecture (**HPCA**), February 2011.

[C5] M. H. Cho, M. Lis, K. S. Shim, M. Kinsy, T. Wen, and S. Devadas: "Oblivious Routing in On-Chip Bandwidth-Adaptive Networks." In Proceedings of the Parallel Architectures and Compilation Techniques (**PACT**), September 2009.

[C4] M. Kinsy, M. H. Cho, T. Wen, G. E. Suh, M. Dijk, and S. Devadas: "Application-Aware Deadlock-Free Oblivious Routing." In Proceedings of the International Symposium on Computer Architecture (**ISCA**), June 2009.

[C3] K. S. Shim, M. H. Cho, M. Kinsy, T. Wen, M. Lis , G. E. Suh, and S. Devadas: "A Comparison of Static and Dynamic Virtual Channel Allocation in Oblivious Routing." In Proceedings of the International Symposium on Networks-on-Chip (**NOCS**), May 2009.

[C2] M. H. Cho, C-C. Cheng, M. Kinsy, G. E. Suh, and S. Devadas: "Diastolic Arrays: Throughput-Driven Reconfigurable Computing." In Proceedings of the International Conference on Computer-Aided Design (**ICCAD**), November 2008.

[C1] M. Kinsy and Z. Lacroix: "Storing Efficiently Bioinformatics Workflows." In Proceedings of the 2007 IEEE International Symposium on Bioinformatics Bioengineering (**BIBE**), October 2007.

Peer-Reviewed Workshops

[W7] M. A. Kinsy, D. Kava, A. Ehret and M. Mark: "Sphinx: A Secure Architecture Based on Binary Code Diversification and Execution Obfuscation." Boston Area Architecture 2018 Workshop (**BARC18**), January 2018.

[W6] M. A. Kinsy, M. Isakov, A. Ehret and D. Kava: "SAPA: Self-Aware Polymorphic Architecture." Boston Area Architecture 2018 Workshop (**BARC18**), January 2018.

[W5] M. Isakov and M. A. Kinsy: "ClosNets: a Priori Sparse Topologies for Faster DNN Training." Boston Area Architecture 2018 Workshop (**BARC18**), January 2018.

[W4] M. Kinsy, R. Agrawal and H. Nguyen: "Fast Processing of Large Graph Applications Using Asynchronous Architecture." Boston Area Architecture 2017 Workshop (**BARC17**), January 2017.

[W4] M. Kinsy and S. Devadas: "Heracles 2.0: A Tool for Design Space Exploration of Multi/Many-core Processors." Workshop on the Intersections of Computer Architecture and Reconfigurable Logic (**CARL** 2012) Co-located with ISCA-39, June 2012.

[W3] M. H. Cho, M. Lis, K. S. Shim, M. Kinsy, and S. Devadas: "Path-Based, Randomized, Oblivious Routing." In Proceedings of the 2nd International Workshop on Network-on-Chip Architectures (**NoCArc'09**), December 2009.

[W2] Q. Shao, M. Kinsy and Y. Chen: "Storing and Discovering Critical Workflows from Log in Scientific Exploration." In Proceedings of the 2007 IEEE International Workshop on Scientific Workflows (**SWF**), July 2007.

[W1] M. Kinsy, Z. Lacroix, C. Legendre, P. Wlodarczyk, N. Yacoubi Ayadi: "ProtocolDB: Storing Scientific Protocols with a Domain Ontology." Lecture Notes in Computer Science by Springer-Verlag. **WISE** Workshops 2007: 17-28

Peer-reviewed Posters

[P4] R. S. Agrawal and M. A. Kinsy: "Adaptive-Approximate Cache Architecture." In the 3rd Career Workshop for Women and Minorities in Computer Architecture, held in conjunction with the 50th IEEE/ACM International Symposium on Microarchitecture **MICRO-50**), October 2017.

[P3] S. Khadka, S. Ergullu-Koehnen, B. Gravelle, and M. Kinsy: "Neural network based predictive routing for network-on-chip architectures." Work-in-Progress Presentation at 53rd Design Automation Conference (**DAC** 2016), June 2016.

[P2] P. Ren, M. Kinsy, C. Yang, B. Gravelle, S. Khadka, and N. Zheng: "Copal: Connectivity preserving algorithm for network-on-chip power-gating." Work-in-Progress Presentation at 53rd Design Automation Conference (**DAC** 2016), June 2016.

[P1] M. Kinsy, J. Poon, I. Celanovic, O. Khan, and S. Devadas: "A Multicore Architecture for Control and Emulation of Power Electronics and Smart Grid Systems Under Hard Real-Time Constraints." Work-in-Progress Presentation at 49th Design Automation Conference (**DAC** 2012), June 2012.

Reports

[R2] P. Ren, M. Kinsy, M. Zhu, S. Khadka, M. Isakov, A. Ramrakhyani, T. Krishna, and N. Zheng. "FASHION: Fault-Aware Self-Healing Intelligent On-chip Network." arXiv preprint arXiv:1702.02313, 2017.

[R1] M. Kinsy and R. Uhler: "SHA-3: FPGA implementation of ESSENCE and ECHO hash algorithm candidates using Bluespec." CSG-Report, CSAIL, MIT, May, 2009

Recent Invited Talks

Host Prof. Sherief Reda   *Designing Secure Heterogeneous Multicore Systems from Untrusted Components*, ECE Department, Brown University, 2017.

Workshop | 2017	*Secure Architecture Design*, 3rd Career Workshop for Women and Minorities in Computer Architecture - 50th IEEE/ACM International Symposium on Microarchitecture (MICRO-50), 2017.
Host Prof. V. Joyner Koomson	*A Scalable Asynchronous Architecture for Fast Processing of Large Graph Applications*, ECE Department, Tufts University, 2017.
Host Prof. Pengju Ren	*Asynchronous Architecture Design for Fast Processing of Large Graph Applications*, Institute of Artificial Intelligence and Robotics, Xi'an Jiaotong University, 2017.
Host Prof. Leibo Liu	*Self-Aware Polymorphic Computer Architecture Design*, Institute of Microelectronics, Tsinghua University, 2017.
Host Prof. Marten van Dijk	*Cyber-Physical Systems Security: Wearable and Implantable Devices*, ECE Department, University of Connecticut, 2016.
CyberSEED Conference	*Secure Heterogeneous Multicore Architecture Design*,Comcast Center of Excellence for Security Innovation, University of Connecticut, 2016.
Seminar	*Fast Processing of Large Graph Applications Using Asynchronous Architecture*, MIT LL Cyber Operations, Research and Engineering (CORE) Seminar Series - Division 5 , 2016.
Host Prof. Ronald Metoyer	*Secure Multicore Architecture Design*, ECE Department, University of Notre Dame, 2016.
Workshop	*Secure Multicore Architecture Design,*, Pacific Northwest Workshop on Securing Hardware Design and IC Supply Chains, sponsored by Mentor Graphics, Intel, and Galois, 2016.
Host Antonio de la Serna	*Cognitive-Approximate Architectures*, Draper Laboratory, 2015.
Workshop	*Hardware Level Computer Systems Security*, Oregon Cyber Security Day, University of Oregon, 2015.
Host Serge Leef	*Augur: A software-hardware co-design framework for efficient execution of binary code diversification*, Mentor Graphics, 2015.
Host Prof. Christof Teuscher	*MARTHA: A Cyber-Physical System Domain Architecture*, ECE Department, Portland State University, 2014.
Host Prof. Ronald Metoyer	*Adaptive and Polymorphic Computer Architectures*, ECE Department, Oregon State University, 2014.

Major Software Released

BRISC-V	Open Source Architectural Design Space Exploration Toolbox around the RISC-V ISA (Link: `http://ascslab.org/research/briscv/index.html`.
ABAQS	Agent Based Architecture for Quorum sensing Simulation (Link: `http://ascslab.org/research/abc/abaqs/index.html`.
Heracles	A Tool for Fast RTL-Based Design Space Exploration of Multicore Processors (Link: `http://projects.csail.mit.edu/heracles/`.

Research Sponsors

External	National Science Foundation (NSF)
External	Defense Advanced Research Projects Agency (DARPA)
External	MIT Lincoln Laboratory
External	Altera Corporation - Equipment and software licenses
External	Xilinx Corporation - Equipment and software licenses
External	Intel Corporation - Equipment
Internal	Division of Equity and Inclusion, University of Oregon
Internal	Incubating Interdisciplinary Initiatives, University of Oregon

Student Advisees

Current Advisees

Ph.D	Lake Bu, Electrical and Computer Engineering, Boston University
Ph.D	Mihailo Isakov, Electrical and Computer Engineering, Boston University
Ph.D	Alan Ehret, Electrical and Computer Engineering, Boston University
Ph.D	Miguel Mark, Electrical and Computer Engineering, Boston University
Ph.D	Rashmi Agrawal, Electrical and Computer Engineering, Boston University
Ph.D	Novak Boskov, Electrical and Computer Engineering, Boston University
M.S.	Donato Kava, Electrical and Computer Engineering, Boston University
M.S.	Sahan Disanayake Mudiyanselage, Electrical and Computer Engineering, Boston University

Graduated Advisees

M.S. 2018	Shreeya Khadka, Electrical and Computer Engineering, Boston University - NVIDIA Corporation
M.S. 2018	Hien Nguyen, Electrical and Computer Engineering, Boston University - JDA Software
M.S. 2017	Rashmi Agrawal, Electrical and Computer Engineering, Boston University. M.S. Project: Adaptive-Approximate Cache Architecture - Intel Corporation
M.S. 2016	Joseph Mohr, Computer and Information Science, University of Oregon. M.S. Project: Securitas: Multi-Tenant Secure Computer Architecture - University of Oregon
B.S 2017	Haley Whitman, University of Oregon
B.S. 2017	Andrew Hill, University of Oregon
B.S. 2015	Jack Ziesing, University of Oregon

Research Mentoring Activities

2018-Present	Dr. Hai Cheng, Visiting Research Fellow
2017-2018	Dr. Ahmad Patooghy, Postdoctoral Fellow - Assistant Professor at the University of Central Arkansas

2017-2018	Miguel Mark, Research Assistant
2015-2016	Dr. Christopher Dudley, Research Fellow
2014-2016	Jacob Riddle, Research Assistant
2014-2015	Sena Ergullu Koehnen, Research Assistant
2015-2016	Piotr Esden-Tempski, Research Assistant

Student Research Support

Departmental Level

Defended August 2017	Jiayi Sheng, Ph. D. Dissertation Committee, Dept. of Electrical and Computer Engineering, Boston University
Defended August 2017	Ryan Silva, Ph. D. Dissertation Committee, Dept. of Electrical and Computer Engineering, Boston University
Defended April 2017	Zafar Takhirov, Ph. D. Dissertation Committee, Dept. of Electrical and Computer Engineering, Boston University
Defended December 2016	Tiansheng Zhang, Ph. D. Dissertation Committee, Dept. of Electrical and Computer Engineering, Boston University
Defended September 2017	Anmol Gupta, M.S. Thesis Committee, Dept. of Electrical and Computer Engineering, Boston University
2016	Chad Wood, Directed Research Project Committee Member, Dept. of Computer and Information Science, University of Oregon
2016	Sabin Kafle, Directed Research Project Committee Member, Dept. of Computer and Information Science, University of Oregon
2015	Robert Lim, Directed Research Project Committee Member, Dept. of Computer and Information Science, University of Oregon
2015	Kanika Sood, Directed Research Project Committee Member, Dept. of Computer and Information Science, University of Oregon
2014-2016	Hao Wang, Dissertation Advisory Committee Member, Dept. of Computer and Information Science, University of Oregon
2014-2015	Amir Farzad, Dissertation Advisory Committee Member, Dept. of Computer and Information Science, University of Oregon

College Level

Defended May 2016	Bryson Nakamura, Ph. D. Dissertation Committee, Dept. of Human Physiology, University of Oregon
2015-2016	Brittany White, Ph. D. Dissertation Committee, Dept. of Biochemistry and Chemistry, University of Oregon

Teaching Experience

Graduate Level Courses

Fall 2018
EC 700: Hardware and Systems Security, *Boston University, College of Engineering*.
In-depth inspection of the role that hardware security plays in cybersecurity and computer hardware related attacks and defense in computing systems. The topics covered are: classic and Modern encryption algorithms, integrity and authentication, key distribution and management, hardware Trojans, side-channel attacks, fault attacks, hardware counterfeiting, oblivious RAM, digital signatures, circuit obfuscation, trust platform modules, physical unclonable functions, true random number generators, and secure architecture designs. The class project consists of building secure multi-core RISC-V ISA architecture. `http://ascslab.org/courses/ec700/index.html`.

Spring 2018
EC 513: Computer Architecture, *Boston University, College of Engineering*.
Examination of the evolution and the principles underlying modern computer architectures. It emphasizes the fundamental relationship between technology, hardware organization, and programming systems. Topics covered include processor micro-architecture, instruction set design, pipelined, out-of-order, and speculative execution, superscalar, very long instruction word (VLIW), vector, and multithreaded processors, cache and virtual memory organizations, synchronization, memory models, and cache coherence protocols for multiprocessors, multithreaded architectures, multiprocessor interconnection networks, and embedded systems. `http://ascslab.org/courses/ec513/index.html`.

Winter 2016 | Fall 2014
CIS 429/529: Computer Architecture, *University of Oregon, Dept. of Computer and Information Science*.
The objectives are to provide students a strong understanding of modern computing systems. The class has roughly 30 students and includes both senior undergraduate and graduate students.

Spring 2015 | Spring 2016
CIS 407/507: Complex Digital System Design, *University of Oregon, Dept. of Computer and Information Science*.
The course introduces architecture and design concepts underlying modern complex VLSIs and system-on-chips. The class has senior undergraduate and graduate students from the Computer and Information Science and Physics departments.

IAP 2012
6.S918: Design and Exploration of Multicore Systems with Heracles - Instructor, *Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science*.
The goal in the class is to perform multi-core and many-core architectures design space exploration using the Heracles Multicore System infrastructure. We examine different implementation choices: core micro-architecture, levels of caches, cache sizes, routing algorithm, router micro-architecture, distributed or shared memory, or network interface, and evaluate their impact on the overall system performance. `http://stellar.mit.edu/S/course/6/ia12/6.S918/`.

Fall 2009
6.823: Computer System Architecture - Teaching Assistant, *Massachusetts Institute of Technology, Dept. of Electrical Engineering and Computer Science*.
A graduate class on the evolution of computer architecture and the factors influencing the design of hardware and software elements of computer systems. Assisted in designing quizzes, retooling problem sets, leading weekly recitation section, and grading. `http://csg.csail.mit.edu/6.823/`.

Undergraduate Level Courses

Fall 2017 **EC 413: Computer Organization**, *Boston University, College of Engineering*.
Introduction to the fundamentals and design of computer systems. Topics covered include computer instruction sets, assembly language programming, arithmetic circuits, CPU design (data path and control, pipelining), performance evaluation, memory devices, memory systems including caching and virtual memory, and I/O. A single-cycle RISC processor design project using design automation tools. The class has roughly 60 students. Instructor Rating: 4.04/5.0 - 45 student participants. `http://ascslab.org/courses/ec413/index.html`.

Fall 2017 **EK100: Freshmen Seminar**, *Boston University, College of Engineering*.
First-year experience course that introduces students to Boston University, the College of Engineering, and the field of engineering.

Fall 2016 **EK131/132: Introduction to Engineering**, *Boston University, College of Engineering*.
The class introduces students to engineering analysis and design. Topics covered in the class include: introduction to analog and digital systems, binary number system, electronic components, RC circuit, circuit analysis, combinational and sequential circuits, micro-control design, and system programming. `http://ascslab.org/courses/ek132/index.html`.

Fall 2015 **CIS 314: Computer Organization**, *University of Oregon, Dept. of Computer and Information Science*.
This course covers the basics of computer organization with emphasis on register-level computer organization, instruction set architecture, and assembly language programming. The class has roughly 75 undergraduate students.

Student Teaching Support

Fall 2017 **EC 444 Smart and Connected Systems**, *Boston University, College of Engineering*.
Led the efforts in the conception of the course with Profs. David Starobinski and Thomas Little, under the college's Future of Undergraduate Engineering Education Task Force.

Service

Internal

Department Level.

2017 - 2018	Dept. of Electrical and Computer Engineering, Masters Program Committee
2017 - 2018	Dept. of Electrical and Computer Engineering, Faculty Search Committee
2016 - 2017	Dept. of Electrical and Computer Engineering, PhD Committee
2016 - 2017	Dept. of Electrical and Computer Engineering, Faculty Search Committee
2015 - 2016	Dept. of Computer and Information Science, University of Oregon, Graduate Education Committee
2014 - 2016	Dept. of Computer and Information Science, University of Oregon, Computing Resources Committee
2014 - 2015	Dept. of Computer and Information Science, University of Oregon, Colloquium Chair

College Level.

2016 - 2017	College of Engineering, Future of Undergraduate Engineering Education Task Force

2015 - 2016	University of Oregon, Incubating Interdisciplinary Initiatives (I3) Review Committee
2014 - 2016	University of Oregon, Regional Accelerator and Innovation Network at UO Advisory
2014 - 2016	University of Oregon, University Venture Development Fund program - Leadership Team

External

Conference Organizing Committee.

2019	24rd ACM International Conference on Architectural Support for Programming Languages and Operating Systems(**ASPLOS**) Publicity Co-Chair.
2018	IEEE International Conference on Computer Design (**ICCD**) Registration Co-Chair.
2018	IEEE Computer Society Annual Symposium on VLSI (**SVLSI**), Co-Organizer of Special Session: Shall We Jointly Address VLSI Reliability and Security?
2017	50th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO-50**) Registration Chair.
2017	IEEE Symposium on Neuromorphic Cognitive Computing (**SNCC**), Co-Organizer of Special Session: Design Methods, Tools and Examples for FPGA-Based Acceleration of Artificial Neural Network.

Conference Session Chair.

2018	IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**). Session 2: Physical Attacks and Tamper Resistance
2017	IEEE International Conference on Computer Design (**ICCD**). 9B: Novel Architecture with 3D and Flash Memory
2017	60th IEEE International Midwest Symposium on Circuits and Systems (**MWSCAS**). 11.2 Trusted Microelectronics Track

Conference Review Committee.

2019	International Symposium on High Performance Computer Architecture (**HPCA**)
2018	IEEE/ACM International Conference on Computer-Aided Design (**ICCAD**).
2018	IEEE International Conference on High Performance Computing, Data, and Analytics (**HiPC**).
2018	Asian Hardware Oriented Security and Trust Symposium (**AsianHOST**).
2018	IEEE International Symposium on Hardware Oriented Security and Trust (**HOST**).
2018	ACM Great Lakes Symposium on VLSI (**GLSVLSI**).
2018	IEEE High Performance Extreme Computing (**HPEC**).
2017	IEEE/ACM International Symposium on Microarchitecture **MICRO-50**).
2017	International Conference for High Performance Computing, Networking, Storage and Analysis (**Supercomputing - SC**) - Architectures and Networks Program Committee.
2017, 2016, 2015	IEEE International Conference on Computer Design (**ICCD**).
2018, 2017	IEEE International Midwest Symposium on Circuits and Systems (**MWSCAS**).

2017	IEEE International Parallel and Distributed Processing Symposium (**IPDPS**).
2015	ACM Richard Tapia Celebration of Diversity in Computing Conference.

Journal Review Committee.

2018	IEEE Transactions on Very Large Scale Integration Systems (**TVLSI**).
2017, 2016	ACM Transactions on Reconfigurable Technology and Systems (**TRETS**).
2016	IEEE Transactions on Computers (**TC**).
2016	IEEE Transactions on Parallel and Distributed Systems (**TPDS**).
2018, 2016	ACM Transactions on Architecture and Code Optimization (**TACO**).

Grant Review Panels.

2015	US Department of Energy SBIR Proposals.

Outreach Activities

Summer 2017	Summer Challenge: Electrical Engineering - For high school students as part of the Boston University Summer Program.
Summer 2016	Undergraduate Research in Hardware Security - University of the Virgin Islands Summer Mainland Visiting Program
Summer 2015	Introduction to Computer Science - For high school students as part of the Oregon Young Scholars Program.
Spring 2015	Computer Science Workshop - African American Rites of Passage Program, University of Oregon.

References

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