Chia-Hsin (Amy) Chen

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Research Interests

Computer Architecture, On-Chip Networks

Education

Massachusetts Institute of Technology, USA — Sep. 2009 – Present

Ph.D. Candicate in Electrical Engineering and Computer Science (GPA 5.0/5.0) Advisor: Li-Shiuan Peh

Thesis: Design and implementation of Low-latency/Low-power Reconfigurable On-Chip Networks

Expected graudation date: August 2016

Princeton University, USA (transferred to MIT) — Sep. 2008 – Aug. 2009

Ph.D. Student in Electrical Enginnering Advisor: Li-Shiuan Peh

National Taiwan University, Taiwan (R.O.C.) — Sep. 2004 – June 2007

B.S. in Electrical Engineering (GPA 4.0/4.0)

Key Research Experiences

SMART: ultra-low latency network design and tapeout, MIT — Feb. 2012 – Present

- Co-designed network reconfiguration techniques that setup virtual multi-hop bypass paths to allow single-cycle multi-hop traversals to dramatically reduce the packet delivery latency.
- Implemented a test-chip with 64 routers and on-chip testers in IBM 32nm SOI technology.

SCORPIO: 36-core shared-memory processor tapeout, MIT — Nov. 2011 – Dec. 2015

- Co-designed a novel network architecture that supports global ordering for broadcast messages on an unordered mesh interconnect.
- Co-implemented a multicore prototype chip with 36 in-order cores and the proposed network design in IBM 45nm SOI technology.

Low-power crossbar generator, MIT — Oct. 2010 – Apr. 2011

- Designed and implemented a low-voltage-swing crossbar generator to enable low-power datapath design flow from synthesis to layout.

Low-power broadcast-enabled NoC tapeout, MIT — Mar. 2010 – June 2010

- Co-designed broadcast-enabled router that improves the performance and lowers energy consumption.
- Co-implemented a test-chip with 16 broadcast-enabled routers in IBM 45nm SOI technology.

DSENT: Design space exploration of NoC tool, MIT — Sep. 2010 – Nov. 2010

- Co-designed and implemented a fast modeling tool to evaluate the power/timing/area cost of opto-electrical network for rapid design space exploration.

Evaluation of express topologies, Princeton University and MIT — Mar. 2009 – Dec. 2009

- Evaluated and compared mesh network designs that use virtual or physical express channels to improve performance under realistic system constriants.

Computer Skills

- Programming: C/C++, CUDA, VB.NET, C#.NET, Python, Ruby, TCL, Cadence SKILL
- Parallel processing: MPI, OpenMP, CUDA
- Circuit design: SystemVerilog, Verilog, Spice, Layout
- Tool: HSPICE, Virtuoso, SoC Encounter, Design Compiler, CACTI, ORION, gem5

Publications (Computer Architecture)

1. M. K. Papamichael, C. Cakir, C. Sun, C.-H. Chen, J. C. Ho, K. Mai, L.-S. Peh, V. Stojanovic, "**DELPHI: a framework for RTL-based architecture design evaluation using DSENT models**," *Symp. on Performance and Analysis of Systems and Software (ISPASS), 2015*

2. C.-H. Chen, S. Park, S. Subramanian, T. Krishna, B. K. Daya, W.-C. Kwon, B. Wilkerson, J. Arends, A. P. Chandrakasan, L.-S. Peh, "**SCORPIO: 36-Core Shared Memory Processor – Demonstrating Snoopy Coherence on a Mesh Interconnect**," *Symp. on High Performance Chips (HotChips), 2014*

3. B. K. Daya, C.-H. Chen, S. Subramanian, W.-C. Kwon, S. Park, T. Krishna, J. Holt, A. P. Chandrakasan, L.-S. Peh, "**SCORPIO: A 36-core research chip prototype demonstrating snoopy coherence on a scalable mesh NoC with in-network ordering**," *Proc. of International Symposium on Computer Architecture (ISCA), 2014*

4. T. Krishna, C.-H. Chen, W.-C. Kwon, L.-S. Peh, "**SMART: Single-Cycle Multi-Hop Traversals Over A Shared Network-on-Chip**," *Special Issue of IEEE Micro, Top Picks from the Computer Architecture Conferences, 2014*

5. T. Krishna, C.-H. Chen, S. Park, W.-C. Kwon, S. Subramanian, A. P. Chandrakasan, L.-S. Peh, "**Single-Cycle Multihop Asynchronous Repeated Traversal: A SMART Future for Reconfigurable On-Chip Networks**," *IEEE Computer, October 2013*

6. C.-H. Chen, S. Park, T. Krishna, S. Subramanian, A. P. Chandrakasan, L.-S. Peh, "**SMART: A Single-Cycle Reconfigurable NoC for SoC Applications**," *Prof. of Design Automation and Test in Europe (DATE), 2013*

7. T. Krishna, C.-H. Chen, W.-C. Kwon, L.-S. Peh, "**Breaking the On-Chip Latency Barrier Using SMART**," *Proc. of International Symposium on High-Performance Computer Architecture (HPCA), 2013*

8. S. Park, T. Krishna, C.-H. Chen, B. K. Daya, A. P. Chandrakasan, L.-S. Peh, "**Approaching the Theoretical Limits of a Mesh NoC with a 16-Node Chip Prototype in 45nm SOI**," *Prof. of Design Automation Conference (DAC), 2012*

9. P. Koka, M. O. McCracken, H. Schwetman, C.-H. Chen, X. Zheng, R. Ho, K. Raj, A. V. Krishnamoorthy, "**A Micro-architectural Analysis of Switched Photonic Multi-chip interconnects**," *Prof. of International Symposium on Computer Architecture (ISCA), 2012*

10. G. Kurian, C. Sun, C.-H. Chen, J. E. Miller, L. Wei, J. Michel, D. Antoniadis, L.-S. Peh, L. C. Kimerling, V. Stojanovic, A. Agarwal, "**Cross-layer Energy and Performance Evaluation of a Nanophotonic Manycore Processor System using Real Application Workloads**," *Prof. of International Parallel and Distributed Processing Symposium (IPDPS), 2012*

11. C. Sun, C.-H. Chen, G. Kurian, L. Wei, J. Miller, A. Agarwal, L.-S. Peh, V. Stojanovic, "**DSENT – A Tool Connecting Emerging Photonics with Electronics for Opto-Electronic Networks-on-Chip Modeling**," *Prof. of International Symposium on Networks-on-Chip (NOCS), 2012*

12. C.-H. Chen, S. Park, T. Krishna and L.-S. Peh, "**A Low-Swing Crossbar and Link Generator for Low-Power Networks-on-Chip**," *Prof. of International Conference on Computer-Aided Design (ICCAD), 2011*

13. K. Aisopos, C.-H. Chen and L.-S. Peh, "**Enabling System-Level Modeling of Variation-Induced Faults in Networks-on-Chip**," *Prof. of Design Automation Conference (DAC), 2011*

14. C.-H. Chen, N. Agarwal, T. Krishna, K.-H. Koo, L.-S. Peh, K. C. Sarawat, "**Physical vs. Virtual Express Topologies with Low-Swing Links for Future Many-core NoCs**," *Prof. of International Symposium on Networks-on-Chip (NOCS), 2010*

Selected Publications (Cryptography and Security)

1. C.-H. Chen, C.-W. Chen, C. Kuo, Y.-H. Lai, J. McCune, A. Studer, A. Perrig, B.-Y. Yang, T.-C. Wu, "**GAnGS: Gather, Authenticate 'n Group Securely**," *Proc. of International Conference on Mobile Computing and Networking (Mobicom), 2008*

2. A. I.-T. Chen, C.-H. Chen, M.-S. Chen, C.-M. Cheng, B.-Y. Yang, "**Practical-Sized Instances of Multivariate PKCs: Rainbow, and lIC-derivatives**," *Prof. of Post-Quantum Cryptography Workshop (PQCrypto), 2008*

3. J. Ding, V. Dubois, B.-Y. Yang, C.-H. Chen, C.-M. Cheng, "**Can SFLASH be saved?**," *Prof. of International Colloquium on Automata, Language and Programming (ICALP), 2008*

4. C.-H. Chen, M.-S. Chen, J. Ding, F. Werner, B.-Y. Yang, "**Odd-Char Multivariate Hidden Field Equations**," *IACR Cryptology ePrint Archive, 2008*

5. J. Ding, B.-Y. Yang, C.-H. Chen, M.-S. Chen, C.-M. Cheng, "**New Differential-Algebraic Attacks and Reparametrization of Rainbow**," *Prof. of Applied Cryptography and Network Security Conference (ACNS), 2008*

6. B.-Y. Yang, C.-H. Chen, D. J. Bernstein, J.-M. Chen, "**Analysis of QUAD**," *Prof. of Fast Software Encryption workshop (FSE), 2007*,

7. J. Ding, B.-Y. Yang, C.-M. Cheng, C.-H. Chen, V. Dubois, "**Breaking the Symmetry: a Way to Resist the New Differential Attack**," *IACR Cryptology ePrint Archive, 2007*

8. C.-H. Chen, B.-Y. Yang, J.-M. Chen, "**The Limit of XL Implemented with Sparse Matrices**," *Prof. of International Workshop on Post-Quantum Cryptography (PQCrypto), 2006*

Industry Experiences

Design space exploration of optical NoC, Oracle Sun Lab, Austin, TX June 2011 – Aug. 2011

Mentors: Herb Schwetman, Pranay Koka, Michael Mccracken

- Developed detailed on-chip network performance simulator using CSIM framework to evaluate different opto-electric NoC.

High-radix router delay/power/area modeling, HP Labs, Palo Alto, CA June 2009 – Aug. 2009

Mentors: Jung Ho Ahn, Nathan Binkert, Naveen Muralimanohar

- Built a tool enabling architectural level design for networks with high-radix routers.
- Integrated CACTI (a widely used SRAM delay/power/area modeling) and Orion (a low-radix router power/area simulator). Introduced a modular program structure to enhance simulation flexibility.

Relevant Courses

- On-Chip Networks, Advanced Computer Architecture, Optical Networks, Computer Networks
- Compiling Techniques, Data Structures, Algorithms
- Design and Analysis of Digital Integrated Circuits, Low Power IC and System Design, Ultra Low Power Bioelectronics
- Stochastic Processes, Cryptography