A New Ringing Detection Based Adaptive Video Scaler with Parallel Memory Architecture

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***Abstract*-This paper proposes a novel video scaler which uses an adaptive polyphase digital filter for image interpolation and possesses a new efficient memory architecture for image data buffering. The proposed adaptive image scaling algorithm is superior to that of bicubic algorithm in preserving details and suppressing ringing artifacts. The new memory architecture, which helps minimize the computational logic and memory usage, significantly simplifies the VLSI design of the scaler. The video scaler can therefore be used independently in any low cost, rational factor image scaling applications without any additional post processing procedures or frame buffering memories.**

I. INTRODUCTION

Video scaler has become extremely important in multimedia applications (e.g. HDTV, game box, digital camera, mobile phone), not only because of the emerging various resolutions of image sources (e.g. QVGA, WXGA, 1080i, 1080p), but also different sizes of display terminals [1, 2]. A popular technique in video scaling is polyphase FIR based filtering algorithm [3-5], this technique could obtain very sharp image than traditional methods (e.g. bilinear and bicubic interpolation); however the ringing artifact is noticeable. Several post processing methods have been studied to remove such ringing artifacts, but most of the proposed algorithms involve complicated calculations which are not apt for hardware implementation. To solve this problem, we propose a new hardware friendly adaptive polyphase structure digital filtering method that can gain very clear images at the same time introduces few ringing artifacts without any post processing needs. In addition, we also propose a new efficient memory architecture which reduces both the cost and complexity of the hardware implementation.

II. Adaptive image scaling algorithm

From the digital signal processing point of view, image scaling can be formulated in terms of a linear filtering operation [6], which is usually defined as below:

$$y(m) = \sum_{n=-\infty}^{\infty} g_m(n)\, x\left(\left\lfloor \frac{mM}{L} - n \right\rfloor\right) \qquad (1)$$

where $g_m(n) = h(nL + mM \oplus L)$, for all m and n, denotes the unit sample response of the digital filter, L and M are the up and down scaling rate.

The key point of this technique is to find the proper low pass filter $h(n)$. The use of a low pass FIR filter will inevitably cause blur and ringing artifacts in the same time, so one has always to compromise between fine details and ringings. Although many post processing techniques could remarkably eliminate the ringing artifacts [3, 7-9], these algorithms usually require complicated mathematical calculations such as multiply, square and sorting, which made them too cost expensive to implement in hardware.

The new idea we proposed, which avoids the necessity of post processing for ringing reduction, is that we selectively change the low pass filter coefficients according to the property of the image contents during the filtering process. Due to the perspective of human visual system [10], the ringing artifact is only prominent in the finite isotropic smooth regions around sharp edges or details. Based on this concept, our strategy is: firstly classify the image pixels into two categories-the smooth regions where ringing artifact may become visible after scaled, which are referred as the "ringing areas", and the rest part of the image. Secondly, we process these ringing areas with a interpolation filter which introduces un-noticeable ringings and the others with a sharper filter which preserves more high frequency contents. Then we can get a scaled image with fine details and few ringings.

The proposed scaler architecture is schematically shown in Fig. 1.

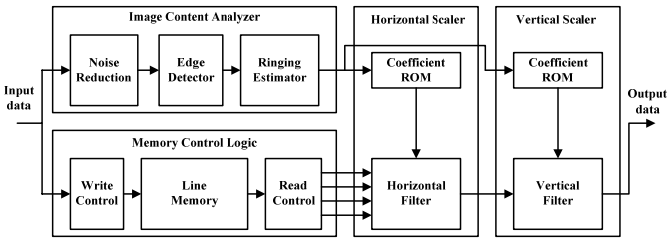
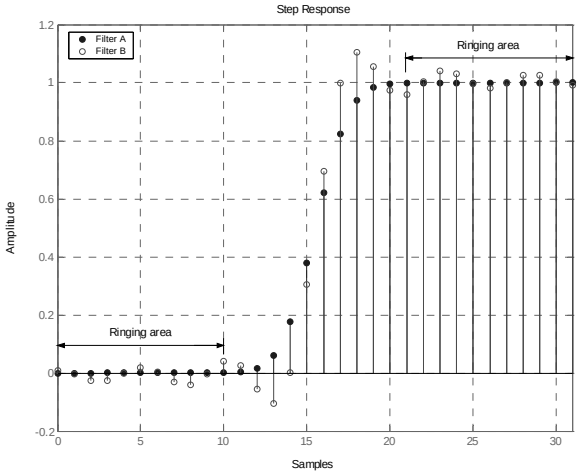


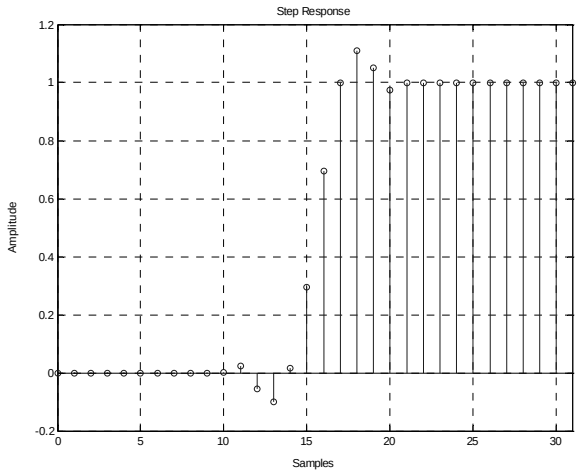
Fig. 1 Proposed Scaler Architecture

To illustrate how our filtering algorithm works, we demonstrate a simplified one dimensional case as Fig. 2 shows. Fig. 2(a) is the step response of the two complementary digital filters we used: Filter A with very small ringings and Filter B with steep transition band around edges. The step response can be regarded as a processed strong edge in images. Therefore, if the pixels in the ringing area are processed by Filter A and the edge pixels are

processed by Filter B, we can get a clear image with sharp edges and free of ringing artifacts, shown in Fig. 2(b).



(a) Step response of the two filters we used



(b) The combined filtering result

Fig. 2 Illustration of proposed algorithm

The image content classification procedure is performed under following steps:

1. Edge detection. This step aims to detect and locate salient edges and other strong fine detail contents present in the input image.
2. Ringing area estimation. After getting the raw edge map, we perform a binary dilation operation to mark the ringing support region around the edges and then perform an ex-or operation by using the generated raw edge map and the raw ringing area map to get the final ringing map, shown in Fig. 3(c), which is used to conduct the filtering process afterwards.

The experiment results are shown in Fig. 3. We performed a 2.5 ratio up-scaling using the "camera man" and "lena" images in both width and height. As you can see, Fig. 3(d) is clear than Fig. 3(c) and ringing doesn't exit in Fig. 3(d).

III. A new parallel memory architecture for data arrangement

There are two major hardware implementation architectures of video scaler according to whether the scaler is bi-directional, which means it could perform both up and down scaling algorithms, or one-directional, which means it could only perform up or down scaling. Traditional architecture of an up-down scaling video scaler usually has to separate the horizontal up scaling unit and down scaling unit with a line memory block [11], because a data rate difference lies between the input and output data stream. This kind of architecture has redundant control and computation logic, since the up and down scaling circuits are mutually transposable [6]. On the other hand, for one-directional scaler [12], extra FIFOs are needed for picking up the final valid data from the raw data stream before the final output port. To reduce the logic and memory usage in the hardware implementation, we propose a parallel memory structure, shown in Fig. 4, by using which we can combine the horizontal up scaling procedure with the down scaling procedure into one unit and omit the additional data buffering FIFOs.

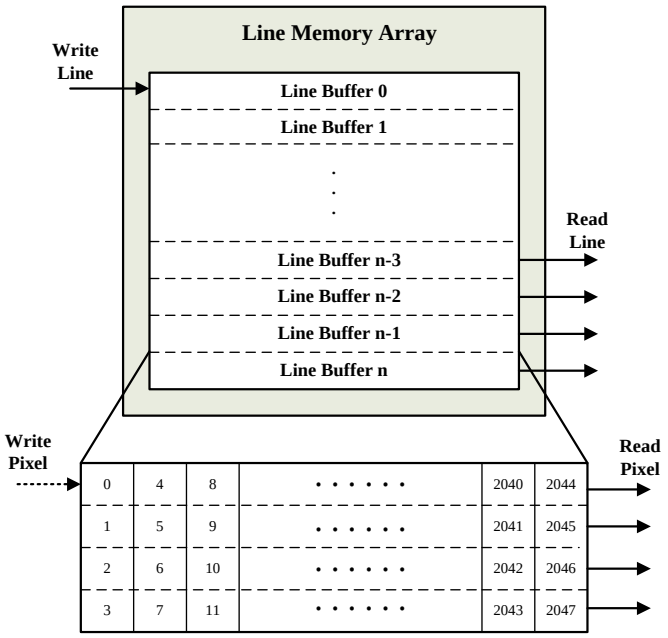


Fig. 4 Memory architecture

According to (1), if the interpolation filter is implemented in a polyphase structure, the coefficient length of each phase $g_m(n)$ is defined as:

$$R = \frac{N}{L} \tag{2}$$

where N is the length of $h(n)$.

Fig. 4 shows how the buffering memories are arranged in a parallel way when $R = 4$. We can see from Fig. 4, the writing and reading procedure is separated by a fix time

interval which promises no confliction in memory accessing. The horizontal interpolation can now be performed in a parallel way in one single clock domain, and only the wanted pixels are calculated which guarantees no more following data FIFOs are needed.

IV. Conclusion

In this paper, we present a new polyphase FIR based video scaler, which adaptively changes its filter coefficients according to the image content to maintain a good balance between blur and ringing. The result of the proposed method is clearer than bicubic, which is one of the best solutions among the present image scaling algorithms. Also, the proposed line memory architecture is efficient in data buffering and logic resource saving, which reduces the die size of the VLSI implement. Therefore, the proposed video scaler can be used in any low cost, high performance video display terminals without additional post processing costs.

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(a) Original image

(b) Detected ringing area

(c) Up-scaling result by bicubic

(d) Up-scaling result by proposed algorithm

(e) Up-scaling result by bicubic

(f) Up-scaling result by proposed algorithm

Fig. 3 Experiment result (ratio 1:2.5)