

Fast Statistical Analysis of Rare Circuit Failure Events in High-Dimensional Variation Space

Carnegie Mellon

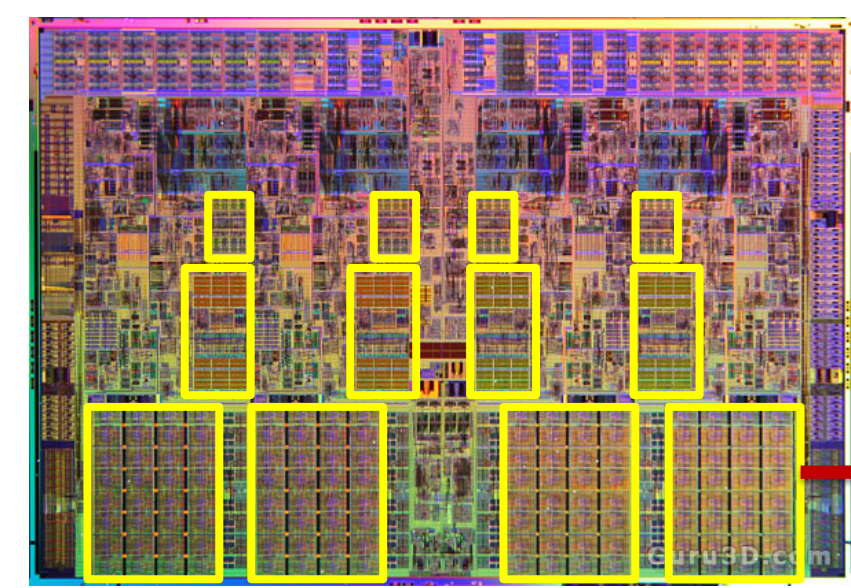
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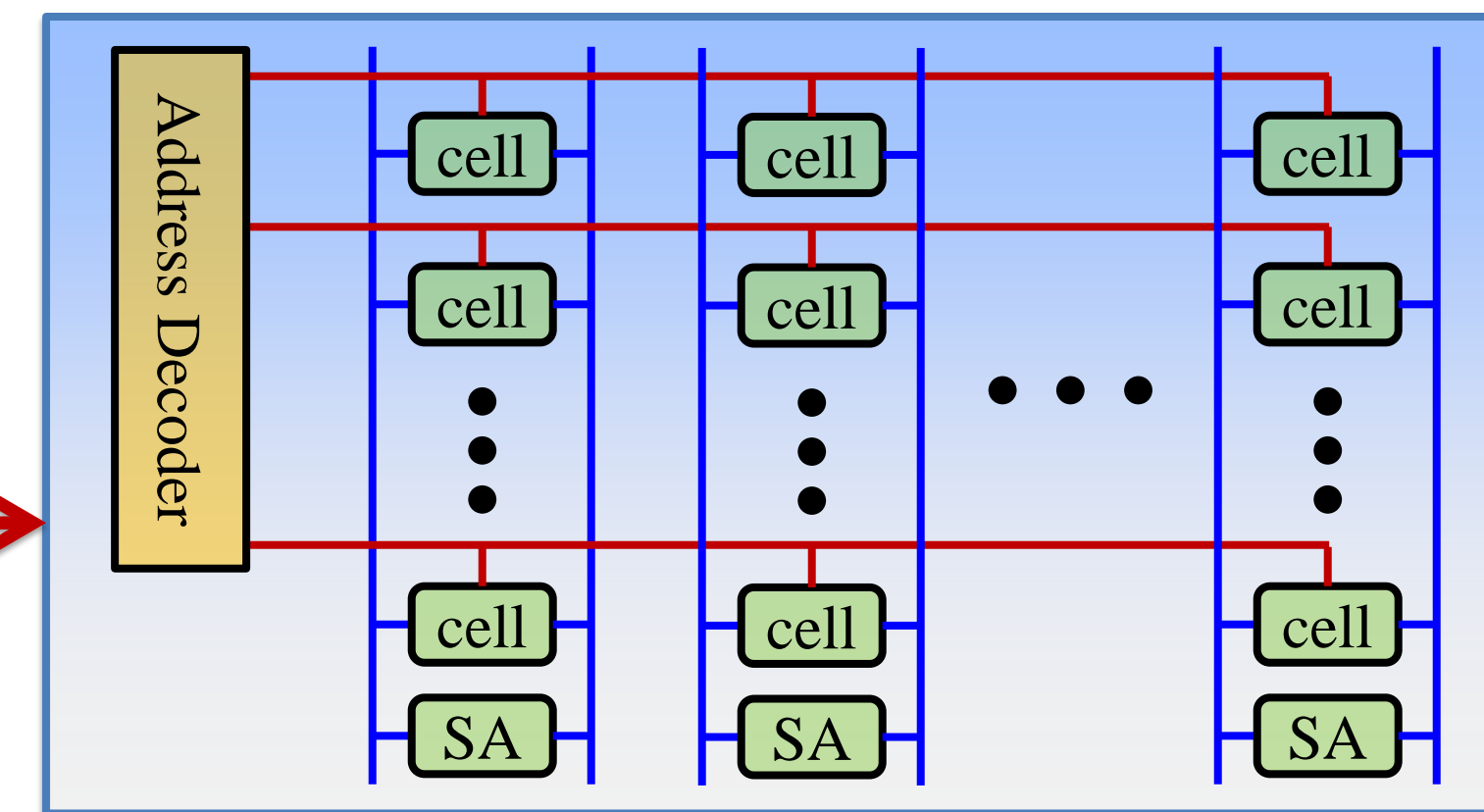
Electrical & Computer ENGINEERING

Motivation

✓ **Scaling:** a large number of replicated components are integrated on the chip

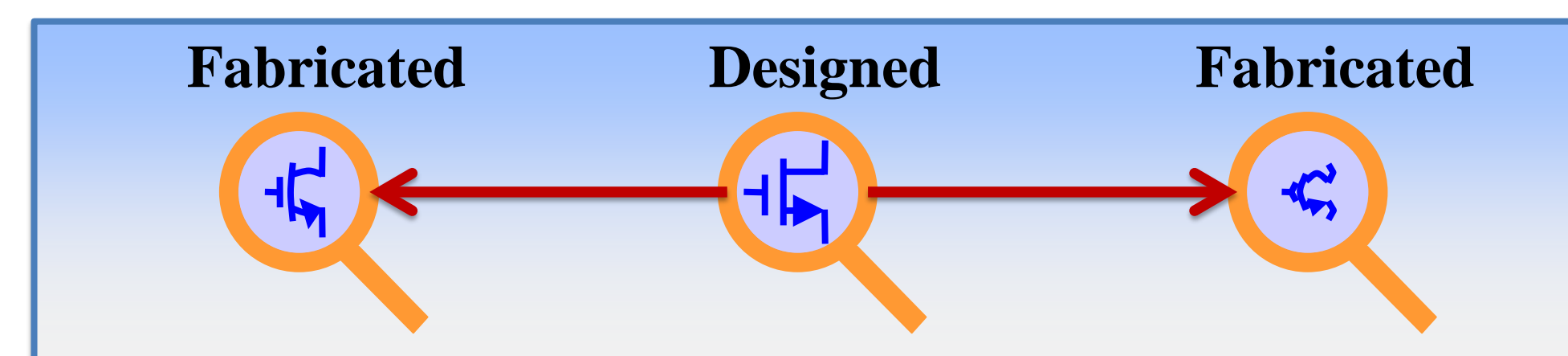


45nm Intel® Core™ i7 Processor



Simplified SRAM Architecture

✓ **Challenge:** all the components need to function correctly under large process variations



Process Variation

✓ **Yield requirement:** each component must be extremely robust under process variations

- The failure event of each component must be rare

✓ **Time to market:** fast statistical tools are highly desired to analyze the rare failure event

Existing Approaches

✓ **Brute-force Monte Carlo (MC)** [1]

- Pros: no dimensionality issue
- Cons: **not efficient**

✓ **Importance sampling (IS)** [2]: bias the sampling distribution

- Pros: efficient in low-D space
- Cons: difficult to find an appropriate biased sampling distribution in **high-D** space

✓ **Statistical blockade** [3]: classifier based

- Pros: efficient in low-D space
- Cons: expensive to construct an accurate classifier in **high-D** space

✓ **Deterministic approach** [4]: integrate the failure region in the variation space

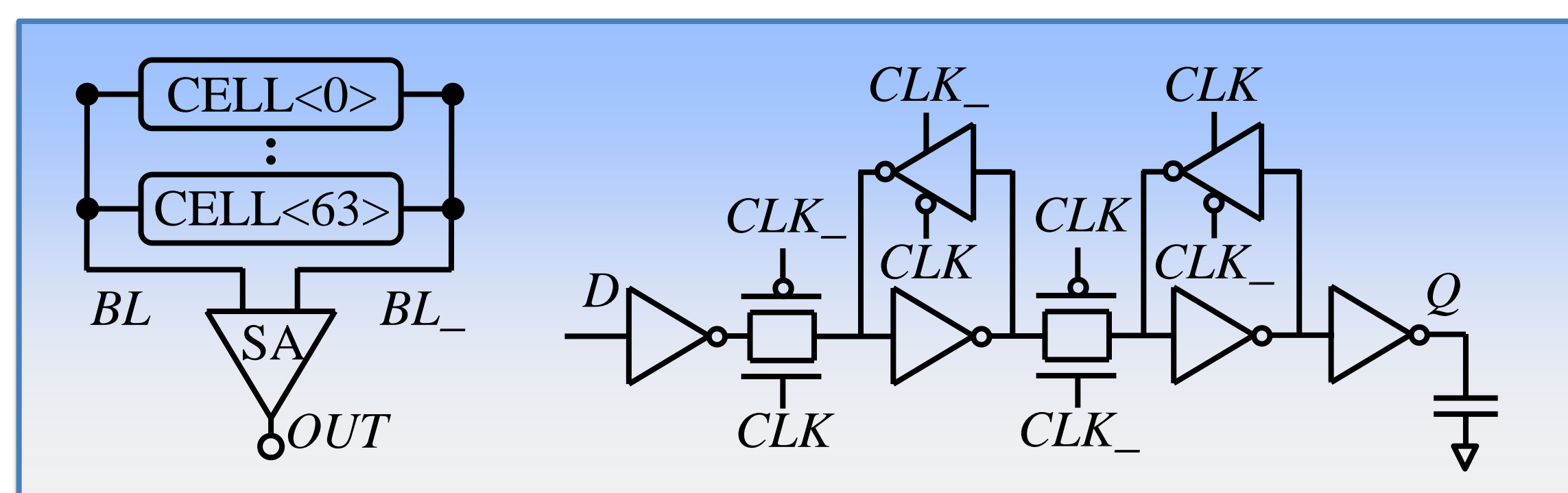
- Pros: efficient in low-D space
- Cons: expensive to accurately describe the failure region in **high-D** space

Challenge: High-Dimensionality

✓ In the past, rare failure event analysis was mainly focused on SRAM bit cell ← **low-D**

✓ Recently, rare failure event analysis in high-D becomes more and more important

1. **Dynamic SRAM bit cell stability related to peripherals:** many transistors from multiple SRAM bit cells and their peripheral circuits must be considered
2. **Rare failure event analysis for non-SRAM circuits:** e.g., DFF



SRAM

DFF

Subset Simulation (SUS): Continuous Performance Metric

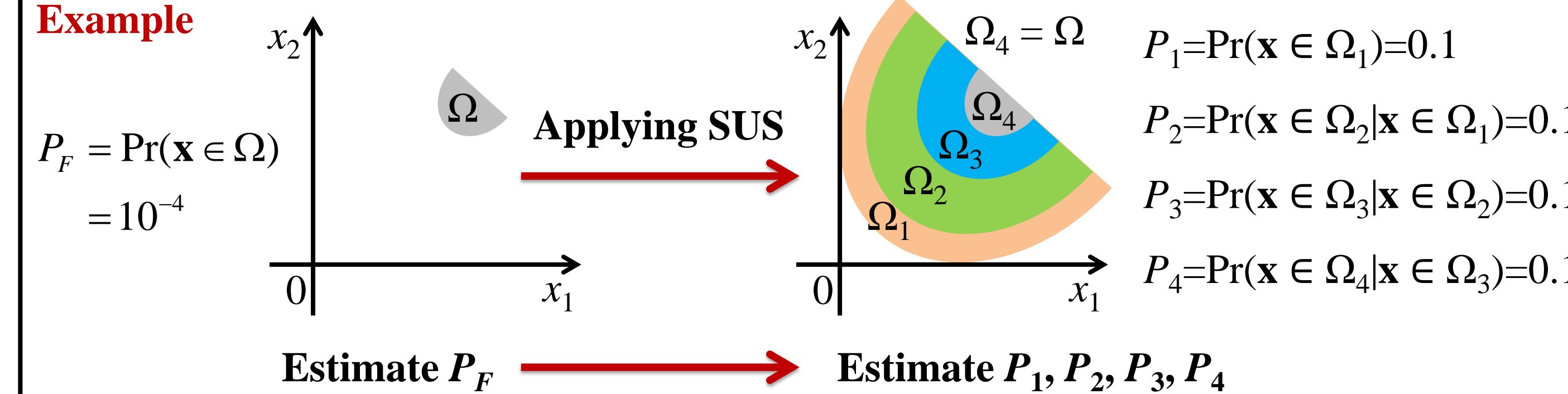
✓ **Idea:** find K subsets $\{\Omega_k; k = 1, 2, \dots, K\}$ in \mathbf{x} -space, and estimate the rare failure rate P_F by the conditional probabilities $\{P_k; k = 1, 2, \dots, K\}$

$$\Omega_1 \supseteq \Omega_2 \supseteq \dots \supseteq \Omega_{K-1} \supseteq \Omega_K = \Omega$$

$$P_F = \Pr(\mathbf{x} \in \Omega) = \Pr(\mathbf{x} \in \Omega_1) \prod_{k=2}^K \Pr(\mathbf{x} \in \Omega_k | \mathbf{x} \in \Omega_{k-1}) = \prod_{k=1}^K P_k$$

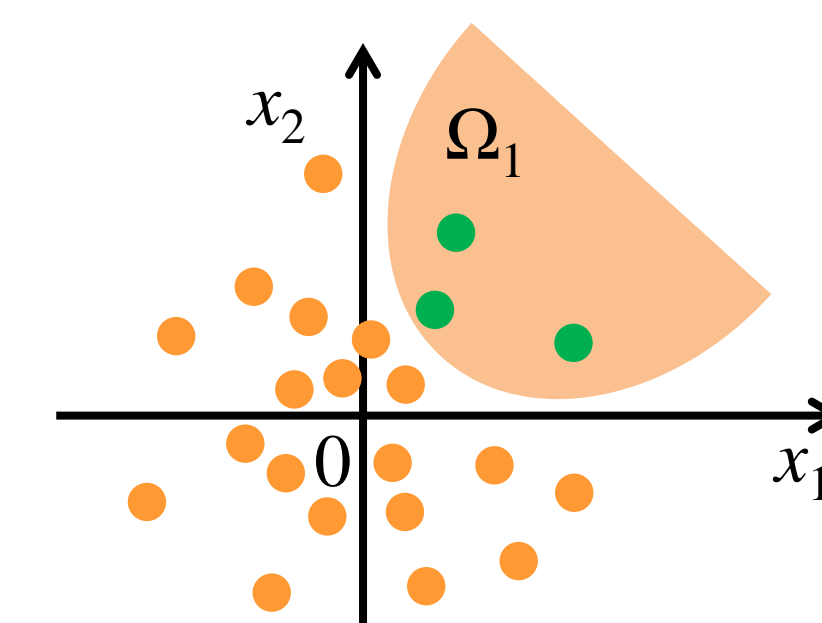
\mathbf{x} : process variation
 Ω : interested failure region
 P_F : interested failure rate

Example



✓ **Question:** how to estimate these conditional probabilities $\{P_k; k = 1, 2, \dots, K\}$?

Phase 1: draw random samples from PDF $f(\mathbf{x})$ and estimate $P_1 = \Pr(\mathbf{x} \in \Omega_1)$

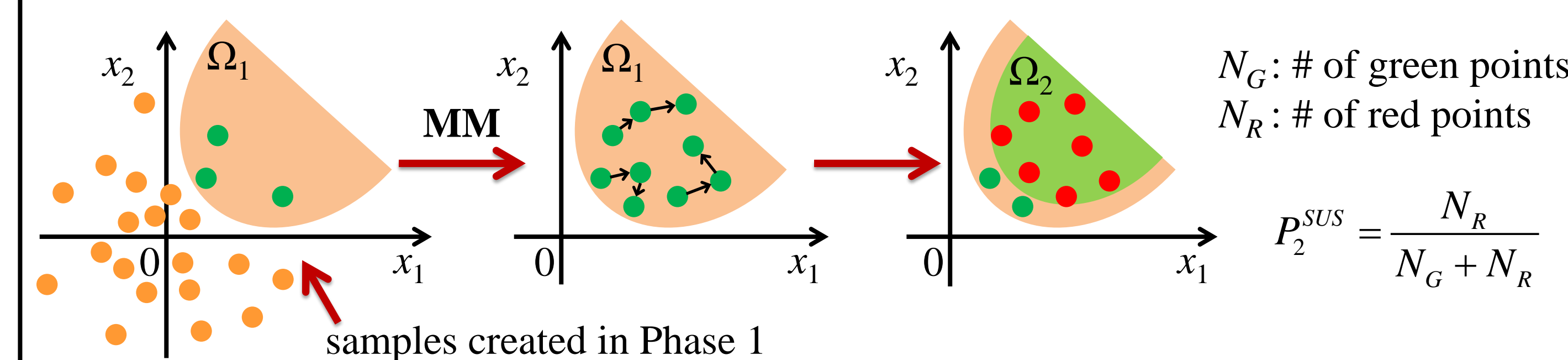
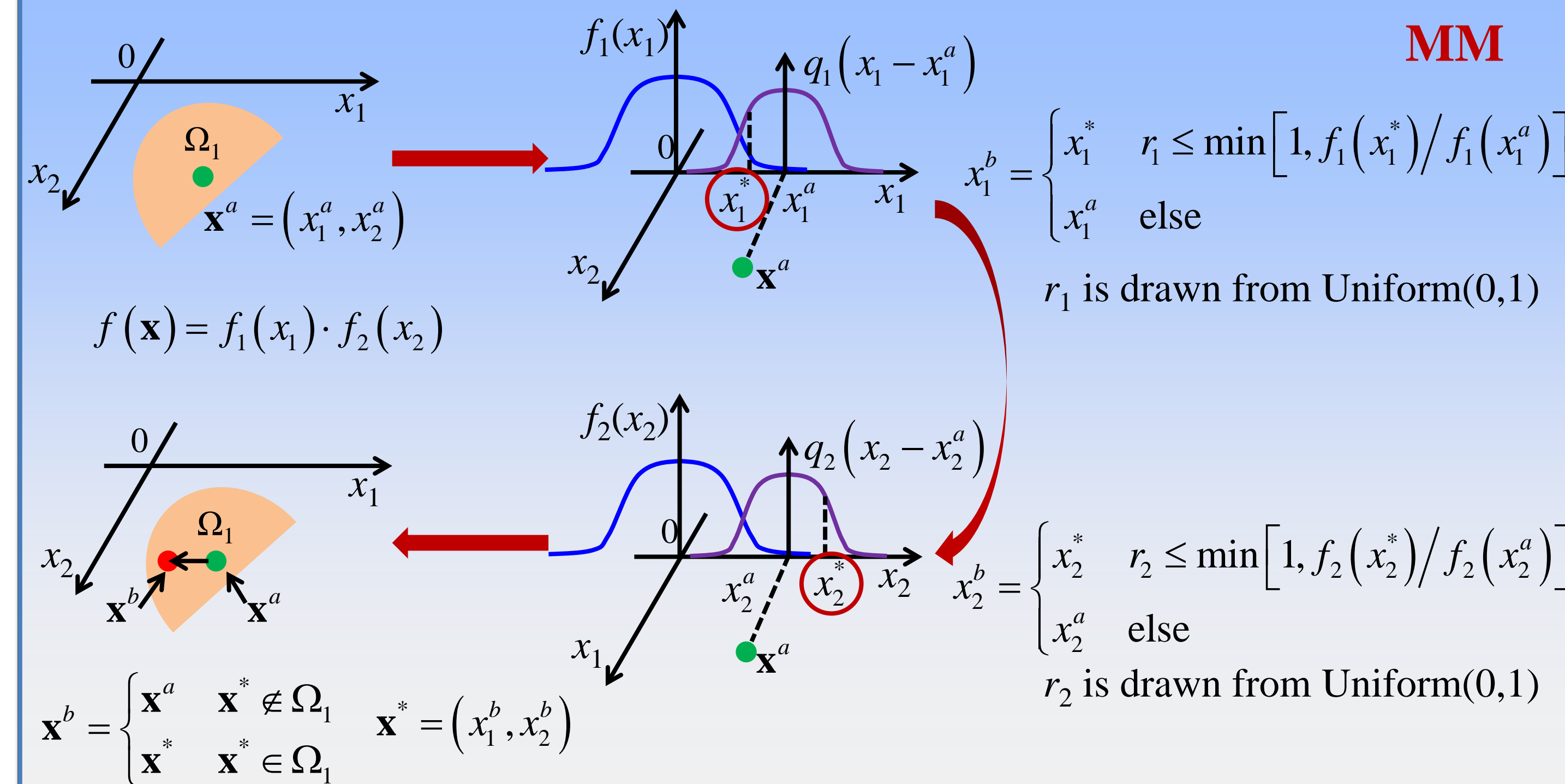


x_1, x_2 are generally modeled as independent Normal random variables

N_Y : # of yellow points N_G : # of green points

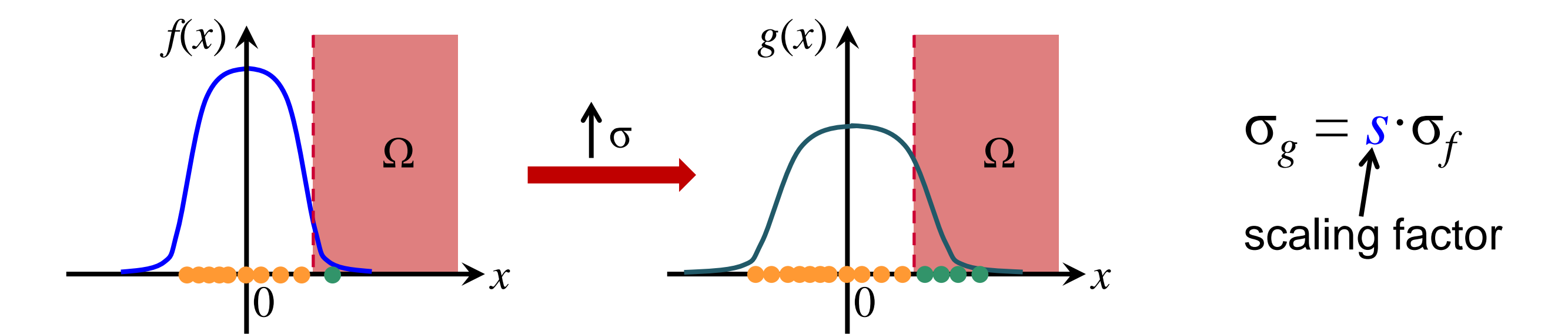
$$P_1^{SUS} = \frac{N_G}{N_G + N_Y}$$

Phase 2: draw random samples from $f(\mathbf{x} | \mathbf{x} \in \Omega_1)$ and estimate $P_2 = \Pr(\mathbf{x} \in \Omega_2 | \mathbf{x} \in \Omega_1)$. $f(\mathbf{x} | \mathbf{x} \in \Omega_1)$ is **unknown** in advance. **Modified Metropolis** (MM) algorithm is applied to generate random samples that follow $f(\mathbf{x} | \mathbf{x} \in \Omega_1)$



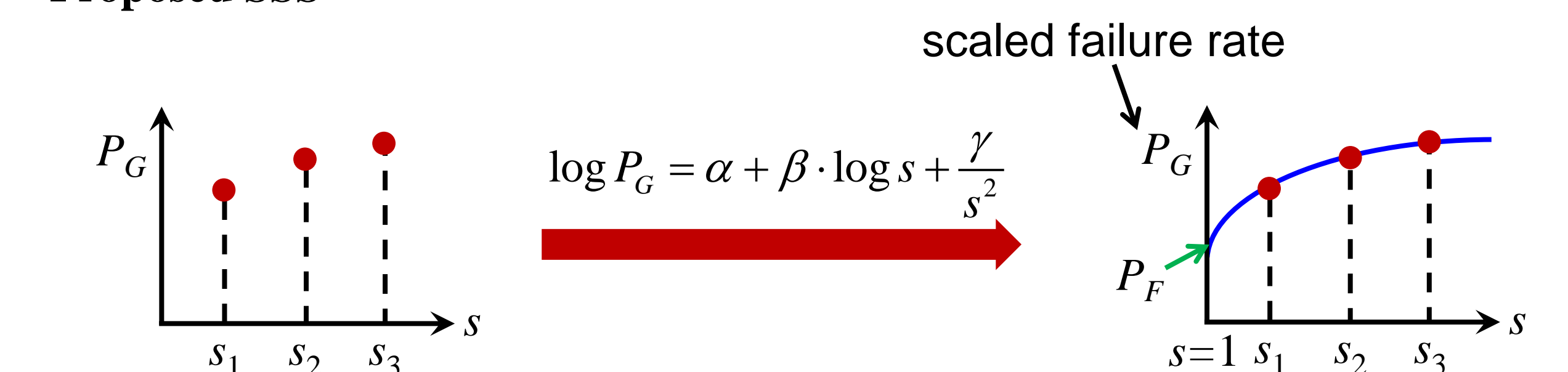
Scaled-Sigma Sampling (SSS): Discrete Performance Metric

✓ **Idea:** it is much easier to estimate P_G than P_F if s is large enough

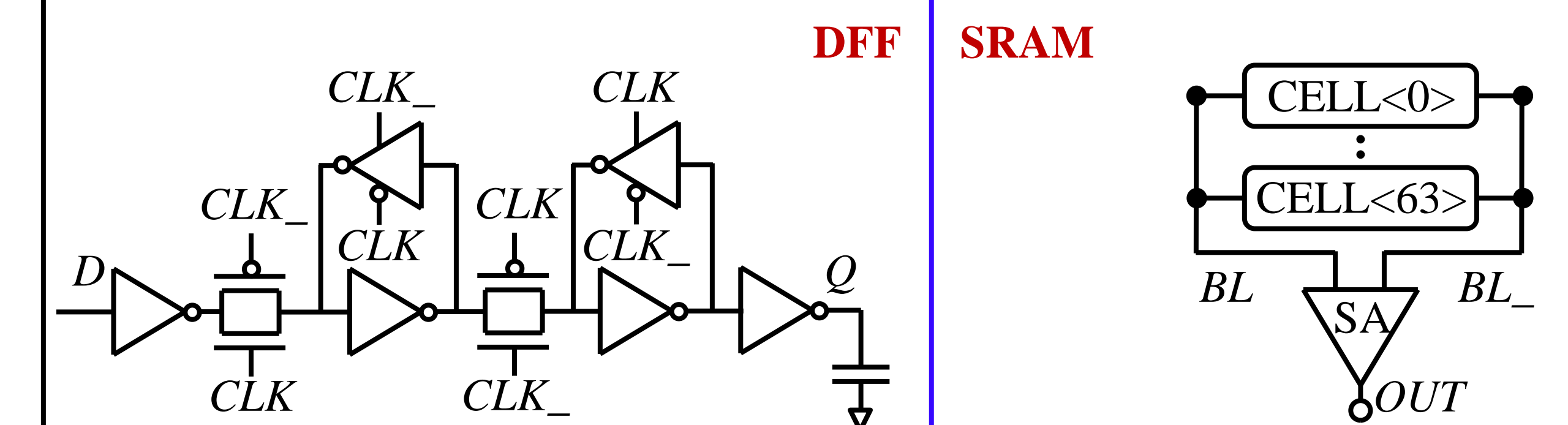


$f(x)$: original probability density function P_F : failure rate by sampling $f(x)$
 $g(x)$: scaled probability density function P_G : failure rate by sampling $g(x)$
 σ_f : σ of $f(x)$ σ_g : σ of $g(x)$

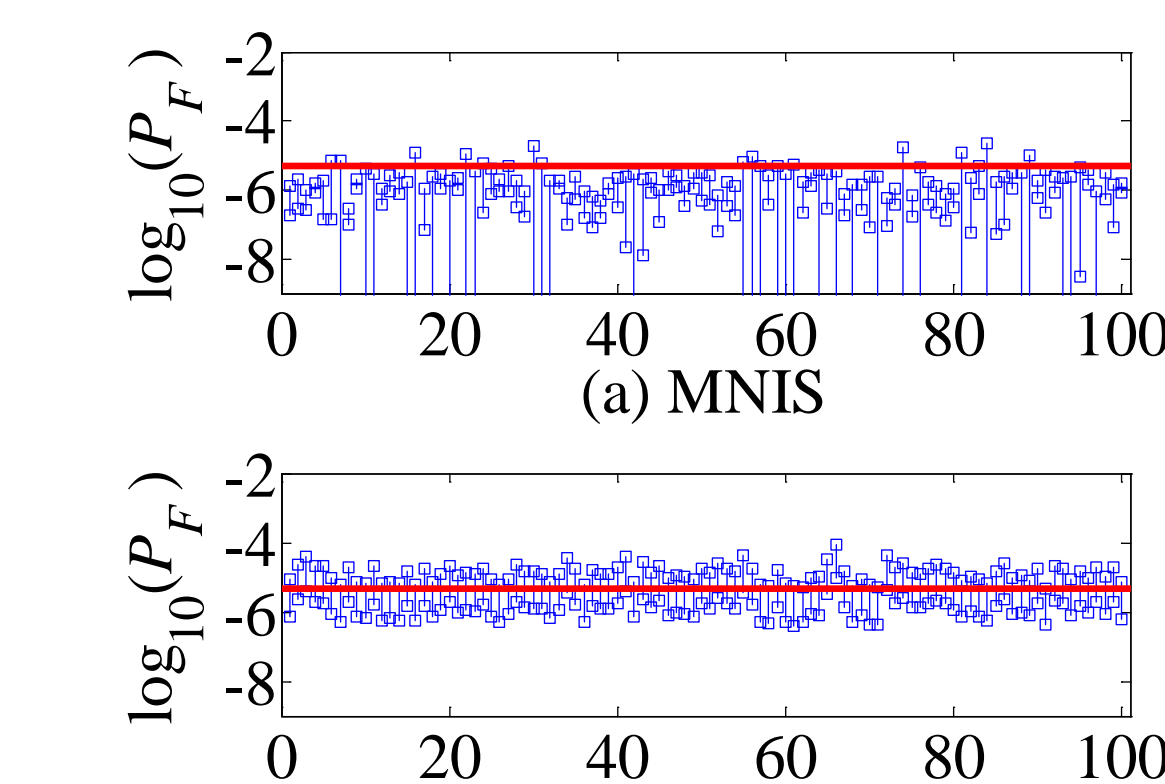
✓ **Proposed SSS**



✓ **Experimental results**

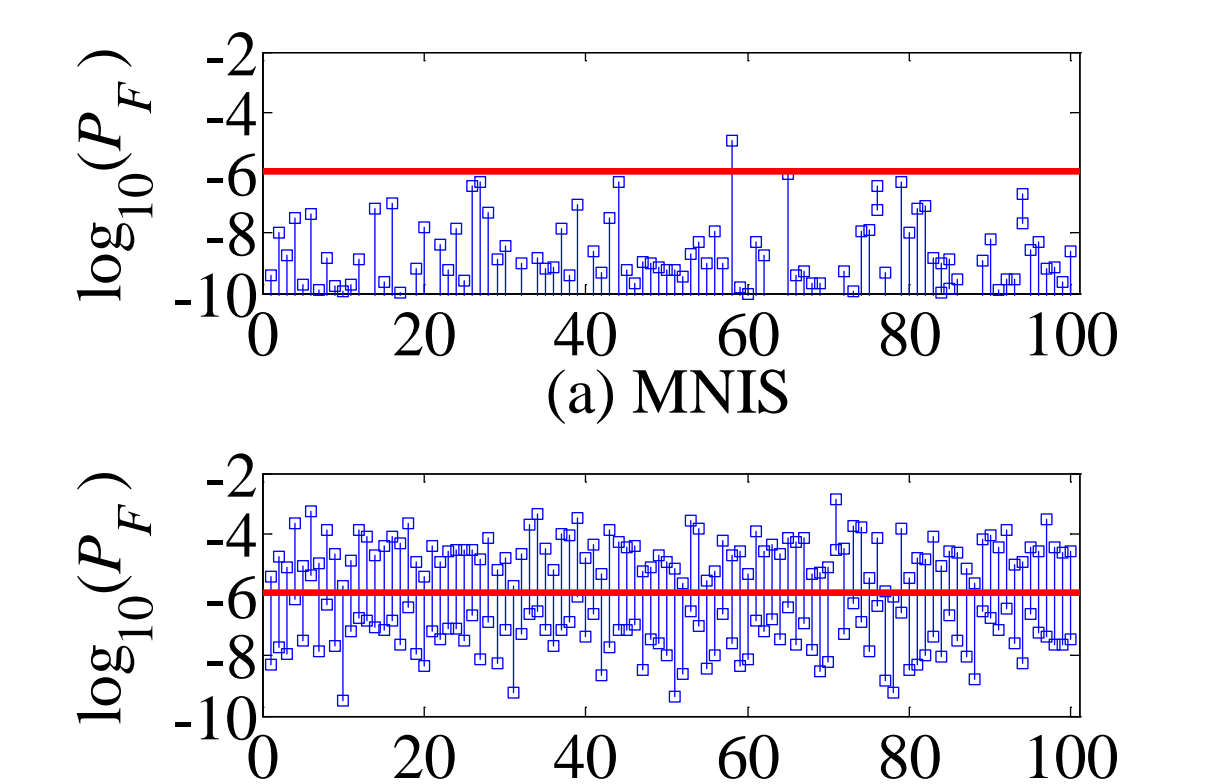


- 45nm CMOS technology
- 200 independent random variables
- The delay from CLK→Q is performance of interest
- 100 95% confidence intervals (CIs) are calculated from 100 runs with 5500 simulations in each run
- The “golden” failure rate is 4.8×10^{-6} that is estimated by MC with 5 million simulations



The 95% CIs (blue bars) of the DFF example for: (a) MNIS [2] and (b) SUS. The red line represents the “golden” failure rate.

- 45nm CMOS technology
- 384 independent random variables
- The output of SA is performance of interest
- 100 95% confidence intervals (CIs) are calculated from 100 runs with 6000 simulations in each run
- The “golden” failure rate is 1.1×10^{-6} that is estimated by MC with 1 billion simulations



The 95% CIs (blue bars) of the SRAM example for: (a) MNIS [2] and (b) SSS. The red line represents the “golden” failure rate.

[1] C. Bishop, *Pattern Recognition and Machine Learning*. Prentice Hall, 2007.
 [2] M. Qazi, et al., “Loop flattening & spherical sampling: highly efficient model reduction techniques for SRAM yield analysis,” *IEEE DATE*, 2008, pp. 801-806.
 [3] A. Singhee and R. Rutenbar, “Statistical blockade: very fast statistical simulation and modeling of rare circuit events, and its application to memory design,” *IEEE TCAD*, vol. 28, no. 8, pp. 1176-1189, Aug. 2009.
 [4] C. Gu and J. Roychowdhury, “An efficient, fully nonlinear, variability aware non-Monte-Carlo yield estimation procedure with applications to SRAM cells and ring oscillators,” *IEEE ASP-DAC*, pp. 754-761, 2008.
 [5] S. Sun, et al., “Fast statistical analysis of rare circuit failure events via scaled-sigma sampling for high-dimensional variation space,” *IEEE ICCAD*, 2013, pp. 478-485.
 [6] S. Sun and X. Li, “Fast statistical analysis of rare circuit failure events via subset simulation in high-dimensional variation space,” *IEEE ICCAD*, 2014, accepted.