# Po-An Tsai

**November 2018**


**CONTACT INFORMATION**

Po-An Tsai
MIT CSAIL, 32 Vassar Street, room 32-G888
Cambridge, MA 02139

+1 (617) 401-5389
poantsai@csail.mit.edu
http://people.csail.mit.edu/poantsai/


**RESEARCH INTERESTS**

Computer system and architecture. Memory hierarchy design. Software/hardware co-optimization. Resource management in multi-core systems. Data center infrastructure efficiency.

**EDUCATION**

**Ph.D. in Computer Science**, June 2015 - June 2019 (expected) *Massachusetts Institute of Technology*
- Advisor: Professor Daniel Sanchez
- Thesis: Redesigning the Memory Hierarchy to Exploit Static and Dynamic Application Information
- Minor: Optimization Methods

**S.M. in Computer Science**, June 2015 *Massachusetts Institute of Technology*
- Advisor: Professor Daniel Sanchez
- Thesis: Reducing Data Movement in Multicore Chips with Computation and Data Co-scheduling
- GPA: 4.92/5.0

**B.S. in Electrical Engineering**, June 2012 *National Taiwan University (NTU), Taiwan*
- GPA: 3.96/4.0

**HONORS AND AWARDS**

Best Paper Nominee, HPCA-21, 2015

Best Poster Award, MIT Industry-Academia Partnership Workshop – MIT, 2014

Jacobs Presidential Fellowship – MIT, 2013

Valedictorian – NTUEE, 2012

Presidential Award – NTU, 2010, 2011, 2012

Second Prize, NTUEE Undergraduate Research Award – NTU, 2012

Star Futures Award, Altera International FPGA Design Contest – China, 2011

**RESEARCH EXPERIENCE**

**Research Assistant**, September 2013–Current *Computation Structure Group, MIT, Cambridge MA*

**Object-based memory hierarchies:**
- Hotpads (**MICRO-51**): designed an object-based memory hierarchy designed from the ground up for modern, memory-safe languages. Hotpads reduces memory hierarchy energy by 2.6×.
- Zippads (**ASPLOS-24**): designed an compressed memory hierarchy for object-based programs. Zippads reduces main memory footprint by 2×, while improving performance by 30%.

**Software-defined memory hierarchies:**
- Jenga (**ISCA-44**): designed a software-defined, heterogeneous memory hierarchy that adapts to the need of applications. Jenga improves full-system EDP by 23% on average and by up to 85%.
- AMS (**MICRO-51**): proposed an analytical model and scheduling algorithms for systems with near-data processing (NDP) capabilities. AMS improves performance by up to 37%.
- Nexus (**PACT-26**): developed an asymptotically better data replication policy for distributed shared caches. Nexus improves performance by 23% on average for replication-sensitive workloads.

**Undergraduate Research Assistant**, March 2012–September 2012
*NTU-IBM Austin Research Lab (ARL) Collaborative Project, NTU PAS Lab, Taiwan*
- Advisor: Shih-Hao Hung
- Worked on a simulation and verification tool for FPGA-accelerated medical image processing.

**Undergraduate Research Assistant**, March 2011–September 2012
*Bio-inspired Network-on-Chip Project, NTU Access Lab, Taiwan*
- Advisor: An-Yeu Wu
- Proposed a path-diversity-aware, adaptive routing algorithm for network-on-chip.

**WORK EXPERIENCE**

**Ph.D. Intern**, Summer 2015 *Distributed Resource Management Team, VMware, Palo Alto CA*
- Manager: Lan Gao Mentor: Rean Griffith and Sahan Gamage
- Developed and prototyped a VM scheduler that performs multi-dimensional resource balancing and traffic engineering which reduces the runtime overhead by 10× while improving utilization by 5%
- The proposed algorithm is implemented in the 2016 release and filed as a US patent (US 15283274).

**WORK EXPERIENCE (continued)**

**Teaching Assistant**, Spring 2015 *Computer System Architecture, MIT, Cambridge MA*

- Lecturer: Professors Daniel Sanchez and Joel Emer
- Designed a new lab assignment on extending Zsim, a pin-based multicore simulator.
- Participated in setting quizzes and provided office hours, tutorials, and recitations.

**Hardware Engineering Intern**, Summer 2011 *Power System Lab, IBM Taiwan, Taiwan*

- Manager: Janice Wang Mentor: Sor Lien and Sertac Cakici
- Participated in PCB design for Power 7 servers, server configuration, and IC vendor collaborations.

**PUBLICATIONS**

**Compress Objects, Not Cache Lines: An Object-Based Compressed Memory Hierarchy**
**Po-An Tsai** and Daniel Sanchez.
The 24th International Conference on Architectural Support for Programming Languages and Operating Systems, (ASPLOS-24), April 2019.

**Rethinking the Memory Hierarchy for Modern Languages**
**Po-An Tsai**, Yee Ling Gan, and Daniel Sanchez.
The 51st International Symposium on Microarchitecture (MICRO-51), October 2018.

**Adaptive Scheduling for Systems with Asymmetric Memory Hierarchies**
**Po-An Tsai**, Changping Chen, and Daniel Sanchez.
The 51st International Symposium on Microarchitecture (MICRO-51), October 2018.

**KPart: A Hybrid Cache Partitioning-Sharing Technique for Commodity Multicores**
Nosayba El-Sayed, Anurag Mukkara, **Po-An Tsai**, Harshad Kasture, Xiaosong Ma, and Daniel Sanchez.
The 24th Intl. Symposium on High Performance Computer Architecture (HPCA-24), February 2018.

**Nexus: A New Approach to Replication in Distributed Shared Caches**
**Po-An Tsai**, Nathan Beckmann, and Daniel Sanchez.
The 26th International Conference on Parallel Architectures and Compilation Techniques (PACT-26), September 2017.

**Jenga: Software-Defined Cache Hierarchies**
**Po-An Tsai**, Nathan Beckmann, and Daniel Sanchez.
The 44th International Symposium on Computer Architecture (ISCA-44), June 2017.

**Scaling Distributed Cache Hierarchies with Computation and Data Co-Scheduling**
Nathan Beckmann, **Po-An Tsai**, and Daniel Sanchez.
The 21st International Symposium on High Performance Computer Architecture (HPCA-21), February 2015. **Nominated for the best paper award**

**Hybrid Path-Diversity-Aware Adaptive Routing with Latency Prediction Model in Network-on-Chip Systems**
**Po-An Tsai**, Yu-Hsin Kuo, En-Jui Chang, and An-Yeu Wu.
International Symposium on VLSI Design, Automation & Test, (VLSI-DAT), March 2013.

**Path-Diversity-Aware Adaptive Routing in Network-on-Chip Systems**
Yu-Hsin Kuo, **Po-An Tsai**, Hao-Ping Ho, En-Jui Chang, Hsien-Kai Hsin, and An-Yeu Wu.
The 6th International Symposium on Embedded Multicore SoCs (MCSoC), September 2012.

**PATENT**

**Resource-Based Virtual Computing Instance Scheduling** US Patent 15283274
**Po-An Tsai**, Sahan Gamage, and Rean Griffith.

**SKILLS AND TOOLS**

Programming languages and projects:

- **C, C++:** Event-driven multicore-processor simulator, Linux kernel extension
- **Verilog**: FPGA-accelerated augmented-reality system, FPGA-accelerated medical image processing
- **CUDA, OpenCL**: GPGPU-assisted ultra-sonic array imaging system
- **Java**: Extending Maxine VM, a meta-circular JVM implementation for research
- Others: Python, Matlab, Shell script, SQL

**Libraries:** CUDA, OpenCL, matplotlib

**Tools:** Git, Intel Pin, Zsim, ModelSim, Altera Quantus II, IC Encounter

**SERVICE**

- Submissions Co-Chair, MICRO-50, 2017
- President, 2014-2015, Taiwanese student association at MIT.