Po-An Tsai

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CONTACT INFORMATION

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RESEARCH INTERESTS

Computer system and architecture. Domain-specific (ML/DL) architecture. Accelerator modeling and prototyping. Memory hierarchy design. SW/HW co-optimization.

EDUCATION

Ph.D. in Computer Science, June 2015 - June 2019 *Massachusetts Institute of Technology*

- Advisor: Professor Daniel Sanchez
- Thesis: Redesigning the Memory Hierarchy to Exploit Static and Dynamic Application Information
- Minor: Optimization Methods

S.M. in Computer Science, June 2015 *Massachusetts Institute of Technology*

- Advisor: Professor Daniel Sanchez
- Thesis: Reducing Data Movement in Multicore Chips with Computation and Data Co-scheduling
- GPA: 4.92/5.0

B.S. in Electrical Engineering, June 2012 *National Taiwan University (NTU), Taiwan*

- GPA: 3.96/4.0

HONORS AND AWARDS

IEEE Micro Top Picks Award, 2021

Best Paper Nominee, HPCA-21, 2015

Best Poster Award, MIT Industry-Academia Partnership Workshop – MIT, 2014

Jacobs Presidential Fellowship – MIT, 2013

Valedictorian – NTUEE, 2012

Presidential Award – NTU, 2010, 2011, 2012

Second Prize, NTUEE Undergraduate Research Award – NTU, 2012

Star Futures Award, Altera International FPGA Design Contest – China, 2011

WORK EXPERIENCE

Research Scientist, July 2019 – Current *Architecture Research Group (ARG), NVIDIA, Westford MA*

- Manager: Steve Keckler
- Work on a novel architecture with runtime reconfigurable HW/SW that enables near ASIC performance (within 10x) but with high programmability for data-intensive algorithms.
- Work on a flexible tensor accelerator that leverages a hierarchical and configurable data delivery network to adapt to a variety of GEMM and CNN workloads.
- Contribute to an open-sourced tool (Timeloop+Accelergy) for rapid evaluation of DNN accelerators.
- Work on analytical modeling methodology for sparse tensor accelerators.
- Work on defining programming model and abstraction for domain-specific architectures.

Research Assistant, September 2013 – May 2019 *Computation Structure Group, MIT, Cambridge MA*

Object-based memory hierarchies:

- Hotpads (**MICRO-51**): designed an object-based memory hierarchy designed from the ground up for modern, memory-safe languages. Hotpads reduces memory hierarchy energy by 2.6×.
- Zippads (**ASPLOS-24**): designed a compressed memory hierarchy for object-based programs. Zippads reduces main memory footprint by 2× while improving performance by 30%.

Software-defined memory hierarchies:

- Jenga (**ISCA-44**): designed a software-defined, heterogeneous memory hierarchy that adapts to the need of applications. Jenga improves full-system EDP by 23% on average and by up to 85%.
- AMS (**MICRO-51**): proposed an analytical model and scheduling algorithms for systems with near-data processing (NDP) capabilities. AMS improves performance by up to 37%.
- Nexus (**PACT-26**): developed an asymptotically better data replication policy for distributed shared caches. Nexus improves performance by 23% on average for replication-sensitive workloads.

Ph.D. Intern, Summer 2015 *Distributed Resource Management Team, VMware, Palo Alto CA*

- Manager: Lan Gao Mentor: Rean Griffith and Sahan Gamage
- Developed and prototyped a VM scheduler that performs multi-dimensional resource balancing and traffic engineering which reduces the runtime overhead by 10× while improving utilization by 5%.
- The proposed algorithm is implemented in the 2016 release and filed as a US patent (US 15283274).

Undergraduate Research Assistant, March 2012–September 2012
NTU-IBM Austin Research Lab (ARL) Collaborative Project, NTU PAS Lab, Taiwan
- Advisor: Shih-Hao Hung
- Worked on a simulation and verification tool for FPGA-accelerated medical image processing.

Hardware Engineering Intern, Summer 2011 *Power System Lab, IBM Taiwan, Taiwan*
- Manager: Janice Wang Mentor: Sor Lien and Sertac Cakici
- Participated in PCB design for Power 7 servers, server configuration, and IC vendor collaborations.

Undergraduate Research Assistant, March 2011–September 2012
Bio-inspired Network-on-Chip Project, NTU Access Lab, Taiwan
- Advisor: An-Yeu Wu
- Proposed a path-diversity-aware, adaptive routing algorithm for network-on-chip.

PUBLICATIONS

Leaking Secrets through Compressed Caches
Po-An Tsai, Andres Sanchez, Christopher W. Fletcher, and Daniel Sanchez.
IEEE Micro's Top Picks from the Computer Architecture Conferences, May/June 2021.

Mind Mappings: Enabling Efficient Algorithm-Accelerator Mapping Space Search
Kartik Hegde, **Po-An Tsai**, Sitao Huang, Vikas Chandram, Angshuman Parashar, and Christopher W. Fletcher.
The 25th International Conference on Architectural Support for Programming Languages and Operating Systems, (ASPLOS-26), April 2021.

Sparseloop: An Analytical, Energy-Focused Design Space Exploration Methodology for Sparse Tensor Accelerators
Yannan Nellie Wu, **Po-An Tsai**, Angshuman Parashar, Vivienne Sze, Joel S. Emer
IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS) March, 2021

Hardware Abstractions for Targeting EDDO Architectures with the Polyhedral Model
Angshuman Parashar, Prasanth Chatarasi, and **Po-An Tsai**.
International Workshop on Polyhedral Compilation Techniques (IMPACT), January 2021.

Safecracker: Leaking Secrets through Compressed Caches
Po-An Tsai, Andres Sanchez, Christopher W. Fletcher, and Daniel Sanchez.
The 25th International Conference on Architectural Support for Programming Languages and Operating Systems, (ASPLOS-25), March 2020.

Compress Objects, Not Cache Lines: An Object-Based Compressed Memory Hierarchy
Po-An Tsai and Daniel Sanchez.
The 24th International Conference on Architectural Support for Programming Languages and Operating Systems, (ASPLOS-24), April 2019.

Rethinking the Memory Hierarchy for Modern Languages
Po-An Tsai, Yee Ling Gan, and Daniel Sanchez.
The 51st International Symposium on Microarchitecture (MICRO-51), October 2018.

Adaptive Scheduling for Systems with Asymmetric Memory Hierarchies
Po-An Tsai, Changping Chen, and Daniel Sanchez.
The 51st International Symposium on Microarchitecture (MICRO-51), October 2018.

KPart: A Hybrid Cache Partitioning-Sharing Technique for Commodity Multicores
Nosayba El-Sayed, Anurag Mukkara, **Po-An Tsai**, Harshad Kasture, Xiaosong Ma, and Daniel Sanchez.
The 24th Intl. Symposium on High Performance Computer Architecture (HPCA-24), February 2018.

Nexus: A New Approach to Replication in Distributed Shared Caches
Po-An Tsai, Nathan Beckmann, and Daniel Sanchez.
The 26th International Conference on Parallel Architectures and Compilation Techniques (PACT-26), September 2017.

Jenga: Software-Defined Cache Hierarchies
Po-An Tsai, Nathan Beckmann, and Daniel Sanchez.
The 44th International Symposium on Computer Architecture (ISCA-44), June 2017.

Scaling Distributed Cache Hierarchies with Computation and Data Co-Scheduling
Nathan Beckmann, **Po-An Tsai**, and Daniel Sanchez.
The 21st International Symposium on High Performance Computer Architecture (HPCA-21), February 2015. **Nominated for the best paper award**

Hybrid Path-Diversity-Aware Adaptive Routing with Latency Prediction Model in Network-on-Chip Systems
Po-An Tsai, Yu-Hsin Kuo, En-Jui Chang, and An-Yeu Wu.
International Symposium on VLSI Design, Automation & Test, (VLSI-DAT), March 2013.

Path-Diversity-Aware Adaptive Routing in Network-on-Chip Systems
Yu-Hsin Kuo, **Po-An Tsai**, Hao-Ping Ho, En-Jui Chang, Hsien-Kai Hsin, and An-Yeu Wu.
The 6th International Symposium on Embedded Multicore SoCs (MCSoC), September 2012.

PATENT

Resource-Based Virtual Computing Instance Scheduling US Patent 15283274
Po-An Tsai, Sahan Gamage, and Rean Griffith.

SKILLS AND TOOLS

Programming languages and projects:

- **C, C++:** Analytical modeling tool for DNN accelerators (Timeloop), Event-driven multicore-processor simulator (Zsim), Linux kernel extension
- **Verilog**: FPGA-accelerated augmented-reality system, FPGA-accelerated medical image processing
- **CUDA, OpenCL**: GPGPU-assisted ultra-sonic array imaging system
- **Java**: Extending Maxine VM, a meta-circular JVM implementation for research
- Others: Python, Matlab, Shell script, SQL

Libraries: CUDA, OpenCL, matplotlib

Tools: Git, Intel Pin, Timeloop, Zsim, ModelSim, Altera Quantus II, IC Encounter

SERVICE

- Program Committee Member, ISMM'20, HPCA'21.
- External Review Committee Member, PACT'20, MICRO'20, ASPLOS'21, MICRO'21.
- Workshop/Tutorial Co-Chair, HPCA'21.
- Tutorial Organizer for Timeloop/Accelergy Tutorial: Tools for Evaluating Deep Neural Network Accelerator Designs, MICRO'19, ISCA'20, ISPASS'20.
- Submissions Co-Chair, MICRO-50, 2017
- President, 2014-2015, Taiwanese student association at MIT.