Parallelizing Time With Polynomial Circuits

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RED GREEN BLUE ORANGE

Parallelism and Serialism: Some Questions

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  – *Note could always have an exponential sized circuit of $O(1)$ depth and unbounded fan-in*
- What is the smallest f such that a serial time t algorithm can be represented by a $t(n)^{O(1)}$*-size circuit of depth at most* $f(t(n))$?

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Short Answer:

YES,

... but some gates in the circuits have unbounded fan-in

Prior Work, in brief

Relatively old area

- All prior work for general computational models focused on extending Hopcroft-Paul-Valiant's seminal and deep result:

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Main Idea of $\mathsf{TIME}[t(n)] \subseteq \mathsf{SPACE}[t(n)/\log t(n)]$**:**

Divide-and-conquer on Computation Graph:

DAG with a node for each timestep (or block of timesteps)

– *Value* of node i is state and symbols read/written in step(s) corresponding to i

Arcs: represent read/write/state dependencies

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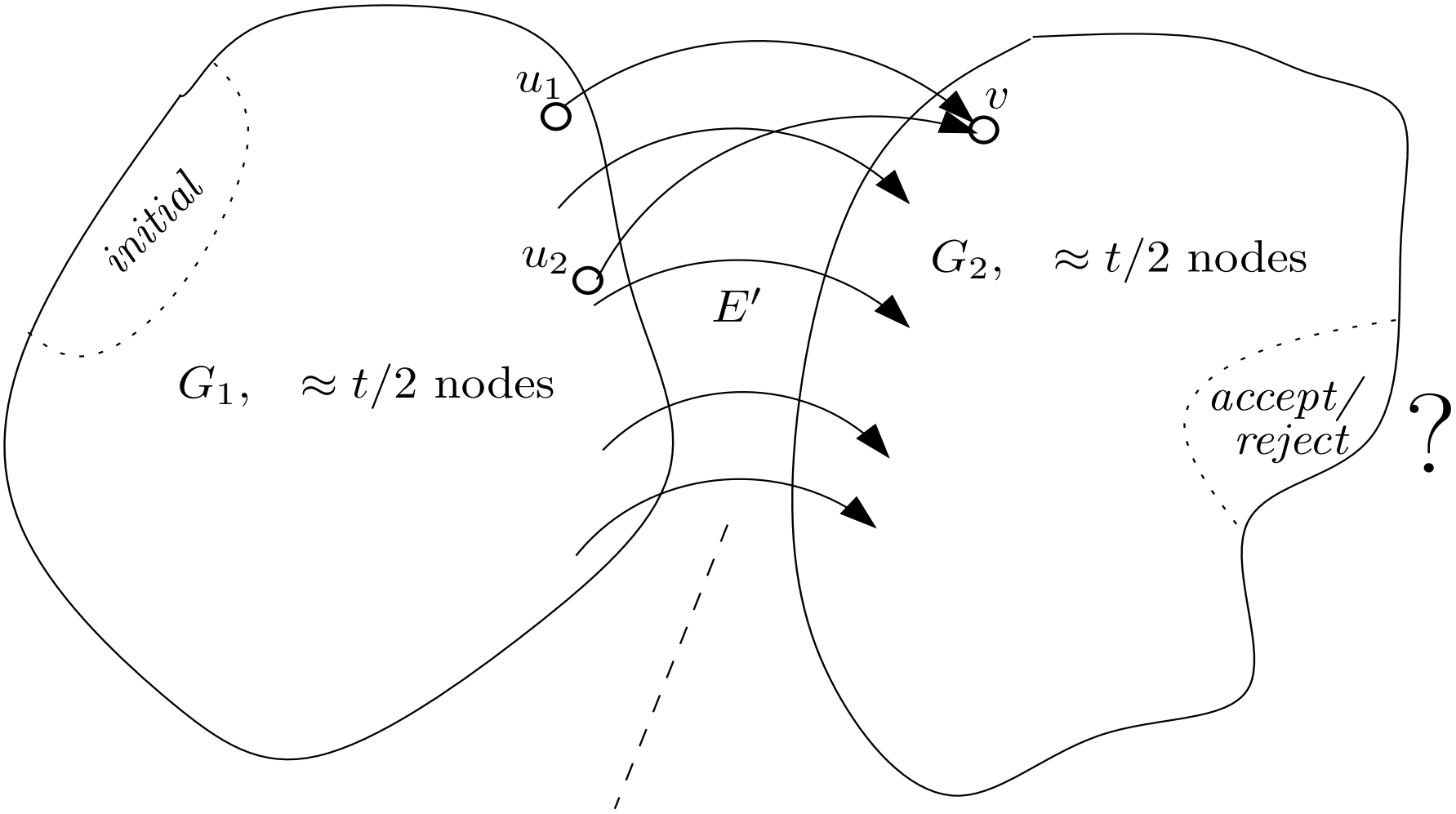

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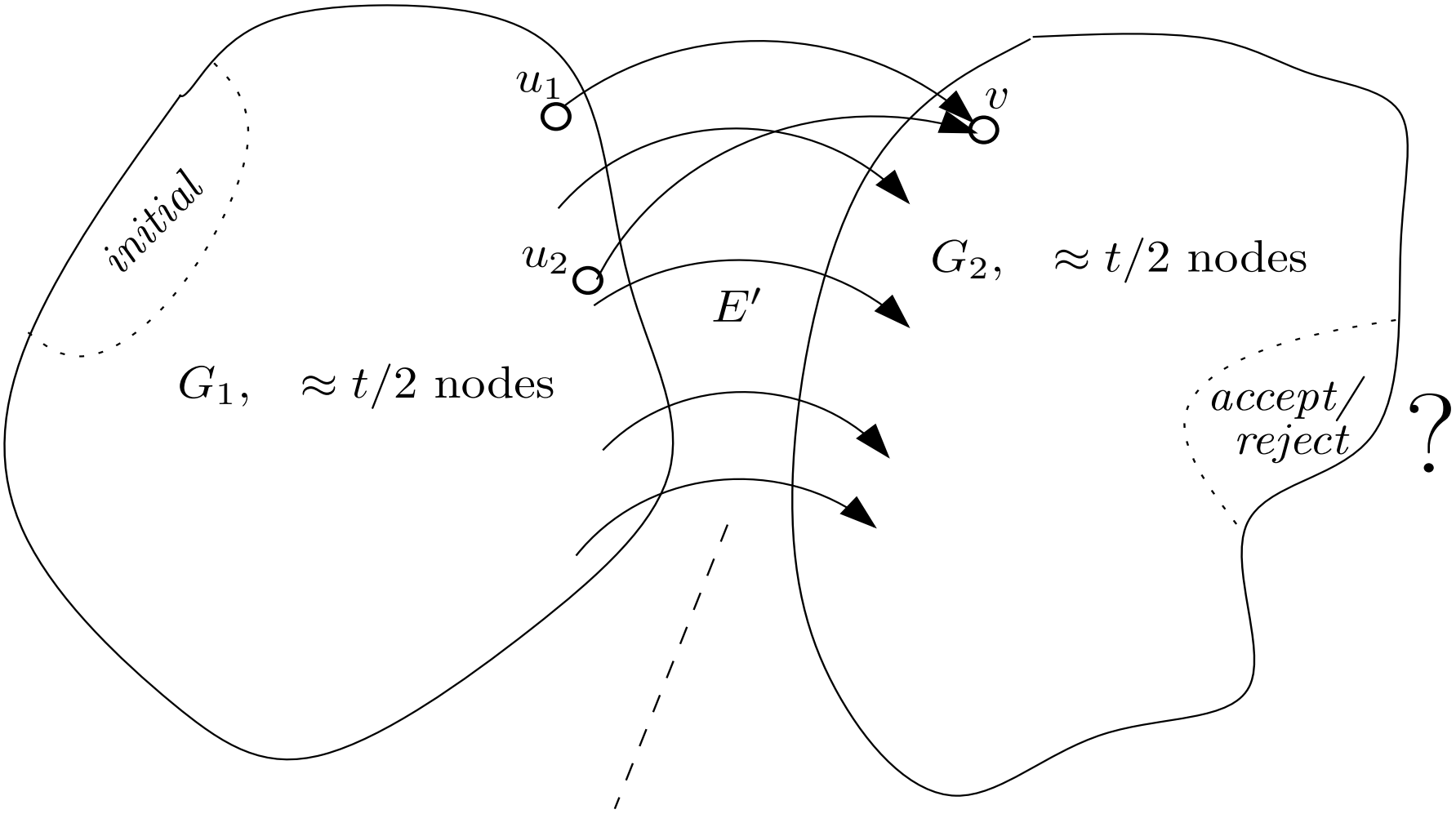

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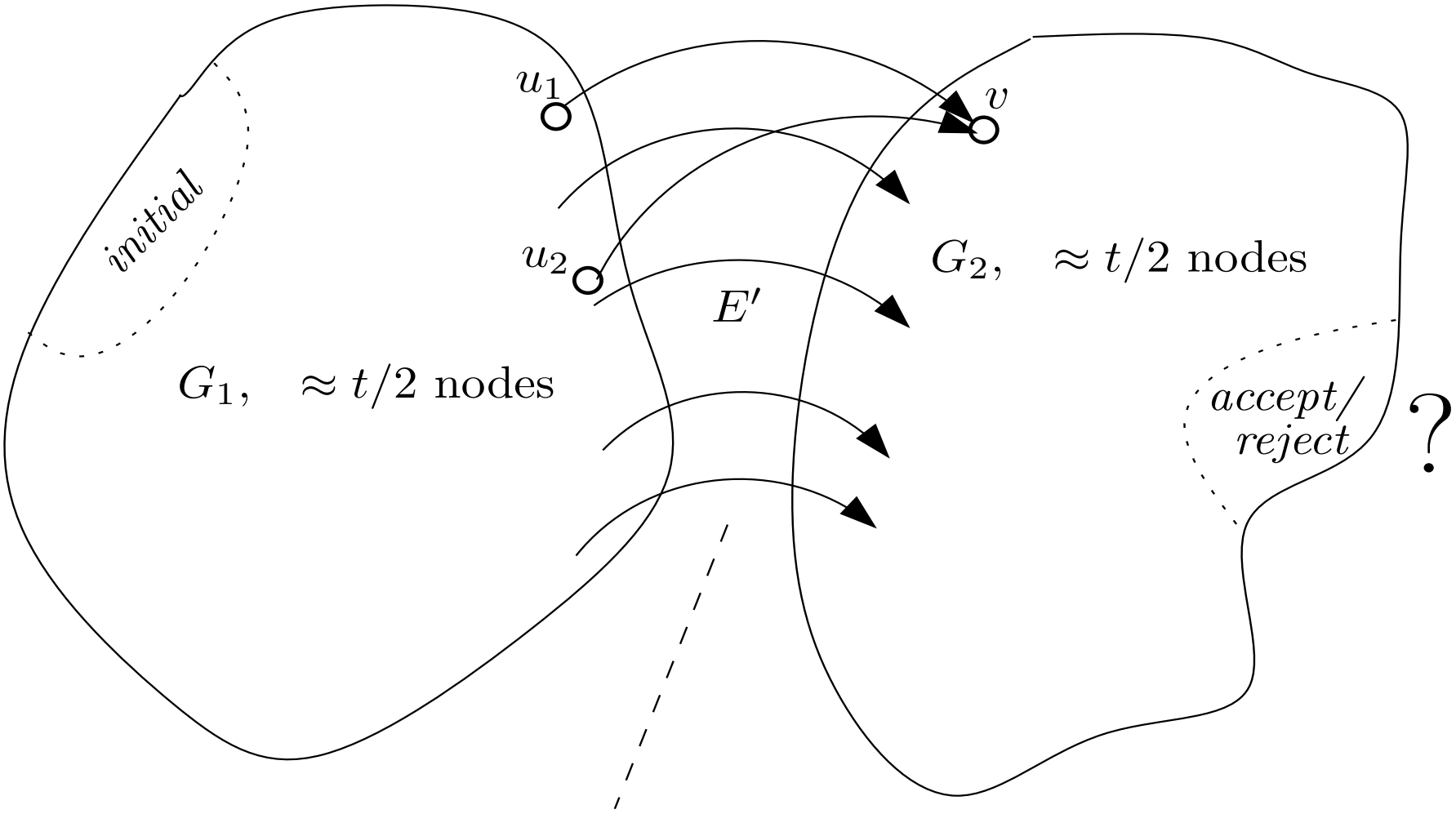

$|E'| \leq t/\log t \Longrightarrow$ "Guess" values at endpoints of E', recurse on G_1 and G_2 separately

$|E'| > t/\log t \Longrightarrow$ To get value of v in G_2, recurse on G_1 for value of u_1 and u_2

Known: Big barriers to this approach

Lower bounds on how well divide-and-conquer can do

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Intuition:

Too much information to be stored when one tries to guess all possible E' in parallel!

Random Access TM Model

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Have:

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In a single step, can:

1. Modify a bit of I
2. Read corresponding register
3. Write to corresponding register
4. Change state

Robust model – can simulate log-cost RAMs (unbounded registers) with constant factor overhead

Main Result

Time $t(n)$ random access TMs can be simulated by a

$t^{O(1)}$-size circuit family of depth $O(t/\log t)$.

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Good news: Construction is *uniform* –

Gives explicit, efficiently constructed circuits.

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1. Partition computation into $O(t/\log t)$ blocks
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1. Partition computation into $O(t/\log t)$ blocks
2. Each block represents $O(\log t)$ consecutive steps

   Blocks are succinctly representable: $O(\log t)$ bits
3. Processing of single block is possible in $O(1)$ depth and $poly(t)$ size:
   - "String" these together

     $\Longrightarrow O(t/\log t)$ depth over all blocks

Local Actions and Blocks

Define **local action** of $A(x)$ at step i to be $\ell = (i, r, I)$, where

r is transition, I is description of index tape at step i

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Define $S_{A(x)}$ to be the (unique) string of the form

$$\ell_0 \, \vec{r}_0 \, \ell_1 \, \vec{r}_1 \, \cdots \, \ell_{(t/\log t)-1} \, \vec{r}_{(t/\log t)-1},$$

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Define a *block* to be an $\ell_i \, \vec{r}_i$ substring of $S_{A(x)}$.

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$\Longrightarrow$ Checks don't contribute to overall depth by more than a constant

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(Top-down description, starting from *output* gate)

Use an AND to simultaneously pick a transition in $\vec{r}$, AND pick ℓ

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If ℓ is picked:

- Use OR to guess the $(i-1)$th block $\ell'\vec{r'}$,
- Call VERIFY$(\ell'\vec{r'}, i-1)$ to **check** state and index tape of ℓ.

  Call LAST-WRITE to **check** that the symbol read in ℓ is correct.

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If the jth component r_j of $\vec{r}$ is picked:

- Use OR to guess I, index tape for the step
- Use ℓ and $\vec{r}$ to **check** that the state of r_j, I are correct
- Call LAST-WRITE on I to **check** that symbol claimed to be read in r_j is correct

Sketch of LAST-WRITE(I, i, σ)**:**

- Use OR to guess ith block: $\ell_i \vec{r_i}$.
- Use AND to simultaneously:
  1. Call VERIFY$(\ell_i \vec{r_i}, i)$ (ensure block is correct), and
  2. **Check** if index tape is ever I in the block;

     if so, then verify σ is written,

     if not, then call LAST-WRITE$(I, i-1, \sigma)$.

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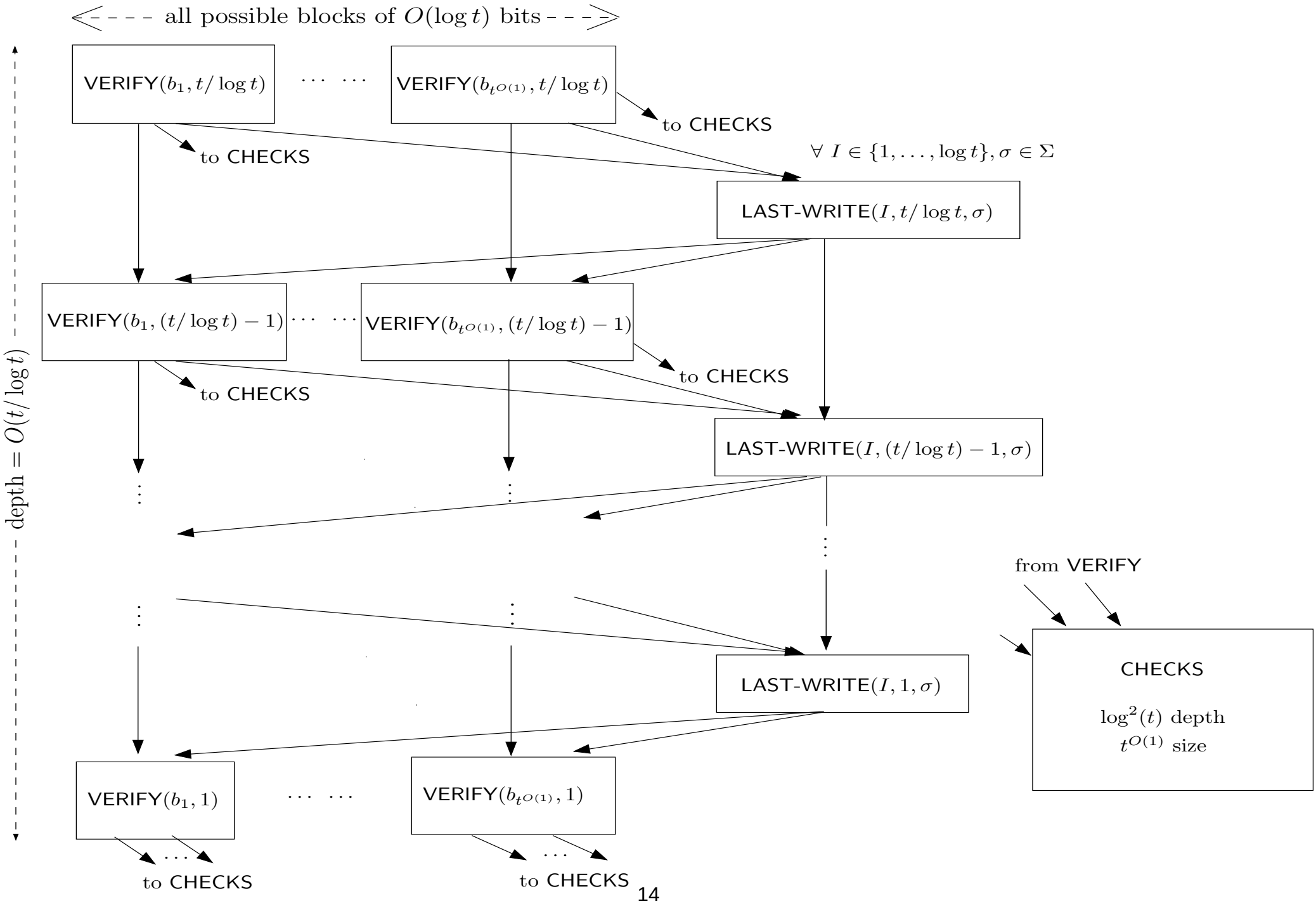
Observations:

- Constant number of OR/AND switches between two recursive calls.
- Depth of recursion = $O(t/\log t)$


all possible blocks of $O(\log t)$ bits
depth $= O(t/\log t)$
VERIFY$(b_1, t/\log t)$
VERIFY$(b_{t^{O(1)}}, t/\log t)$
to CHECKS
$\forall\ I \in \{1, \ldots, \log t\}, \sigma \in \Sigma$
LAST-WRITE$(I, t/\log t, \sigma)$
VERIFY$(b_1, (t/\log t) - 1)$
VERIFY$(b_{t^{O(1)}}, (t/\log t) - 1)$
LAST-WRITE$(I, (t/\log t) - 1, \sigma)$
LAST-WRITE$(I, 1, \sigma)$
VERIFY$(b_1, 1)$
VERIFY$(b_{t^{O(1)}}, 1)$
from VERIFY
CHECKS
$\log^2(t)$ depth
$t^{O(1)}$ size

Implications for Parallel Simulations

Corollary. Every log-cost time t RAM can be simulated by a log-cost CRCW PRAM in $O(t/\log t)$ time with $t^{O(1)}$ processors.

Previous parallel simulations required $2^{\Omega(t/\log t)}$ processors

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Perhaps possible –

combine our ideas with Hopcroft-Paul-Valiant divide-and-conquer(?)