



Special Systems Features Bulletin

IBM 7090-7094 Multiprogramming Package RPQ E07291 (7090) or RPQ 880287 (7094)

TWO FUNCTIONS necessary for efficient multiprogramming or time-sharing of the computer system are automatic relocation of instructions and variable bounds storage protection. The multiprogramming package provides both functions without extending execution time of any computer instruction.

RELOCATION MODE

A seven-bit relocation register is used. During operation in the relocation mode, the contents of this register are added to the high-order seven bits of all storage addresses generated by the central processing unit. This relocated address is then sent to storage. Therefore, a program written to execute in a particular block of storage locations can be moved, with its data, to any other block of locations (the increment being a multiple of 4008) and can be executed there. The contents of the instruction counter are relocated but are always unaltered.

LRI--Load Relocation Indicators



Description: Execution of this instruction places bits 21-27 of location Y into the relocation register. In addition, the CPU is placed in the relocation mode if no bit is present in the S position of location Y. If a 1 bit is present in the S position, the CPU is not placed in the relocation mode.

Relocation and channel traps (including direct data) cannot occur until the instruction following the LRI has been executed. If either an XEC or LPI (or an SEA or SEB used with the Additional Core Storage Feature, 7090 RPQ E02120 or 7094 RPQ 880290) is given immediately following the LRI, an additional instruction delay is effective. If the CPU is in relocation mode, execution of any trap or the STR instruction takes the CPU out of the relocation mode and inhibits channel traps (including direct data) until restored or enabled. In the case of an interval timer trap (7090 RPQ F89349 or 7094 RPQ 880295), a 1 bit is stored in position 17 of location 00006 to designate that the CPU was in relocation mode.

Indicators: Relocate Mode.

Timing: 2 cycles (no overlap with the 7094).

This edition, Form L22-6641-3, obsoletes Form L22-6641-2 and all earlier editions.

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SRI--Store Relocation Indicators



Description: Execution of this instruction stores the relocation register contents in positions 21-27 of location Y. If in relocation mode, a 1 bit is stored in position 1 of location Y. Positions S, 2-20, and 28-35 of location Y are cleared to zeros.

Indicators: None.

Timing: 2 cycles (overlap with even and odd addresses on the 7094).

PROTECTION MODE

Two registers, lower and upper, are used. When operating in the protection mode, any CPU generated storage address is compared against these two registers. Comparison is made after relocation (if any). If the higher order seven-bits of the relocated address is less than the contents of the lower register or greater than the contents of the upper register, execution of the instruction is blocked (except for CAQ, CRQ, and CVR) and a protect trap occurs. The CPU leaves the relocation mode and the protection mode. The protect trap stores the contents of the instruction counter (the location of the instruction causing the trap, plus one) in location 00032₈ and transfers control to location 00033₈.

LPI--Load Protect Indicators



Description: When this instruction is used, it must immediately follow the LRI instruction. Execution of the instruction places the contents of positions 3-9 and 21-27 of location Y into the upper and lower registers, respectively. In addition, the CPU is placed in the protection mode if no bit is present in the S position of location Y. If a 1 bit is present in the S position of location Y, the CPU is not placed in the protection mode. The larger magnitude number must be placed in the upper register.

Protection mode does not become effective and channel traps (including direct data) cannot occur until the instruction following the LPI has been executed. If an XEC (or an SEA or SEB used with the Additional Storage Feature) is given immediately following the LPI, an additional instruction delay is effective. Execution of any trap or the STR instruction takes the CPU out of the protection mode.

Indicators: Protect mode.

Timing: 2 cycles (no overlap with the 7094).

SPI--Store Protect Indicators



Description: Execution of this instruction places the contents of the upper and lower bound registers in positions 3-9 and 21-27 of location Y, respectively. If operating in the protection mode, a 1 bit is stored in position 2 of location Y. Positions S, 1, 10-20 and 28-35 of location Y are cleared to zeros.

Indicators: None.

Timing: 2 cycles (overlap with even and odd addresses with the 7094).

Trapping

If the CPU is operating in the protection mode, execution of any of the following instructions is blocked and a protect trap occurs: BSF, BSR, BTT, ECTM, EFTM, ENB, ESNT, ESTM, ETM, ETT, IOT, LCH, LFTM, LPI, LRI, LSNM, LTM, RCH, RCT, RDC, RDS, REW, RUN, SDN, TCN, TCO, TEF, TRC, WEF, WRS, and I/O Sense. Also: EFT, IFT, SEA, SEB, TIA, and TIB with the Additional Core Storage feature; SWTF and SWTT with the tape switching Feature; and PSL or SSL when the Direct Data Connection Feature (7090 RPQ M90976 or 7094 RPQ 880294) and the Sense Line Protect Feature (7090 RPQ W03471 or 7094 RPQ E21080) are both installed.

If the CPU is in both the transfer trap mode and protection mode, execution of any of the following instructions causes a protect trap instead of a transfer trap: ESNT, TCO, TCN, TEF, and TRC. If the CPU is in both the select trap mode and protection mode, execution of any instruction affected by both modes causes a select trap instead of a protect trap.

With the 7094 only, if the CPU is in both floating-point trap and protection modes, a DST instruction with an odd effective address outside the values in the bounds registers causes a protect trap. No floating-point trap is generated in this case.

Trap Priority is:

- Floating Point Trap
- Interval Timer Trap
- Protect Trap
- Direct Data Trap
- Data Channel Trap

Manual Operations

The relocate mode indicator, protect mode indicator, relocation register, lower bound register, and upper bound register are reset by: power-on reset, reset key, clear key, load cards key, and load tape key. The display storage key and enter instruction key are subject to the relocation mode but not the protect mode.

Publications

The following Special Systems Features Bulletins contain information of value when the Multiprogramming Package Feature is used:

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| 1. Additional Core Storage | L22-6636-1 |
| 2. Core Storage Clock and Interval Timer | L22-6554-2 |
| 3. Direct Data Connection | L22-6537-1 |

