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Identification.

The Processor Data Segment
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Purpose.

The Processor Data Segment is a "wired-in" block of core storage for each processor in the system. The Processor Data Segment that belongs to a specific processor contains information about that processor and the process it is executing and supplies the guaranteed available core space required for the Processor Stack. (See Section BK.1.03 for a description of the Processor Stack.) The Processor Data Segment is maintained by Swap-DBR (Section BJ.5.01) when a processor switches processes and by the System Interrupt Interceptor (Section BK.2.02) when a processor accepts an external interrupt. The Processor Data Segment is passed along from process to process and is always accessible to the process in execution.

Contents of the Processor Data Segment.

The Processor Data Segment is accessible to only one processor, so it needs no interlock. The contents of the Processor Data Segment are as follows:

1. The Processor Data Block. For convenience, the Processor Data Block is stored at the base of the Processor Data Segment. The Processor Data Block contains specific information about the processor to which the Processor Data Segment belongs. (See Section BK.1.02 for a description of the Processor Data Block.)

2. The Processor Stack. The Processor Stack is used by the System Interrupt Interceptor for safe-storing the processor state following an external interrupt and for calling the appropriate interrupt handling procedures.

Discussion.

For each processor in a multics system, the System Interrupt Interceptor must have access to an amount of guaranteed available core space in order to safe-store the processor state when an external interrupt occurs and in order to perform calls to the interrupt handling procedures. This guaranteed available core space is contained in the Processor Data Segment and is maintained as the Processor Stack. That the Processor Data Segment is the source of guaranteed available core space implies that a.) the Processor Data Segment is "wired" into core memory and cannot be paged out and b.) the Processor Data Segment contains enough core space to allow for the "worst case" occurrence of successive external interrupts and the maximum depth of calls to the interrupt handling procedures for each

interrupt. The amount of core space contained in a Processor Data Segment is determined on a processor by processor basis since certain processors accept a greater number of external interrupts than other processors in the system. (For example, drum interrupts are directed to a specific processor.)

Management of the Processor Data Segment.

The following list of actions taken in the management of the Processor Data Segment is presented here for clarification purposes only. Further details are given in Section BL, System Initialization, Section BJ.5, Process Switching, and Section BK.1.03, the Processor Stack.

When a multics system is initialized, a Processor Data Segment is created for each processor in the system and the following actions are taken:

1. A segment number is selected for the Processor Data Segment. All processes in the system use the same segment number to reference the respective Processor Data Segments.

2. Sufficient core space is allocated for each Processor Data Segment to allow for the worst cases described above.

3. The Processor Data Block is built for each processor in the system and stored at the base of the Processor Data Segment for that processor.

4. The Processor Stack is initialized for each processor in the system in the Processor Data Segment for that processor.

When Swap-DBR switches a processor from one process to another, it takes the following actions with regard to the Processor Data Segment:

1. Stores relevant information about the next process into the Processor Data Block.

2. Passes the segment descriptor word for the Processor Data Segment along from the process in execution to the next process.