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COMPUTATION CENTER
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TO: Computation Center Staff

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SUBJECT: Latest Write-up on M.I.T. 7090 RPQ for Relocation and Protection Modes

The following write-up is the latest material received from IBM on the 7090 RPQ.

All superscript numbers refer to the Errata and Clarification Sheet at the end. These have been prepared to make this write-up serve as a guide to programmers working with the RPQ and represents our understanding of the RPQ.

RPQ E07291

SPECIFICATIONS FOR A MULTIPROGRAMMING PACKAGE FOR THE 7090 SYSTEM

I. PURPOSE

This feature performs two (2) relatively independent functions for the 7090 which are required for efficient multiprogramming or time-sharing of the system. They are: automatic relocation and variable bounds memory protection. Both functions are provided without extending the execution time of any 7090 instruction.

II. DESCRIPTION

A. Automatic Relocation

A seven bit register (relocation register) is provided. When in the relocation mode, these seven bits are added to the high order 7 bits of all memory addresses, including "I" cycles generated by the CPU. A program, therefore, written to execute in a particular set of storage locations can be moved along with its data to any other location (the increment being a multiple of 256) and executed there.

Two new instructions are provided:

1) LRI - Load Relocation Indicators

+0562.....Y

Indicators.....Mode indicator under the CE panel of the 7151 console.

Timing.....2 cycles

Execution of this instruction will place bits 21-27 of Y into the relocation register. In addition, the CPU is placed in the relocation mode if no bit is specified in th S position of location Y. ~~Exiting from the relocation mode can be done by inserting a bit in the S position of location Y.~~ This method of exiting is only effective if the CPU is out of the memory protect mode. The instructio is indexable and indirectly addressable. Relocation will not take place until after the instruction following the LRI instruction has been executed. Should an "Execute" instruction be given immediately following the LRI instruction, and additional instruction delay will be effective. A program sequence may be:

Execution of an LRT Y where Y has a 1 in the S-position causes the computer to leave the relocation mode

LRI.....Y
2 EXC.....Z
3 Z = TRA.....X*

LRI Y
XEC Z
where Z is... TRA X

(X will be relocated and the next instruction will be taken from X relocated)

No I/O traps can occur between the LRI instruction and the instruction following it.

Execution of any trap will take the CPU out of the relocation mode. In addition:

If the CPU is in the relocation mode:

a) All traps will inhibit I/O traps until restored or enabled.

b) Execution of the interval timer trap (RPQ F89349) will store a "1" in position 17 of location 6.

2) SRI - Store Relocation Indicators

17 -6XX.....Y → -0601.....Y
Indicators.....None
Timing.....2 cycles

Exeuction of this instruction will store the contents of the relocation register into positions 21-27 of location Y. If the CPU is in the relocation mode, a "1" will be stored in position "1" of location Y. The instruction is indexable and indirectly addressable. the instruction counter (IC) always takes on and shows at the console only unrelocated values, when in the relocation mode.

B. Variable Bounds Memory Protection

Two seven bit registers are provided, designated the Lower and Upper Bound registers. When in the protection mode, any CPU generated memory address, including "I" cycles, is compared against the contents of these two registers. The comparison is made after address relocation has taken place, if any. If the address is less than the contents of the lower bound register or equal to or greater than the contents of the upper bound register, a trap is generated storing the actual (unrelocated) value of the program counter plus one in the address portion of location 32_8 and transferring control to location 33_8. The execution of the instruction causing the trap is blocked. In addition, execution of any trap will take the CPU out of both the protection and relocation modes, leaving the contents of the relocation and bounds registers unchanged. Two new instructions are provided:

In other words, if the instruction at location A violates the bounds, its execution is blocked, the trap occurs during the "I" cycle of the instruction at A+1

1) LPI - Load Protect Indicators

-0564.....Y
Indicators.....Mode indicator under the CE Panel of the 7151 console
Timing.....2 cycles

Execution of this instruction will place bits 3-9 and 21-27 into the upper and lower bounds registers, respectively. In addition, the CPU is placed into the protect mode, if no bit is specified in the "S" position of location Y. If a bit is placed in the "S" position of location Y, the CPU will be prevented from entering the protect mode, however, the bounds registers will be loaded. The instruction is indexable and indirectly addressable. The protect mode does not become effective until after the' instruction following the LPI instruction has been executed. Should an "Execute" instruction be given immediately following the LPI instruction, an additional instruction delay will be effective before the protect mode is entered. No I/O traps can occur between the LPI instruction and the instruction following it.

Execution of any trap will take the CPU out of the memory protect mode. The larger magnitude number should be placed in the upper bound register in order for the device to operate correctly.

The instruction is indexable and indirectly addressable.

2) SPI - Store Protect Indicators

-0604.....Y
Indicators.....None
Timing.....2 cycles

Execution of this instruction will place the contents of the upper and lower bounds registers into positions 3-9 and 21-27 of location Y, respectively. If the CPU is in the protect mode, a "I" will be stored in position 2 of location Y. The instruction is indexable and indirectly addressable.

C. Trapping

When in the protection mode, decoding of the following instructions will cause a memory protect trap.

LPI, LRI, ENB, RCT, RDC, & RCH RLCH, LCH, TEFN, TRCN, RUN, SDN, WEF, BSF, BSR, REW, RDS, WRS, I/O Sense, RTT, ~~EOT, BOT,~~ ECTM, ESNT, IOT, LTM, ETM, ESTM, EFTM, LFTM. TRC, ETT, BTT

An exception to this would be if an ECTM or ESTM instruction is given prior to entering the protect mode, then if an instruction violating either of these modes (RTT, CPY, etc.) is given while in the protect mode, instead of executing a memory protect trap, the normal traps will occur and the CPU will leave the protect mode.

A transfer out of bounds is trapped 10 such that ~~immediately and~~ the execution of the transfer is blocked. If such a transfer is executed in the transfer trapping mode (the ETM instruction having been given before entering the memory protect mode) the transfer trap will take place first and reset the protect and relocation mode.

The effective delay in execution and protection against I/O 11 ~~or~~ Direct Data traps is extended if the instruction following also provides a one instruction grace period. It is expected that a normal exit from the monitor will be:

including

```
    ENB     A
    LPI     B
    LRI     C
12  TRA*    ~~32~~ 26
```

No I/O or Direct Data, traps will occur until after the TRA has been executed. The protection and relocation will begin on the "I" cycle following the TRA.

Trap priority is as follows:

1) Floating Point Trap
2) Interval Timer Trap
3) Memory Protect Trap
4) Direct Data Trap/Manual Interrupt (Enabled)
5) Data Channel (I/O) Trap

For machines with B/M 570220 (Storage Cell Clock), the incrementing of core storage location 0005 will not be affected by either the protect or relocation mode.

D. Manual Operations

1. If the "Display Storage Key" is depressed while in the relocation mode, the contents of the relocated 14 ~~address~~ location will be displayed.

2. If the "Enter Instruction Key" is depressed while in the protect and relocation mode, the 15 ~~address of~~ specified location for the instruction will be relocated, however, instructions can be entered into out of bound regions 16 without ~~effecting~~ causing a memory protect trap to occur.

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11/28/61

ERRATA AND CLARIFICATION SHEET

1 Replace this sentence by:

"Execution of an LRI Y where Y has a 1 in the S position causes the comp ter to leave the relocation mode; this"

2 "XEC" instead of "EXC"

3 Replace line with:

"where Z is TRA X"

4 "relocation" instead of "relocate"

5 Add this paragraph:

"The instruction counter (ILC) always takes on and shows at the console only unrelocated values, when in the relocation mode."

6 Add:

(32 and 33 are octal references).

7 Add:

"In other words, if the instruction at location A violates the bounds, its execution is blocked; the trap occurs during the "I" cycle of the instruction at location, A+1."

8 "RCH" instead of "RLCH"

9 "TRC, ETT, BTT" instead of "EOT and BOT".

10 "Such that" instead of "immediately and"

11 ", including Direct Data," instead of "or Direct Data"

12 "TRA* 26" instead of "TRA* 32"

13 ", including Direct Data," instead of "or Direct Data"

14 "location" instead of "address"

15 "specified location for" instead of "address of"

16 Replace last line:

Without causing a memory trap to occur.

17 Replace line with:

-0601.....Y