Special Systems Features Bulletin

Direct Data Connection for IBM 7090, RPQ M90976

The Direct Data Connection permits connection of non-IBM input-output devices to an IBM 7090 Data Processing System. Transfer of data between such devices and the 7090 is the same as with standard IBM input-output units.

The Direct Data Connection, when installed on an IBM 7090 Data Processing System, provides a communication link with analog/digital converters, telegraph or telephone lines, radar, telemeters, microwave links, or other non-IBM input-output devices. The Direct Data Connection consists basically of a direct data interrupt signal, 36 data transfer lines, and 20 sense lines. It permits real time or direct transmission of data between core storage of the 7090 and external devices at data transmission rates up to 152,777 words per second.

A direct data interrupt signal from the non-IBM device to the computer automatically interrupts normal program execution and transfers program control to storage location 0004. Upon interruption, the address of the next normal instruction to be executed replaces the address part of location 0003 so that re-entry to the normal program is possible after processing the direct data.

Transfer of data between any associated IBM input-output device and core storage of the 7090 system is accomplished over 36 data lines. These lines are brought out to connectors that may be cable-connected to the non-IBM input-output device.

The sense lines, which are under program control, provide a data transfer between any core storage address and the Direct Data Connection. Ten lines are for input control and another ten are for output control.

The Direct Data Connection is installed on any IBM 7607 II Data Channel and uses the data register of that particular data channel as its buffer. Standard data channel commands are used with the Direct Data Connection.

TRAP AND INTERRUPT OPERATION

Several types of trap operations, in addition to direct data interrupt, can occur on the 7090. Their priority is: (1) Floating Point Trap, (2) Direct Data Interrupt, (3) External Signal Interrupt, (4) Data Channel Trap.

NOTE: Availability of this feature can be determined by requesting a price quotation from IBM. Copies of the bulletin are only available from IBM Region Sales Engineering Departments. This description is subject to modification by engineering developments.

Floating Point Trap

A floating point trap is given priority over any other trap because certain conditions causing the trap must be stored. This operation, however, delays execution of any other trap by only two computer cycles. If a direct data interrupt occurs during a floating point instruction in which a floating point trap occurs, the contents of the instruction counter are stored in the address part of location 0000 (floating point trap store address), and 0010 (floating point trap transfer address) is stored in the address part of storage location 0003 (interrupt store address). The program then transfers to the instruction at storage location 0004.

Direct Data Interrupt

A direct data interrupt is given priority over a data channel trap interrupt because some uses of the direct data interrupt may demand immediate control of the 7090. A data channel trap can be delayed without interfering with I/O operation. Executing the direct data interrupt causes all further interrupts and data channel traps to be inhibited until a restore or a new enable instruction is given. If the Direct Data Connection is installed on more than one data channel, interrupts occurring simultaneously will be executed simultaneously. The programmer, by checking the decrement portion of storage location 0003, can determine if one or more traps occurred and which data channel inhibited them.

External Interrupt

The 7090, as part of its standard equipment, has an external signal interrupt. When used, regardless of the purpose, it is given the same priority as a direct data interrupt. An external interrupt trap transfers to the same storage address as a direct data interrupt. However, no indication is stored in the decrement portion of location 0003. A programmer has difficulty if a direct data interrupt and an external interrupt occur simultaneously because only an indication of the direct data interrupt appears. If his program is coded to check the decrement of storage location 0003, the programmer would see something in the decrement and assume that an external interrupt did not occur. Execution of an external interrupt does not inhibit further external interrupts, direct data interrupts, or data channel traps.

Data Channel Trap

A data channel trap has least priority in the 7090 system. Delay of a channel trap does not interfere with I-O operation because every data channel trap is accompanied by a disconnect condition within the channel. Executing a data channel trap causes all further data channel traps and direct data interrupts to be inhibited until a restore or enable instruction is given. A programmer should be cautious about using direct data interrupts and data channel traps because it may be necessary to re-enable direct data interrupts immediately after the execution of a data channel trap.

DIRECT DATA CONDUCTOR CABLES

Six cables of 20 conductors each are used with the Direct Data Connection. Conductor pin numbers are located as shown in Table I. The use of each cable wire is as follows:

Output Data Bus

The output data bus consists of 36 lines connected to the outputs of the data register. These lines are not logically isolated from the data register when the direct data device is not selected.

Input Data Bus

The input data bus consists of 36 lines connected to the inputs of the data register. These lines are isolated from the data register when the direct data device is not selected.

Read Select

This signal is the output of the direct data read select trigger that is turned on by the execution of the direct data read select instruction. This signal sets the information flow between the data channel register and core storage. Any condition causing a disconnect will terminate this signal.

Write Select

This signal is the output of the direct data write select trigger that is turned on by the execution of the direct data write select instruction. This signal sets the information flow between core storage and the data channel register. Any condition causing a disconnect will terminate this signal.

Direct Data Demand

This signal is generated by the external device. In the direct data read operation, this signal indicates to the data channel that the external device has established the signal levels on the input data buses, and causes the data on the buses to enter the data register within the data channel. In the direct data write operation, this signal indicates to the data channel that the word on the output data buses has been accepted by the external device.

Under word count control, the number of words, plus one, must be given unless a reset or reset and load channel instruction is used, to assure transfer of the last word.

If a direct data demand is given when the channel ready-read signal is down on a read operation, or the channel-ready write signal is down on a write operation, a data channel I-O check will occur, thus initiating a disconnect.

Cable No	Conductor No.	Signal
1	1	Output Data Bus 1
1	2	" " 2
1	3	" " 3
1	4	" " 4
1	5	" " 5
1	6	" " 6
1	7	" " 7
1	8	" " 8
1	9	" " 9
1	10	" " 10
1	11	" " 11
1	12	" " 12
1	13	" " 13
1	14	" " 14
1	15	" " 15
1	16	" " 16
1	17	" " 17
1	18	" " 18
1	19	SPARE
1	20	SPARE
2	1	Output Data Bus 19
2	2	" " 20
2	3	" " 21
2	4	" " 22
2	5	" " 23
2	6	" " 24
2	7	" " 25
2	8	" " 26
2	9	" " 27
2	10	" " 28
2	11	" " 29
2	12	" " 30
2	13	" " 31
2	14	" " 32
2	15	" " 33
2	16	" " 34
2	17	" " 35
2	18	" " 36
2	19	SPARE
2	20	SPARE

Cable No.	Conductor No.	Signal
3	1	Input Data Bus 1
3	2	" " 2
3	3	" " 3
3	4	" " 4
3	5	" " 5
3	6	" " 6
3	7	" " 7
3	8	" " 8
3	9	" " 9
3	10	" " 10
3	11	" " 11
3	12	" " 12
3	13	" " 13
3	14	" " 14
3	15	" " 15
3	16	" " 16
3	17	" " 17
3	18	" " 18
3	19	SPARE
3	20	SPARE
4	1	Input Data Bus 19
4	2	" " 20
4	3	" " 21
4	4	" " 22
4	5	" " 23
4	6	" " 24
4	7	" " 25
4	8	" " 26
4	9	" " 27
4	10	" " 28
4	11	" " 29
4	12	" " 30
4	13	" " 31
4	14	" " 32
4	15	" " 33
4	16	" " 34
4	17	" " 35
4	18	" " 36
4	19	SPARE
4	20	SPARE

Cable No.	Conductor No.	Signal
5	1	Sense Output 1 (Stg Pos 8)
5	2	" " 2 " 9
5	3	" " 3 " 10
5	4	" " 4 " 11
5	5	" " 5 " 12
5	6	" " 6 " 13
5	7	" " 7 " 14
5	8	" " 8 " 15
5	9	" " 9 " 16
5	10	" " 10 " 17
5	11	Sense Input 1 " 8
5	12	" " 2 " 9
5	13	" " 3 " 10
5	14	" " 4 " 11
5	15	" " 5 " 12
5	16	" " 6 " 13
5	17	" " 7 " 14
5	18	" " 8 " 15
5	19	" " 9 " 16
5	20	" " 10 " 17
6	1	Direct Data Demand
6	2	End of File
6	3	End of Record
6	4	Word Count Zero and Record Control
6	5	Channel Ready Read
6	6	Channel Ready Write
6	7	Sense Output Reset
6	8	Write Select
6	9	Read Select
6	10	Interrupt
6	11	Sense Input Reset
6	12	SPARE
6	13	"
6	14	"
6	15	"
6	16	"
6	17	"
6	18	"
6	19	"
6	20	SPARE

TABLE I.

Channel Ready-Read

This signal indicates that the data channel is ready to accept a word from the external device. This signal can be terminated by any of the following:

1. Direct Data Demand: the channel ready-read signal is terminated within one machine cycle (2.18 microseconds) of the fall of this signal. The signal is restored during the machine cycle on which the data word is placed in storage (provided the word count is not zero). If X number of other channels are in use simultaneously with computing, restoration of this signal can be delayed as much as 3X + 5 machine cycles. This delay is caused by prior demands from these other channels, plus the time required to execute the longest CPU instruction; the delay is, therefore, a function of the computer program.

With no other channel activity and the shortest delay in the CPU, the signal is restored within two machine cycles. To insure a minimum delay in the CPU, continuous execution of a transfer on channel in operation instruction should be given.

If a direct data demand pulse is given prior to the restoration of the channel ready-read signal, the channel causes the I-O check indicator to be turned on in the CPU. Loss of information occurs because the channel is disconnected. The I-O check indicator can be tested by the computer program.

2. Any disconnect within the channel.
3. A reset and load channel instruction for the channel.

Channel Ready-Write

This signal indicates that the data channel has placed a 36-bit word on the data bus during a direct data write operation. Sufficient time should be allowed for the data bus to attain its full static level before sampling this information into the external device. This signal can be terminated by any of the following:

1. Direct Data Demand: the channel read-write signal is terminated within one machine cycle of the fall of this signal. The signal is restored during the machine cycle on which the next data word is called from storage. For timing considerations see Channel Ready-Read.
2. Any disconnect within a channel.
3. A reset and load channel instruction for the channel.

Word Count Zero and Record Control

This signal indicates to the external device the earliest time following a word count zero condition at which an end-of-record (EOR) pulse may be given. A storage reference cycle used to store information read by the computer does not necessarily follow the demand pulse which set the information into the data register. It can be delayed by other channel activity or by CPU instructions. The word count zero condition occurs on this final storage cycle. If the EOR pulse occurs prior to the word count zero and record control signal, loss of data results.

This signal line is up when the word count of the data channel is zero and the channel is under record control (indicator 1 on and the external device selected).

End of Record

This signal is generated by the external device. If the channel is under IORP or IOSP control, the rise of this signal line causes the channel to obtain a new control word. If the channel is under IORT or IOST control, the rise of this signal line causes a new control word to be obtained from the CPU if a load channel or reset and load channel instruction is waiting; otherwise it causes a disconnect. If the data channel trap (special feature) is on the computer, IORT or IOST control can be used to cause an interrupt of the CPU program.

End of File

This signal is generated by the external device. The rise of the signal line causes an immediate data channel disconnect and turns on the end-of-file indicator.

If the data channel trap is on the computer, an interrupt may be initiated if desired.

Sense Output

Execution of the present sense lines (PSL) instruction in the computer program conditions these lines. The ten lines correspond to bits in positions 8 through 17 of the storage location specified by the present sense lines instruction. The PSL instruction may be given at any time, whether the channel is selected or not.

Sense Input

Execution of the store sense lines (SSL) instruction causes sampling of the ten sense input lines. Information placed on these lines by the external device is stored in positions 8 through 17 of the storage location specified by the address of the store sense lines instruction. The SSL instruction may be given at any time, whether the channel is selected or not.

Sense lines may be used for address selection of more than one external device, or as a more limited form of data transmission without tying up the data channel. Possible applications include low data rate devices such as serial readers, punches, paper tape, and typewriter. By interrupting on each character, communication can be maintained with minimum loss of computer time and without delaying other input-output operations.

Sense Output Reset

This signal line provides a pulse that precedes the sense output pulse by three microseconds. It can be used to reset a register in the external device.

Sense Input Reset

This signal is a pulse which comes after the storage of sense inputs upon execution of store sense lines instructions.

Interrupt--Input

The rise on this line of a signal produced by the external device turns on the interrupt trigger in the data channel. If the channel had been enabled by the enable instruction and no other data channel trap had occurred, a trap in the computer program occurs during the instruction (I) time cycle of the next instruction to be executed except for the following special conditions:

1. If a floating point trap is being executed at the time an interrupt is received, the interrupt trap will be delayed until the following I time.
2. Upon execution of a restore channel traps or an enable instruction, an interrupt will not cause a trap until two I times later instead of the following I time. This allows an indirectly addressed transfer instruction to be executed.
3. Upon execution of a read or write select (other than direct data address x240), an interrupt will not cause a trap until two I times later. This allows a reset and load channel instruction to be executed.
4. Upon execution of an execute instruction, an interrupt will not cause a trap until the instruction to be executed is actually completed.

The contents of the instruction counter are stored in the address portion of storage location 0003, and the next instruction is taken from location 0004. A one (1) is placed in the following positions of the decrement portion of storage location 0003 to indicate which channel caused the trap.

Channel Originating Trap	Decrement Positions
A	17
B	16
C	15
D	14
E	13
F	12
G	11
H	10

Traps occurring simultaneously in two or three channels present an OR configuration in the decrement portion of location 0003.

Upon execution of an interrupt trap, the computer is inhibited against further interrupt traps or data channel traps. If an interrupt is received while the data channel is either inhibited or not enabled, the interrupt is remembered until one of the following conditions is met:

1. Execution of an enable or restore instruction enabling the specific data channel: this resets the interrupt trigger and allows the trap to be executed after execution of the instruction following the restore or enable instruction.

2. Execution of a direct data write or read select instruction: this resets the interrupt trigger.

3. A machine reset: if an interrupt trap occurs during the execution of a floating point trap, the interrupt is delayed until the following I time.

CABLE CONNECTOR

The coaxial low voltage connector is composed of a machine half (IBM 598027) and cable half. The machine half is slotted and normally mounted as shown in Figure 1. Since six of the connectors are used, different mounting arrangements may be used. A latch mechanism insures proper orientation and engagement of both halves of the connector. Parts and tools required for the connection of this device are:

Name	Number	Quantity
Connector Block Assembly	598027	6
Male Braid Connector	595986	103
Miniature Hyfen Sockets	595987	103
Outer Hy Rings	595981	103
Burndy Tool	M8ND	
Burndy Tool	RX4-1	
Burndy Tool Die	N22RVT	

Complete assembly details are given in IBM Engineering Specifications 985441. Cable lengths specified are measured from the base of the IBM 7607 II to the connectors in the external device. All six cables exit from the center of the cable access hole under the 7607 II and each of the six cables must be specified individually.

COMPUTER INSTRUCTIONS

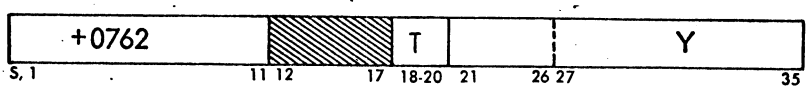
RCT--Restore Channel Traps

Description: Upon execution of a data channel or interrupt trap, all data channels are inhibited from executing additional traps. This instruction allows traps to occur as specified by the previous enable instruction.

Timing: 2 cycles.

Execution: Because the address part of this instruction is a part of the operation code, modification by an index register may change the operation code.

RDS--Read Select



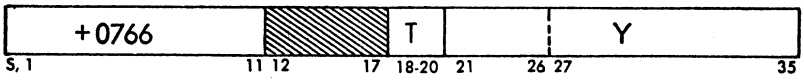
Description: This instruction causes the computer to prepare to read information from the I-O device specified by the Y portion of the read instruction into core storage. Y also specifies the data channel to which the I-O device is attached.

Timing: 2 cycles (CPU execution time)

Execution: Positions 27-35 of the address part of this instruction are subject to address modification. The address designated by Y is:

Data Channel	Octal	Decimal
A	1240	0672
B	2240	1184
C	3240	1696
D	4240	2208
E	5240	2720
F	6240	3232
G	7240	3744
H	10240	4256

WRS--Write Select



Description: This instruction causes the computer to prepare to write information from storage to the I-O device specified by Y. Y also specifies the data channel to which the I-O device is attached.

Timing: 2 cycles (CPU execution)

Execution: Positions 27-35 of the address part of this instruction are subject to address modification. The address designated by Y is:

Data Channel	Octal	Decimal
A	1240	0672
B	2240	1184
C	3240	1696
D	4240	2208
E	5240	2720
F	6240	3232
G	7240	3744
H	10240	4256

PSL--Present Sense Lines

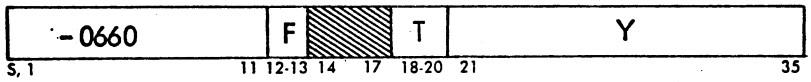
Description: A separate instruction is provided for each data channel and refers to positions 8 through 17 of the designated storage address Y. The instruction presents this bit configuration in pulse form to the direct data connection. The bit configuration is preceded by a reset pulse on a separate line.

Timing: 3 cycles.

Execution: Data channel designations with the proper operation codes are:

0664	Present sense lines, Channel A
-0664	Present sense lines, Channel B
0665	Present sense lines, Channel C
-0665	Present sense lines, Channel D
0666	Present sense lines, Channel E
-0666	Present sense lines, Channel F
0667	Present sense lines, Channel G
-0667	Present sense lines, Channel H

SSL--Store Sense Lines



Description: A separate instruction is provided for each data channel. The instruction samples the static sense lines from the direct data I-O device and stores their information in positions 8 through 17 of the storage location specified by Y. A plus voltage level on the lines is decoded as a 1 bit.

Timing: 2 cycles.

Execution: Data channel designations with proper operation codes are:

0660	Store sense lines, Channel A
-0660	Store sense lines, Channel B
0661	Store sense lines, Channel C
-0661	Store sense lines, Channel D
0662	Store sense lines, Channel E
-0662	Store sense lines, Channel F
0663	Store sense lines, Channel G
-0663	Store sense lines, Channel H

ENB--Enable from Y

Description: When this instruction is executed, the contents of location Y determine which data channels may cause a trapping operation.

Timing: 2 cycles

Execution: An interrupt on a given channel is enabled if the appropriate position of storage location Y contains a 1:

Enabled Channel	Bit Position (Y)
A	26
B	25
C	24
D	23
E	22
F	21
G	20
H	19

An enable instruction with 0's in any of the control positions (26-19) of location Y disables the interrupt on the corresponding channel if the interrupt was enabled by a previous enable instruction. To enable interrupts of a channel, a 1 is placed in the appropriate control position of storage location Y. A computer reset disables all channels.

General Programming Information

The fastest IBM input-output device available as standard equipment on the 7090 system has a data rate of one word approximately every 67.5 microseconds. If the external device to be used with the direct data connection has a data rate no faster than these figures, no further programming restrictions are applicable. When data rates from these external devices exceed the fastest IBM data rates, other data channel activity must be curtailed. To achieve the maximum data rate of 152,777 words per second on the 7090, all other data channel operation must be stopped and the delay (due to CPU instruction timing) must be minimized. To insure minimum delay in the CPU, continuous execution of any two cycle instructions (for example TCO) is required.

To determine the maximum data rate possible with a given computer input-output configuration, include three machine cycles for each channel in use, plus five machine cycles for the longest CPU instruction. Multiply the number of cycles by the basic cycle (2.18) to obtain a figure in microseconds. Divide 1,000,000 by this figure to obtain the number of words per second. Allow a safety factor percentage for random fluctuations in computer timings.

Direct Data Program Example

As an example of Direct Data Connection use with a computer, assume an application in which normal computer activity is to be interrupted by a signal that will alert the computer to accept data from a wind tunnel test stand. Digital results of the test are to be recorded on magnetic tape for future data reduction, and the computer is to be returned to its initial status.

The test stand operator signals the computer by pressing a ready button. The computer, when available, responds by turning on a light at the test stand. The test operator begins the test.

In addition to the Direct Data Connection, assume that a device such as an analog/digital converter is available to the computer. This device encodes the test data and presents them to the computer when available. One tape unit on the channel not equipped with the Direct Data Connection must be available to the direct data program. The present computing problem may be dumped on a magnetic tape so that it may be recalled when the direct data problem is completed.

Normal computer programs must obey the usual conventions when using data channel traps. These conventions are:

1. All reset or reset and load channel instructions must be given immediately after the select instruction, and each select instruction must be preceded by a transfer on channel in operation instruction.
2. The enable instruction should be used through a subroutine so that the direct data interrupt is not accidentally disabled.
3. A section of core storage containing part of the direct data program must be used.
4. A standard location must be used to hold the unit address associated with the enable instruction.

When using data channel traps, save all program and hardware indications. Before this is done, however, all current stacked data channel operations should be executed before going into the direct data program. An instruction sequence to accomplish delaying the direct data program until all channel operations are completed is:

```
      RCT
      NOP
(A)   TCOA    A
      TCOB    A
      TCOA    A
      TCOB    A
```

This sequence delays execution of the direct data program until data channels A and B are not in operation. Because program control is not returned to the main program, no new tasks for data channels are assigned. Therefore, the channels rapidly come to a stop. The time delay is usually no longer than a few seconds; however, if a large area of core storage is processed by the on-line card punch, the time delay might exceed a

few minutes. The enable instruction should enable all channels previously enabled with the exception of the direct data interrupt, to prevent the test stand operator from initiating a new interrupt condition.

After all channel operations are complete, the status of the entire central processing unit and the status of the data channel indicator to be used must be saved. Indicators such as end-of-file, tape check, input-output check, and the contents of the channel location and address registers are among the status indicators saved. All pertinent central processing unit registers and the necessary portion of core storage needed to continue normal processing can be written on a special magnetic tape.

The direct data program can then be read from its tape into core storage; the computer is then ready to process whatever direct data is sent from the test stand. The computer, at this point, informs both the test stand and program operators that it is ready to work on the wind tunnel problem. When processing is complete on the direct data, the results are written on tape for future reference. The computer can restore the original program and computer status to its interruption point.

After all indicators, core storage, and magnetic tapes are restored, the computer executes a transfer to location 0003, where it picks up the address of the next instruction in the original program that had to be executed (this address was stored here when the interrupt occurred).

ELECTRONIC SPECIFICATIONS

Two signal level options are available and must be specified at least 90 days prior to delivery of the direct data connection. Once specified, they cannot be changed.

Option I--Current Mode

All lines are current mode signals to IBM specifications. These signals are standard N lines with a nominal ±.4 volts swing around ground (binary 0 = -.4, binary 1 = +.4 volts). Inputs and outputs for the 7090 shall be the equivalent of a standard P logic block (IBM 371211 class) driving a line terminator (IBM 371242) or equivalent. The cable supplied with this option is a 93 ohm coaxial cable, maximum length of 150 feet (10 feet of this is internal to the 7607 II).

Option II--Voltage Mode

All lines are voltage mode signals to IBM specifications. These signals have a nominal +8 volt swing from ground. Signals are:

Inputs--voltage	8 ± 3 volts = binary 1
	0 ± 1.5 volts = binary 0
--Termination	93 ohms ± 2% in parallel with 100uuf ± 100%
Outputs--voltage	8 ± 2 volts = binary 1
	0 ± .5 volts = binary 0
--Termination	150 feet of RG62 B/U coaxial wire terminated with 93 ± 4.65 ohms in parallel with a maximum of 150uuf or electrical equivalent.

Signal Timings

Timing specifications are for either option. Equipment destruction may occur if these parameters are exceeded. Variable duration signals are governed by the occurrence of other signals. In no case should the rise or fall time of any signal exceed 1.20 microseconds. Equipment destruction may occur if this specification is not followed. Rise time is defined as the time required to go from 10% to 90% of the nominal levels (option I, -.4 to +.4 volts; option II, +.5 to +6 volts). Fall time is defined as the time required to go from 90% to 10% of nominal levels. Rise and fall times must be compatible with pulse widths for maximum transfer rates.

Pulse Width. Pulse width is defined as the length of time a signal is above the minimal signal level.

7090 Inputs and Timings:

Direct Data Demand	1.26 ± .54 microseconds*
Interrupt	Minimum .4 microseconds
End of Record	Minimum 2.54 microseconds
End of File	Minimum .4 microseconds
Sense Inputs	Variable

*For maximum transfer rate of 152,777 words per second.

7090 Outputs and Timings:

Read Select	Variable
Write Select	Variable
Channel Ready-Read	Variable
Channel Ready-Write	Variable
Word Count Zero and Record Control	Variable
Sense Outpus	3.33 microseconds
Sense Outputs Reset	.72 microseconds*
Sense Input Reset	1.26 microseconds**

* Time between fall of sense output reset to rise of sense outputs is 0 ± .25 microseconds

** Sense Input reset rises 1.0 microseconds after the gate which places the sense inputs into storage falls.

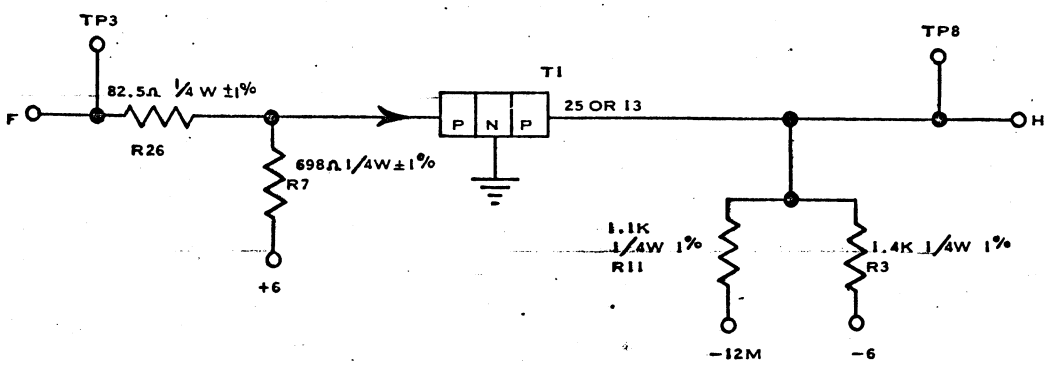


Figure 1. Alloy "N" Terminator, Part Number 371242

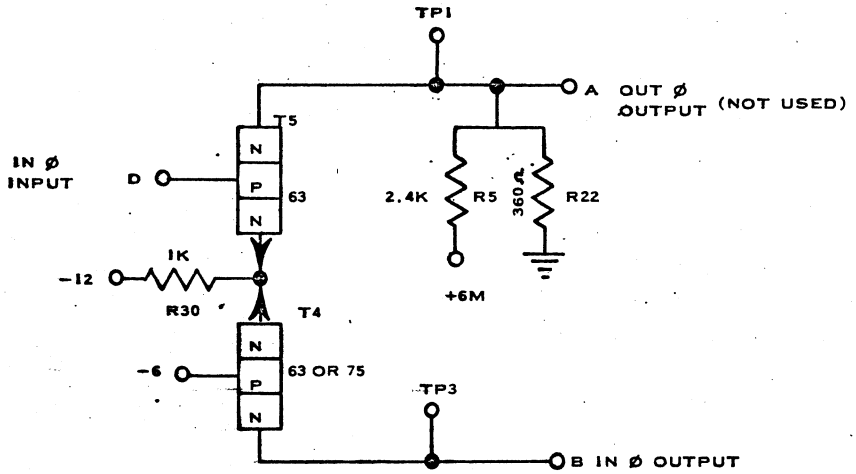


Figure 2. Alloy-One Way "P", Part Number 371211

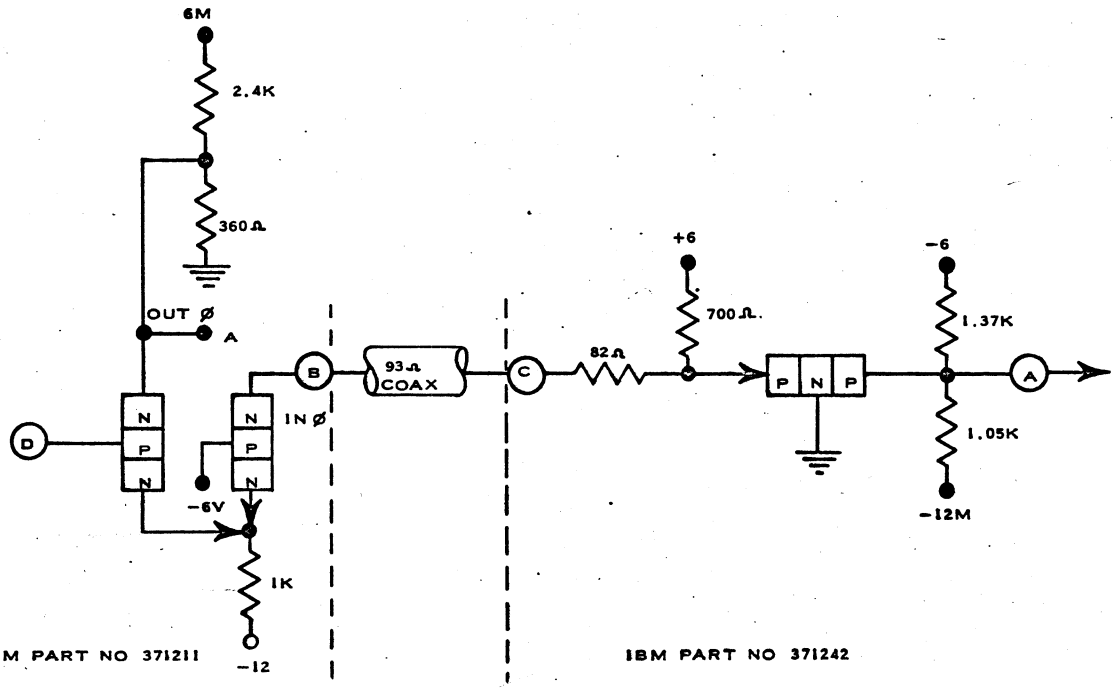


Figure 3. Line Terminating Circuit