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Identification

Major Module Configuration Table
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Purpose

The Major Module Configuration Table is a system-wide data base, accessible to the Multics Initializer and diagnostic routines. It contains a complete description of the current major module configuration, i.e., cable arrangements, plugboard, settings, and switch settings. There is also some information that could be of interest to the users (system identification, etc.). The table is built up by the Multics initializer and afterwards is read only, unless the operator commands a reconfiguration.

This section first discusses identification of devices in the configuration. This is followed by a list of the data items in the Major Module Configuration Table, and an EPL declaration for the table.

Discussion

The unique identification of a device (system controller, clock, processor, GIOC, EMM) is its serial number which never will be changed. For processors, there exists an abbreviation, the processor tag (BK.3.01). This tag normally will not be changed unless some patch board in the processor are changed. The local name of a device ("A" to "H" for all modules) is assigned by the installation staff and reflects in a certain way the hardware cabling among the devices. These names too will not be changed unless the hardware cabling is rearranged. The index (e.g. processor index) is assigned by the Multics initializer and may be different each time the system is loaded. The only way the Multics System refers to a specific device is through this index. The other items might be regarded as restricted synonyms as in the table below.

item	depends on	changes	set by
unique identification	serial number	never	manufactory
tag (only processors)		processor wiring	installation staff
local name	hardware cabling	upon rearrangement of hardware cabling	installation staff
index	initialization	each time the system is loaded	Major Module Configuration Table initializer

Contents of System Configuration Table

1. System identification (sys_name). This item identifies unambiguously the version of Multics currently loaded.

2. Calendar time of the issue of the Multics System Tape (sys_date). This date will be set by the program which creates a new Multics System Tape.

3. Calendar time (start_date) the currently running Multics System was loaded (initialized). This date will be set by the Multics Initializer.

4. Configuration identification (conf_id). Name of the configuration loadlist selected by the operator.

5. Hardcore supervisor identification (supv_id). Name of the supervisor loadlist selected by the operator.

6. Number of System controllers (nsys_contrs).

7. Number of System clocks (nclocks).

8. Number of processors (nprocessors).

9. Number of GIOC's (ngiocs).

10. Number of drums (ndrums).

For each System controller:

Memory size (size) in multiples of 1024.

For each port there is a two-part identification of the module connected to that port giving module type and module number. For example, for port 4, "type" may be "10001"b, while "index" may be "3". This means that Processor 3 is attached to port 4. A table of bit patterns for each module type is given below.

The port number of the control processor (contr_proc_port). This item describes which processor will be interrupted.

The system controller's local name (name). This item is an arbitrary character string assigned by the installation staff.

Unique identification of the System controller (id).

Interrupt assignment for the production clock. There are two different interrupt conditions of the clock, trouble and wakeup. Each interrupt condition has an interrupt cell assigned (1 out of 32). This item specifies which interrupt cell will be set when the interrupt condition occurs.

Identification of the system controller (sys_contr) in which the production clock resides. (In case of a prototype clock, this item specifies the system controller which the interrupt will be reflected to. This reflection is done by the control processor of the prototype clock.)

11. Index of system clock (i_sys_clock).

12. Index of bootload processor (i_bl_cpu).

13. Index of bootload GIOC (i_bl_gioc).

Real residence of the prototype clock (sys_contrx). This item is required only for the prototype clocks.

For each processor:

The base_ptr of the processor pointing to the base location of the fault vector (BK.1.04).

Information about what is connected to which port. (Prototype clock 2, system controller A, etc.) (See "bit pattern" in this document.)

The processor's local name.

Processor identification (its serial number).

Processor tag (BK.3.01).

Port for interrupts (int_port). The processor expects interrupts through the specified port.

For each GIOC:

The base address of the GIOC (base_ptr). This address points to the base location of all the mailboxes used by any channel of the GIOC.

Information about what is connected to which port (e.g. system controller B on port 3, port 4 disconnected, etc.) (See "bit pattern" in this document.)

Interrupt cell assignment (init_cell). Each status channel is able to set 1 out of 32 interrupt cells. There are restrictions for status 0 and 1 (BC 1.04). This item specifies which cell will be set by which channel. The GIOC is able to set interrupt cells, only in the system controller which contains the memory location of the GIOC base address.

The largest channel number (largest_channel). This item is used in order to check whether mailbox areas and/or interrupt vectors are overlapping.

The GIOC's local name.

GIOC identification (its serial number.)

For each drum:

The base address (base_ptr). Points to base location of the mailboxes.

Information about what is connected on which port.

Interrupt cell assignment. Upon detecting one of the three possible interrupt conditions (program, data or trouble), the drum will set the specified interrupt cells in the system controller which the memory location corresponding to the drum base address resides.

The drum's local name.

Unique identification of the drum (serial number).

Per System Data:

There are 5 interrupt cells set by a processor (initialize, pre_empt, time_out, quit, sys_trouble). Assume processor 1 has to pre_empt processor 2, i.e. it has to set an interrupt cell in one of the system controllers of which processor 2 is the control processor. In which system controller the interrupt cell will be set depends on through which port processor 2 expects the interrupt (see item 27).

Interlace control (interlace). This item describes the actual interlace switch settings (see "bit pattern" in this document).

Base addresses of the system controllers. Together with item 14 (the size of the system controllers) the address range of each system controller is determined.

Bit Pattern

Port assignment:

port (x).ind is the index into the Major Module Configuration Table

port (x).id is a 5 bit description of the device through port x.

"00000"	port disabled i.e. nothing connected through this port belonging to the system (although there might be some cables).
"00001"	System Controller
"00010"	Prototype Clock
"10001"	Processor
"10010"	GIOC
"10100"	EMM

Interlace Control:

There are six bits that gives all information about interlace. The names s1234 etc refer to declarations (see below). If the bit s1234 is set, the system controllers "A", "B", "C", "D" are in 4-way interlace. If this bit is not set, there might be system controllers in 2-way interlace. In order to find the information, the bits s12 and a34 are checked. If s12 is set, system controllers "A" and "B" are in 2-way interlace; if it isn't set, there is no interlace with these controllers. Bit s34 is treated similarly as s12. The interlace control for system controllers "E", "F", "G", "H" is handled the same way as above.

```
/*          major module configuration table                    */
                                                                 /*  10.22.67   */

dcl 1       mmct$mmct ext ,

      2     sys_name char (16) ,          /* system identification          */
      2     sys_date bit (72) ,           /* date of system tape issue      */
      2     start_date bit (72) ,         /* date and time of system loading */
      2     conf_id   char (16) ,         /* configuration identification */
      2     supv_id   char (16) ,         /* hardc superv identification  */
      2     nsys_contrs fixed ,           /* number of system controllers */
      2     nclocks fixed ,               /* number of clocks              */
      2     nprocessors fixed ,           /* number of processors          */
      2     ngiocs fixed ,                /* number of giocs               */
      2     ndrums fixed ,                /* number of drums               */
      2     i_sys_clock fixed bin (3) ,   /* index of system clock         */
      2     i_bl_cpu  fixed bin (3) ,     /* index of bootload CPU         */
      2     i_bl_gioc fixed bin (3) ,     /* index of bootload GIOC        */

    1       mmct$sys_contr (8) ext ,
      2     size fixed bin (35) ,         /* storage capacity              */
      2     port (0:7) ,                  /* port assignment               */
        3   id bit (5) ,                  /* module identification         */
        3   ind fixed bin (4) ,           /* mmct index of module          */
      2     contr_proc_port fixed bin (4) ,
      2     name char (32) ,              /* installation name             */
      2     id bit (18) ,                 /* sys contr identification      */
      2     ex_sw bit (1) ,               /* switch on if memory exists    */

    1       mmct$clock (3) ext ,
      2     name char (32) ,              /* installation name             */
      2     id bit (18) ,                 /* clock identification          */
      2     int_cell ,                    /* interrupt cell assignment     */
        3   program fixed bin (6) ,       /*                               */
        3   trouble fixed bin (6) ,       /*                               */
      2     sys_contr fixed bin (4) ,     /* sys contr residence           */
      2     sys_contrx fixed bin (4) ,    /* real residence (prot.clock)   */

    1       mmct$processor (7) ext ,
      2     base_ptr ptr ,                /* base of fault vector          */
      2     port (0:7) ,                  /* port assignment               */
        3   id bit (5) ,                  /* module identification         */
        3   ind fixed bin (4) ,           /* mmct index of module          */
      2     name char (32) ,              /* installation name             */
      2     id bit (18) ,                 /* proc identification           */
      2     tag bit (3) ,                 /* processor tag                 */
      2     int_port fixed bin (4) ,      /* port for process interrupts   */
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```
1       mmct$gioc (4) ext ,
  2       base_ptr ptr ,              /* base of mailboxes              */
  2       port (0:7) ,                /* port assignment                */
    3       id bit (5) ,              /* module identification          */
    3       ind fixed bin (4) ,       /* mmct index of module           */
  2       int_cell ,                  /* interrupt cell assignment      */
    3       sc0 fixed bin (6) ,       /* status channel 0               */
    3       sc1 fixed bin (6) ,       /* status channel 1               */
    3       sc2 fixed bin (6) ,       /* status channel 2               */
    3       sc3 fixed bin (6) ,       /* status channel 3               */
  2       largest_channel fixed ,     /* largest assigned ch            */
  2       name char (32) ,            /* installation name              */
  2       id bit (18) ,               /* gioc identification            */

1       mmct$drum (4) ext ,
  2       base_ptr ptr ,              /* base of mailboxes              */
  2       port (0:7) ,                /* port assignment                */
    3       id bit (5) ,              /* module identification          */
    3       ind fixed bin (4) ,       /* mmct index of module           */
  2       int_cell ,                  /* interrupt cell assignment      */
    3       program fixed bin (6) ,   /*                                */
    3       data    fixed bin (6) ,   /*                                */
    3       trouble fixed bin (6) ,   /*                                */
  2       name char (32) ,            /* installation name              */
  2       id bit (18) ,               /* drum identification            */

1       mmct$proc_int_cell ext ,      /* interrupt cell assignment      */
  2       initialize fixed bin (6) ,  /* for interrupts set by a        */
  2       pre_empt   fixed bin (6) ,  /* processor                      */
  2       time_out   fixed bin (6) ,  /*                                */
  2       quit       fixed bin (6) ,  /*                                */
  2       sys_trouble fixed bin (6) , /*                                */

/*  the following items describe switch settings which must be the      */
/*                  same on all active modules                          */

1       mmct$interlace ext ,          /* interlace control              */
  2       sabcd bit (1) ,             /* 4_way                          */
  2       sab   bit (1) ,             /* 2_way                          */
  2       scd   bit (1) ,             /* 2_way                          */
  2       sefgh bit (1) ,             /* 4_way                          */
  2       sef   bit (1) ,             /* 2_way                          */
  2       sgh   bit (1) ,             /* 2_way                          */

1       mmct$base_addr (8) fixed bin (24) ext ;
                                      /* lowest addr in each sys_cont */
```