DRAFT

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ASYNCHRONOUS BIT SERIAL INTERFACE -- FUNCTIONAL SPECIFICATION

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1. General Description

For some time it has been clear that a replacement for the former Multics interface (the FIMPSPIF) to the ARPA Network IMP (Interface Message Processor) would be necessary for use with the 6180 system.

The principal reason for this was the necessity of using a "Distant Host Interface" arrangement since the IMP is to remain at 545 Technology Square whereas Multics resides in building 39. In addition, it was deemed necessary that the new interface run in a full duplex mode, thereby allowing simultaneous read and write operations.

I have designed and built such an interface, the Asynchronous Bit Serial Interface (ABSI). Like the GIMPSPIF, the new interface communicates with Multics via a Common Peripheral Interface (CPI) as defined in Honeywell document number 43A130524 (revision H1), and to the IMP as defined in Bolt, Beranek and Newman report 1822. Unlike the SIMPSPIF, two CPI type channels are needed to allow full duplex operation. One is used for write operations (HOST to IMP) and the other for read operations (IMP to HOST). The new interface uses the "two way handshake" procedure (see BBN-1822) for communicating with the IMP. The timing has been made slow enough to meet distant host interface requirements but it is capable of running with either a local or distant interface. This allows a theoretical maximum transfer rate of about 800,000 bits/sec. in each direction. The ABSI attempts to meet as closely as possible the CPI specifications. All known exceptions are summarized in section 6 below. It is expected that the interface will operate with any Honeywell 6000 series IOM Common Peripheral Channels. It probably will not work with a DataNet 355, 600 IOC, or 645 GIOC channel.

The following description assumes that the reader is familiar with BBN-1822 and the Common Peripheral Interface specifications and operation. No attempt is made to suplicate the information contained there.

2. Operation

The new interface accepts the following commands:

OPCODE (octal)	MEANING
00	REQUEST STATUS
01	READ (start input from IMP)
11	WRITE (start output to IMP)
20	HOST DOWN
40	RESET STATUS
60	HOST UP

The device code sent as part of the command sequence is ignored although its parity is checked.

2.1 Request Status (00)

This command will return the same status as the previous command on the same channel. Previous COMMAND REJECT status, however, will be ignored so that if COMMAND REJECT status is received in reply to REQUEST STATUS, it indicates that there was an error in the transmission of the REQUEST STATUS command itself. Note that the status stored may indicate the substatus IMP DOWN even if the IMP has since come up. To correctly obtain the current IMP up/down status, RESET STATUS (see section 2.5) should be used. (A similar condition exists for the substatus HOST DOWN.) Note also that the status returned by this command may be garbage if it is the first command given after initialization of the ABSI (see section 3 below).

2.2 Read (01 on the read channel only)

This command will start reading a message from the IMP. It will terminate under any of the following conditions:

1. The LAST IMP BIT line is received along with a data bit.
2. The host up/down relay is changed to the down state by either of the following:
   a) the manual HOST DOWN pushbutton on the interface
   b) the HOST DOWN command on the write channel
3. The IMP goes down (according to its up/down relay).

4. The channel decided to terminate the command.
   Note that terminate will not actually happen until just after a complete character (6 bits) has been transmitted to the channel. Possible causes are:
   a) The storage buffer indicated in the DATA DCW has been filled and there are no additional DATA DCW's.
   b) The channel is "masked" by the software (see the IOM specifications).
   c) Some other condition occurs which causes masking, such as a second "connect" to the channel before the first list has completed.
5. An "initialize" signal is received (see section 3 below).
   Note that all transmissions are aborted immediately and no status is stored. When the "initialize" level is removed, the channel will be ready to accept a new command no matter what its previous state was. The "initialize" condition also forces the host up/down relay to open (i.e., HOST DOWN).

In normal operation, only cases 1 (COMPLETE MESSAGE, no errors) and 4a (INCOMPLETE MESSAGE, no errors) should occur. If the latter occurs, the termination status will be READY with substatus INCOMPLETE MESSAGE. The message may be reconstructed by appending the data read by the next READ command to the end of the current data. Unlike the GIMPSPIF, the READY FOR NEXT IMP BIT line is not raised until a read command is issued. Thus there is no way to determine that the IMP has a message waiting until a READ command is issued. It is expected that the software will normally keep a READ command pending whenever the system is in operation. The expected method for aborting such a read command is to issue a HOST DOWN command on the write channel. If this fails, the HOST DOWN pushbutton on the ABSI should be used. If this also fails, the initialize bushbutton on the ABSI should be tried.

2.3 Write (11 on the write channel only)

This command starts writing a message to the IMP. Normally termination will occur only on end of message condition in the buffer. Note, however, that any of the conditions listed in section 2.2 above for aborting the READ command also apply (except obviously 1 and 2b). The LAST HOST BIT level will

be sent with the last bit transmitted only if termination is caused by the channel rather than the ABSI. Also note that termination under conditions 4b and 4c (the channel becoming masked) will take place only after the next character (6 bits) has been sent to the IMP.

2.4 Host Down (20 on the write channel only)

This command will open the relay closed by the HOST UP command. If a READ or WRITE operation is taking place on the other channel, it will be aborted when that channel sees the relay open. It is possible the HOST DOWN command will not take effect if followed too closely by a HOST UP command (i.e., the relay doesn't get a chance to open). Whenever the relay is open (or opening), READ and WRITE commands will be rejected with the status COMMAND REJECT and the substatus HOST DOWN. The HOST DOWN command may be simulated at any time by the manual HOST DOWN pushbutton.

2.5 Reset Status (40)

This command is identical to REQUEST STATUS, except that any resettable status condition from the previous command will be reset. Note that a RESET STATUS command is effectively executed before any command (other than REQUEST STATUS). Resettable status is defined as:

1. any DATA ALERT condition
2. INCOMPLETE MESSAGE substatus
3. IMP DOWN substatus if the IMP is no longer down
4. HOST DOWN substatus if a HOST UP command has subsequently been given.

2.6 Host Up (60 on the write channel only)

This command causes the HOST MASTER READY line to be connected to the HOST READY TEST line by closing a relay. The software must make sure that no READ or WRITE command is issued to either channel until the relay has had a chance to settle. The delay time is not specified here, because relay characteristics may vary. The current relay takes about 500 μsec, but the programmer should probably allow 100 msec. to be safe. This command may be simulated at any time by pushing the manual HOST UP button.

3. Initialization

Initialization of the ABSI resets it to a state in which it is ready to receive a command from both channels. Any operations in progress will be aborted without returning status. An "initialize" signal can be generated by any of the following:

1. Either IOM channel opens its relay ("POX" line) which is used by the peripheral to check that the IOM channel is connected and has power applied. Note that this relay is opened by the "SYSTEM INITIALIZE" button on the IOM or the bootload console. The same effect is obtained if one of the cables is disconnected*. (Note that if either side of the ABSI is set to the "offline" position, all signals from the corresponding channel will be ignored.)
2. The manual "initialize" button is pushed.

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* Note that if the IOM ABSI cables are routed through in "Peripheral Switch" one may use these switches to initialize the ABSI. If this is done, the switches for both the read and the write sides should be "cycled" to make sure that both IOM channels are also reset.

4. Special Interrupts

When the IMP comes up (closes its IMP READY relay) a "special interrupt" will be sent on the READ channel. Note that any bounce in the relay contacts may cause several interrupts to be sent to the software; they should be ignored. It is suggested that the software delay at least 100 msec. after receiving the first interrupt to allow the relay to settle. During this time the extra interrupt should be ignored. A somewhat safer alternative would be to restart the 100 msec. timer on each interrupt and not consider the IMP up until this delay has passed without any further interrupts.

5. Status

The following status codes have been defined for the ABSI:

Major Status	Substatus	Meaning
0000		Ready
	xxl xxx	IMP Down
	xlx xxx	HOST Down
	lxx xxx	Incomplete Message
0011		Data Alert
	xxx lxx	Parity Error
	xxl xxx	IMP Down
	xlx xxx	HOST Down
	lxx xxx	Incomplete Message
0101		Command Reject
	xxx xxl	Invalid Operation Code
	xxx lxx	Parity Error in Command Sequence
	xxl xxx	IMP Down
	xlx xxx	HOST Down
	lxx xxx	Incomplete Message
1000		Channel/Peripheral Subsystem Busy

Any substatus condition may occur simultaneously with any of the other substatus conditions under the same major status. If this occurs, the appropriate substatus codes will be merged to form the substatus returned.

5.1 Ready Status

The READY status indicates that the channel is ready to accept a command and that no (unreset) errors occurred in the previous command to the channel.

5.1.1 IMP Down Substatus (READY)

The IMP DOWN substatus indicates that the IMP READY relay is open (i.e., the IMP READY TEST line is not connected to the IMP MASTER READY line.) Note, however, that once this bit comes on (i.e., the IMP goes down) it stays on until it is reset by a command other than REQUEST STATUS (e.g., RESET STATUS). Note that this relay, like the host up/down relay, is subject to bounce and so it would be a good idea to wait for the relay to settle before rechecking the status. One could also wait for the special interrupt which says the IMP is up (see section 4 above), but this may be unreliable if one does not

carefully consider race conditions. (The software may receive the special interrupt before the IMP down status). A "timeout" on waiting for the interrupt would therefore be suggested.

5.1.2 Host Down Substatus (READY)

The HOST DOWN substatus indicates in a similar manner that host up/down relay has been, is, or is becoming open.

5.1.3 Incomplete Message Substatus (READY)

The INCOMPLETE MESSAGE substatus may occur only on the READ channel. It indicates that termination occurred before the LAST IMP BIT level was received. Since no bits are lost when this occurs, the entire message may be reconstructed by appending the data read by the next READ command to that read by the most recent READ command.

5.2 Data Alert Status

This status is stored if an error has occurred during the transfer of data in the appropriate direction. Any error will cause the channel to abort the current operation immediately.

5.2.1 Parity Error Substatus (DATA ALERT)

Note that the READ channel will indicate a parity error in the channel status rather than the peripheral status field since this error is detected by the channel rather than the ABSI. Therefore PARITY ERROR substatus can occur only on the WRITE channel. It indicates that a character has been received from the IOM channel with bad parity. The WRITE command is aborted and the LAST HOST BIT level is not sent to the IMP. Thus the software could indicate to the IMP that this message should be ignored by flashing the HOST UP line (waiting appropriate times for relay opening/closure) and then exchanging a reset sequence with the IMP. (Note that this error recovery procedure will also abort any pending read operations when the HOST DOWN command is executed. Since all communications may be aborted, this is not a recommended method of error recovery.)

A much less drastic way to cause the IMP to discard the message in error would be to immediately WRITE a second message whose length is greater than the maximum legal message length (256 words, for instance, is greater than the current maximum length of 8096 bits). Since the previous WRITE did not

send a LAST HOST BIT level, this second message will be appended to the first, causing the IMP to discard it. The original message may then be rewritten as if nothing had happened (assuming no further PARITY ERROR's occur).

It should be noted that the PARITY ERROR substatus usually will be returned only if a logic gate fails and so it may actually be reasonable to consider such an error fatal.

5.2.2 IMP Down Substatus (DATA ALERT)

IMP DOWN substatus indicates that the IMP went down at some time during the Read/Write operation. Data may have been lost.

5.2.3 Host Down Substatus (DATA ALERT)

HOST DOWN substatus indicates that the host up/down relay become open (e.g., the HOST DOWN pushbutton was pushed) during the Read/Write operation. Data may have been lost.

5.2.4 Incomplete Message Substatus (DATA ALERT)

INCOMPLETE MESSAGE substatus is solely an indication that the LAST IMP BIT level was not received before the operation terminated. (It occurs on the READ channel only). This information is actually of little use since data may have been lost due to the error which caused the DATA ALERT status. INCOMPLETE MESSAGE substatus will usually occur in conjunction with either HOST DOWN or IMP DOWN when the major status is DATA ALERT.

5.3 Command Reject Status

COMMAND REJECT status indicates that the command could not be accepted for the reason indicated by the substatus.

5.3.1 Invalid Operation Code Substatus (COMMAND REJECT)

INVALID OPERATION CODE substatus indicates that the command code received by the ABSI was not one of the legal command for that channel.

5.3.2 Parity Error in Command Sequence Substatus (COMMAND REJECT)

PARITY ERROR IN COMMAND SEQUENCE indicates that either the device code (which is otherwise ignored) or the command code received by the ABSI had bad parity. The command is not executed even if the command code would otherwise be legal.

5.3.3 IMP Down Substatus (COMMAND REJECT)

For all operations except READ and WRITE, this substatus can occur only in conjunction with one of the above two command transmission errors. In this case this status is described in section 5.1.1 above.

For READ and WRITE operations, this substatus (without invalid operation code or parity error in command sequence substatus) indicates that the command could not be initiated because the IMP READY relay is open.

5.3.4 Host Down Substatus (COMMAND REJECT)

This substatus is analogous to IMP DOWN substatus in section 5.3.3 above.

5.3.5 Incomplete Message (COMMAND REJECT)

This substatus can only occur in conjunction with one of the two command transmission errors described in section 5.3.1 and 5.3.2 above. It is otherwise analogous to the substatus of the same name, described in section 5.2.4 above (and is likewise nearly useless). Note that in this case it refers to the previous READ/WRITE operation, not the rejected one.

5.4 Channel/Peripheral Subsystem Busy

This sattus indicates that a READ/WRITE command was properly received and is currently being executed.

6. Exceptions and Assumptions

This section describes all the known assumptions concerning the interfaces with the CPI type channels and with the IMP. Also noted are any exceptions to the specifications.

6.1 Restriction on EDT Transmission on the Write Channel

The WRITE channel must know when it is writing the last bit to the IMP so that it can assert the LAST HOST BIT level. In order to avoid extra buffering and a large increase in complexity, it is necessary that the EDT strobe arrive no more than 4 μsec. after the WRITE CLOCK TO PERIPHERAL strobe. This is despite the section on Write Command Termination (section 4.3.3, sheet 32) of 43A130524. Honeywell document 43A177715 (the IOM specifications) section As.3.4.3 states, however, that the IOM CPC sends the EDT .5 μsec. after the WRITE CLOCK TO PERIPHERAL. Since the ABSI is intended for use only with the 6000 IOM, no problems are foreseen.

6.2 Restriction on EDT Transmission on the Read Channel

The READ channel must know whether the most recent character sent to the channel is to be the last character before it can read the next character from the IMP (because we have decided to eliminate read-ahead which is both an unjustifiable complexity and undesirable with regard to network protocols). As defined in 43A130524 the EDT strobe may arrive at an arbitrary time after the READ CLOCK TO PERIPHERAL strobe. Clearly, the ABSI must make some restriction on how long it will wait before reading the next character. The ABSI therefore delays 1 μsec.

The current IOM Common Peripheral Channel violates the standard in 43A130524. It sends the EDT instead of the last READ CLOCK TO PERIPHERAL, rather than after it. (43A177715, section As.3.4). The ABSI will work equally well with this convention. In fact, the current method of indicating termination seems to make more sense.

6.3 Lack of Transfer Timing Error Detection

In spite of section 6.2 (sheet 52) of 43A130524, no provision is made for detecting TRANSFER TIMING ERRORs. This is because the asynchronous nature of the ABSI makes such detection unnecessary; its inclusion would only add nearly useless (and possibly detrimental) logic to the interface.

6.4 Minimum Initialization Time

It is assumed that if an "initialize" signal is given to the ABSI (i.e., the Peripheral Reset Line is opened) it will stay asserted for at least 50 μsec. If this does not happen, the ABSI may not reset completely. In practice the IOM asserts this signal for much longer times than this and so no problem is expected. Similarly it is assumed that the RESET pushbutton will be held down for at least this amount of time. (Note, that it would be very difficult to hold it down manually for a shorter period, so this is not really a problem).

6.5 Initial Power-on and Initial On-line Status

Section 6.3 of 43A130524 does not specify what the initial status should be. It is therefore assumed that garbage may be returned until a command other than Request Status is sent.

6.6 Minimum Buffering Requirements

Section 6.5 of 43A130524 specifies a minimum buffering capability of two characters for the WRITE channel. Only one is provided. Since the ABSI is asynchronous, no problem except a very slight speed loss should be encountered.

6.7 Definition of Data Transmission Time

In many places 43A130524 specifies times as "sufficient time ... to set ... receivers". It is assumed that 0.75 μsec. is more than sufficient to cover all skew, cable length, and settling time considerations.

6.8 Skew in the IMP Connection

The IMP currently delays 500 ns. (see 1822 section 4.5) to avoid errors due to skew in the IMP connection. The ABSI makes no further (intentional) provision for such skew. If problems due to this are detected, it is expected that the delay times in the IMP can be increased to compensate for this.

6.9 Voltage Levels for the Distant Interfaces

BBN-1822 specifies ±0.5 volt signals for the distant interface connections; the drivers used are closer to ±0.75 volt. BBN indicates that this should cause no problem (and, in fact, is probably better).

6.10 Maximum Pulse Width

43A130524 section 1.1 (sheet 5) states that no maximum width is specified for the pulses used in the common peripheral interface. The ABSI requires that the WRITE CLOCK TO PERIPHERAL pulses have a maximum width of 120ns. for the write side and 180ns. for the read side. The 6000 IOM sends 50ns. pulses so no problem should be encountered. It is expected that this restriction will be removed in production versions of the ABSI.

6.11 Maintenance Requirements

Section 6.6 of 43A130524 is not met in that neither a Running Hour Clock nor full off-line test facilities have been provided. A Running Hour Clock is considered unnecessary because the ABSI does not have its own power supply. A minimal maintenance panel has been provided for the prototype. Connections for further off-line test facilities have been provided in the ABSI but are not currently used.

6.12 Initialization

When the ABSI is manually initialized (via the "initialize" pushbutton) it will also open the "CP CHN POX" lines to both channels. This will cause each channel to reset, and act as if the ABSI had been disconnected. (This condition lasts only as long as the "initialize" signal is present.) This behavior seems like the only reasonable way to inform the software and the channels that the ABSI has been manually initialized. Although the feature is allowed by 43A130524, it is not believed to be present in any other peripheral and so it has been included in this section on exceptions.

7. Physical Characteristics

The ABSI is implemented on a single 12" x 12" Honeywell MQX type circuit board. Communication with the two CPI channels is through the two free-edge connectors (one channel on each connector). Communication with the IMP is through the backpanel, using slip over connectors on the backpanel wire-wrap pins. It is required that -5v. be provided to the board through the backpanel, in addition to the +5v. and ground normally provided. -5v. is not normally connected to the backpanel although it is available in the power supply. A standard wire exists for making the connection. It is expected that the ABSI will work in any slot providing such power and packpanel connections. In particular, it may be mounted in either a 6000 IOM or a DataNet 355 payload slot.

The logic used is Honeywell 500 series (similar to Sylvania SUHL II) with the exception of the distant interface drivers and receivers which are 400 series logic and are similar to the TI SN75107-110 group of integrated circuits.* Although 400 series logic is deemed generally preferable to 500 series logic, the difference is not critical for this application. The decision to use the latter was made on the basis of the availability of an MQX prototype board, which has +5v. (Vcc) and ground prewired to pins 4 and 10 of the chip positions (thereby matching 500 series chips).

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* Due to poor common mode rejection in the 407 (SN75107) receiver, one dual receiver in the prototype has been replaced by a National DM8820A dual receiver which has common mode noise rejection characteristics.

8. Nomenclature

The official name for the interface is Asynchronous Bit Serial Interface. The official Asronum for the ABSI is appropriately enough, ABSO. The official nickname is Fred. Use of any other nickname (e.g., Gumpertz Gizmo, that G-d D--n thing, etc.) is allowed, but does not conform to any ANSI, EIA, ASTM, RETMA, CCITT, FCC, FAA, FDA, or NBS standards. It may also not conform to students of good taste.