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MASSACHUSETTS INSTITUTE OF TECHNOLOGY *CAMBRIDGE, MASS. 02139*

from the office of The Director, Information Processing Center

TO: R. C. Daley
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J. R. Steinberg

FROM: W. J. Burner

DATE: February 5, 1974

SUBJECT: 6180 PERFORMANCE

Attached is a copy of Bob Hoffman's reply to my letter of last October for your information.

As you can see, they missed the whole point. They addressed each of the specifics of my complaint, but refused to address the problem of why, even now six months after turnover, 2 processors, 384K memory and 2 million words of bulk store still support only 70 users.

We are continuing to force the issue.

/jm (Enc.)

Honeywell

1 February 1974

Mr. Weston J. Burner, Director
Information Processing Center
Massachusetts Institute of Technology
60 Vassar Street, Building 39
Cambridge, Massachusetts 02139

Dear Wes:

As you know, we have been trying for some time to collect data from our engineering group to support a response to your requests for "formal" explanations of (a) why 6180 Multics has not shown more of a price-performance improvement over 645 Multics, and (b) the reasons for certain engineering changes which you assert have been "made under the guise of reliability without concern for the overall system performance". Recent Phoenix reorganizations, with the consequent changes in people and responsibilities, have all resulted in an extra-long turnaround time in answering your requests for which we are sincerely apologetic.

You have identified your principal areas of concern to be Bulk Store Controller, Associative Memory, Processor Speed, and Disk Storage.

Bulk Store Controller (BSC)

Engineering has stated that they are essentially in agreement with the measured wait times you have stated, with one qualification. The production model BSC (the "new controller") does have an average wait time of 0.425 ms per 1024-word page versus 0.398 ms for the engineering model BSC (the "old controller"). This 27-microsecond increase was caused by the addition of synchronization logic between the BSC and the Bulk Store Units (BSU). This added logic requires an extra clock cycle (100 nanoseconds) for each four-word transfer from the BSU.

$$(1{,}024 \text{ words}) \times \frac{100 \text{ nanoseconds}}{4 \text{ words}} = 25.6 \text{ microseconds}$$

After the arrival of the new BSC at MIT, a change has been installed to minimize the adverse effects of adding the synchronization logic--this change (FCO #PHAMA013) removed one clock cycle from each read error correction cycle. Because of the timing of the data transfer to the system controller unit, however, only every other read cycle was affected. Thus, the net savings was 12.5 microseconds per page. Additional ways to reduce wait times are being investigated.

The initial change in the design-spec wait times (from 0.256 ms to 0.384 ms) was necessitated by a change in store unit technology (from bi-polar shift register to high-density core). This technology change was forced upon Honeywell when the bi-polar BSU vendor decided to discontinue production. The proposal description of the Bulk Store Subsystem was rewritten by Design Engineering and submitted to Henry Nye of DSO/SDC who presumably transmitted the revised information to MIT at the time of the change.

Associative Memory and Processor Speed

During April of 1973, MIT personnel made some measurements which compared MIT's 6180 Multics with MIT's 645 Multics; these results were reported in Professor Jerry Saltzer's draft dated 4 May 1973. Since that time, our 6180 Hardware Engineering group has spent considerable effort in a clean-up and redesign of the 6180 appending unit hardware (including associative memory) to improve processor hardware performance. The following table is a comparison of MIT measurements with those made in Phoenix on a 6180 and on the "I6180" improved (but not yet released) processor:

	645 MIT	6180 MIT	6180 PHX	I6180 PHX	Ratio 6180/645	Ratio I6180/645
ADA	1920	832	766	669	2.66	2.88
STA	2250	1140	1043	973	2.25	2.30
EPPn	2970	1505	1490	1005	2.0	2.82
SPRPnn	2870	2230	2250	1200	1.27	2.32
LPRPnn	---	---	2000	1910	---	---
LARn	---	1990	1930	1800	---	---
SARn	---	2230	2150	1200	---	---

The small variations between 6180-MIT and 6180-PHX can be attributed to differences in cable lengths and possibly to other factors (such as whether the store units were interlaced, etc.). All of the Phoenix measurements were made on a system with 10-foot cables, interlaced store units, and a paged running environment. You should note that in the "unimproved" 6180, the appending unit cycle time was longer for a paged cycle than for an unpaged cycle; on the other hand, the cycle times are the same for the "improved" version of the 6180.

There are several additional items (not discussed in Professor Saltzer's report) which will have an effect on system performance: the use of bit 29 adds 150 nanoseconds to the control unit address preparation path; Character-to-Bit conversion will add 100 nanoseconds to the execution time for many of the appending unit load and store instructions; and the various impacts of EIS (f3 in the Saltzer Report) have not yet been quantified but should be quite significant.

Disk Storage

As you know, the reformatting of the DSS190 disk subsystem to "DSS191" is now scheduled to occur over the coming weekend. We certainly agree with you that this enhancement has been long in coming, but I must state with a clear conscience that Honeywell Marketing has made absolutely no "promises" or "guarantees" as you have suggested in your letter. Engineering has steadfastly declined to commit to any availability date for this enhancement which is prior to the product calendar schedule, and Marketing has followed suit by making no commitments to you on this matter. Because of the close working relationships between MIT and CISL personnel, you are well aware of the existence and the real status of all of our planned enchancements; since the 6180 at MIT is utilized for Multics software development, it will be the first system to have a pre-release version of the DSS191 capability.

You also know that the DCH190 dual-channel capability is now scheduled for installation next week. You will recall that this hardware feature was part of the original configuration on which MIT's anticipated performance improvements were based. Subsequently, the DCH190 was deleted from the original configuration in an MIT economy move, but the expectations of system performance were not revised to reflect only a single disk channel.

We hope you agree, Wes, that this letter is responsive to your requests for comments in the various areas of stated concern. Bob Chevalier and I would like to have a meeting with you to discuss these (and any other) performance issues after you've had a chance to review these comments with your colleagues in IPS and MAC.

Cordially,

R. E. Hoffman
Branch Manager
Northeast Branch

REH/kmp