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"The Effect of Reordering of Instructions upon Execution Time"

In order to examine the effect of reordering of instructions included in the instruction sequence which was used in measuring the degree of memory cycle interference (See MPL-54), the randomized version of the sequence, mipt_ty*, obtained by shuffling and reordering the first nine instructions of mipt_ty* was executed and measured on both a single processor system and a two processor system. The original sequence, mipt_ty*, and the particular randomized sequence

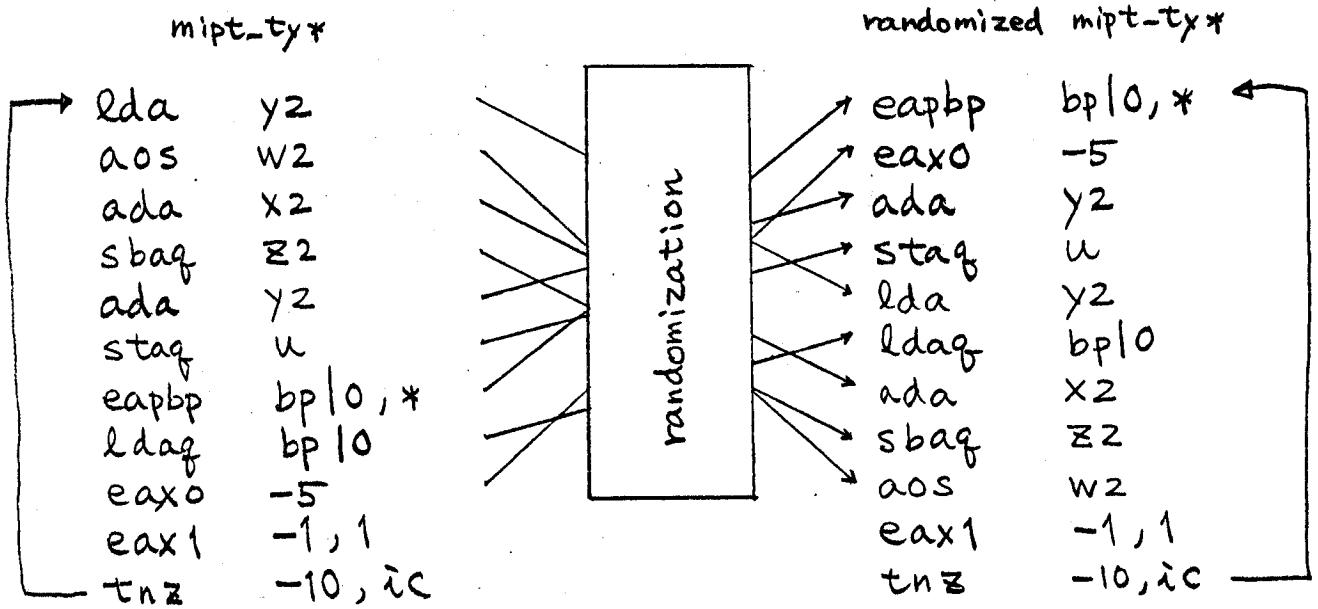

Figure 1 Generation of the Randomized Instruction Sequence

used in the experiment are shown in Figure 1. The one processor experiment was undertaken when the system was heavily loaded. As for the two processor experiment, only the first kind of experiment (See MPL-54), i.e., the one which runs the sequence to be measured against other normal Multics users was carried out when the full configuration system was heavily loaded.

Each experiment was exercised by running the randomized mipt_ty* in exactly the same way as that reported in MPL-54. The measured execution times and instruction execution rates are summarized in Table 1. It is clearly seen that the execution time of the sequence depends on the ordering of constituent instructions. The explanation for this is that the degree of overlapped execution of instructions on an asynchronous processor can significantly depend on the order in which instructions are executed by it. In our case, the randomized mipt_ty* ran at the 5.3 (= .374/.355) % increased speed on the single

Table 1 The Measured Execution Times and Rates

instruction sequence		1 CPU	[sample size]	2 CPUs against normal users (3 core boxes)	[sample size]	(percent increase in time)
original						
mipt_ty*	ave.	31559 μsec		33827 μsec		(+7.2 %)
	min.	-427 μsec		-2067 μsec		
	max.	+416 μsec		+6923 μsec		
ave.	rate	.355 mips	[10]	.331 mips	[20]	
randomized						
mipt-ty*	ave.	29914		31878		(+6.6 %)
	min.	-441		-2221		
	max.	+435		+2254		
ave.	rate	.374	[20]	.351	[20]	

* mips = million Honeywell 645 instructions per second

** The minimum (maximum) execution time observed in each experiment is represented as a deviation from its average.

processor system and at the 6.0 (= .351/.331) % increased speed on the two processor system. It is also observed that the execution time of the randomized mipt_ty* was lengthened by 6.6 % on the full configuration system, because of memory cycle interference.