

September 27, 1965

SUBJECT: Peripheral T&D Interface With 645 Software Monitor

SUMMARY

This is a first attempt at defining an interface between the 645 Peripheral T&D Programs and the 645 Software Monitor System. The approach which I believe to be the most feasible is described in this document.

The philosophy of the approach described is to include the subset of the Peripheral T&D Control Program, required for on-line testing, into the 645 Software Monitor Program as it is being written.

This description was written with the "worst case" in mind, when a GIOC and an IOC are both included in the system. The reader should disregard all mention of the IOC if it is not to be considered in the Software Monitor Program.

This approach was chosen for the following reasons:

1. Allows more thorough testing - We will be able to perform all testing that our present Peripheral Tests perform.
2. Less manpower - It will be cheaper for the Computer Department to include the features in the Software Monitor to interface with the T&D Programs than it will be to rewrite all of the T&D Programs. The features needed in the Software Monitor Program is less than 4K of code. It should be mentioned also that the original writer of the T&D Control Program, Paul Jennings, is now working in the 625/635 Software Subsection.

I shall appreciate it if all comments and criticism of this document is directed to me as soon as possible.

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PERIPHERAL T&D INTERFACE WITH 645 SOFTWARE MONITOR

- I. T&D PROGRAM STORAGE - Approximately 60K of storage will be required on the DRUM, MD-32, or DSU for on-line T&D Programs. These programs will be backed up on Mag. Tape for the case where the normal storage device is not operable.
- II. T&D PROGRAM CALL - The T&D Program will be called into memory by a request from a Product Service man. This call should be made from a "spec." Maintenance Console or Communication Terminal. The Program Call should be enabled from more than one input source because of the possibility of failure of any input source.
- III. T&D PROGRAM LOAD - The Software Monitor must be able to search for the T&D Program from information contained in the T&D Program Header (first 11 words of the program). The Program Header (fig. 1) is used as a form of communication between the T&D Program and the Monitor Program controlling it. It provides the Monitor Program with Program Number, Program Name, Test Identification, Program Size, Address of Table which contains entry points, Maximum Time counts to wait for interrupts, and type codes of peripheral requirements. The monitor in turn supplies the T&D Program with counts for "Special" interrupts, channel number for required peripherals, device numbers for required peripherals, and the type code for the required peripheral. The format for the T&D Program Header is as follows:

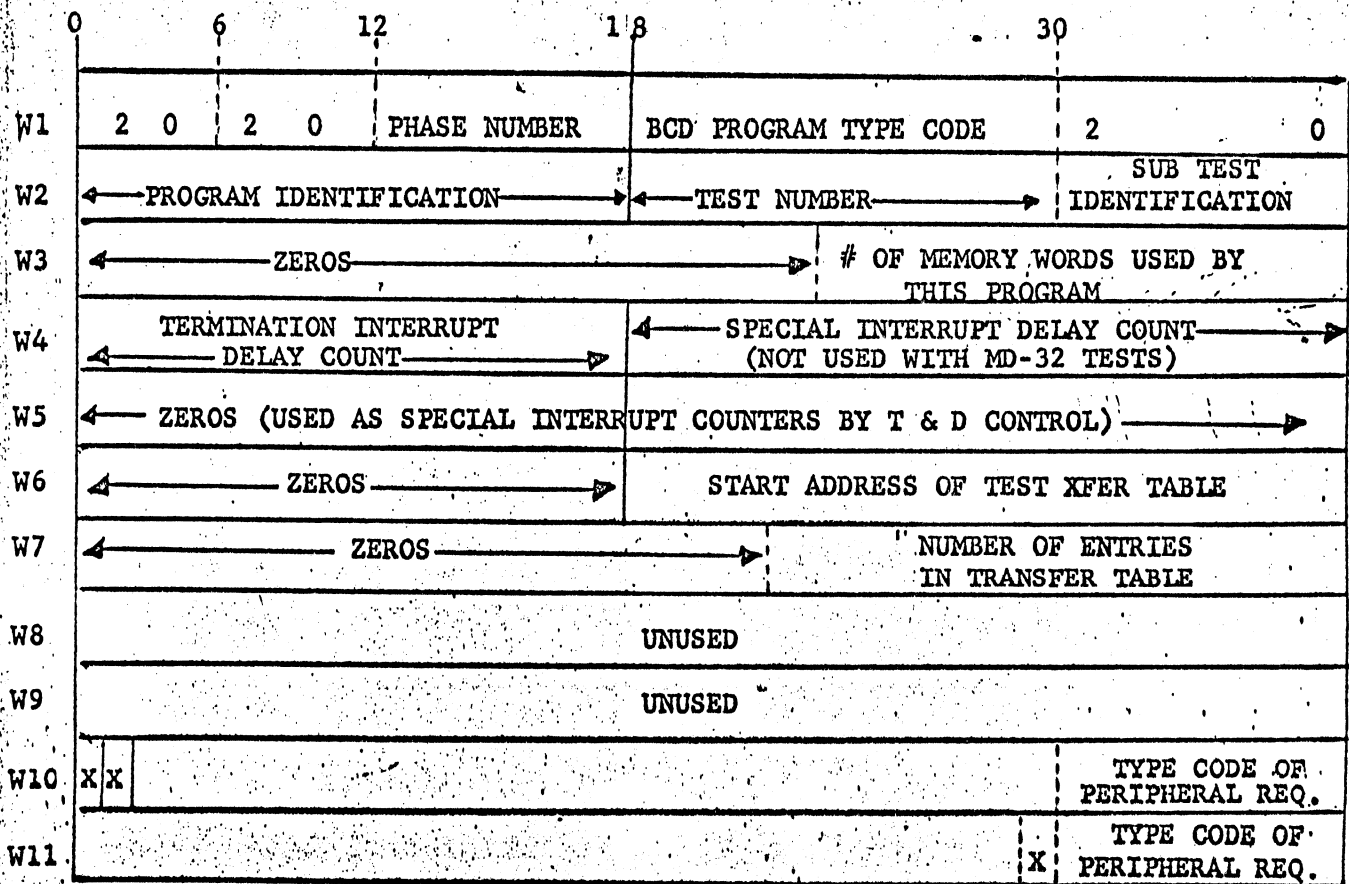


Figure 1

W1 - Contains Program Code (Bits 12-29) which is made up of the Phase Number (Bits 12-17) and the Program Type Code (Bits 18 - 29). This code is BCD to allow ease of typing. The Program Type Codes are defined as follows:

1. IOC -	01 (OCTAL)
2. GIOC -	03 (OCTAL)
3. Console -	02 (OCTAL)
4. P.T. Reader/Punch -	14 (OCTAL)
5. Card Punch -	22 (OCTAL)
6. Card Reader -	23 (OCTAL)
7. Printer -	26 (OCTAL)
8. DSU -	34 (OCTAL)
9. Mag. Tape -	60 (OCTAL)
10. Drum -	73 (OCTAL)
11. MD-32	50 (OCTAL)

The Phase Number and Program Type Codes are what the Software Monitor Program searches on when it is locating a program to be called into memory for execution.

- W2 - Contains Program Identification (Bits 0-17) consisting of 3 ALF characters, test number (Bits 18-29) which is made up of 2 BCD characters (01-99) and Subtest Identification (Bits 30-35) consisting of one ALF character (A-Z). It will be the responsibility of the Peripheral Program to update the test number and Subtest Identification each time they should be changed. This word will be typed (or printed) each time the Software Monitor Program outputs an error message.
- W3 - Contains the amount of memory used by this program in Bits 23-35. This field assumes a program will not exceed 8K.
- W4 - Contains a count (count = 1 millisecond) which will determine the length of time to allow for a termination interrupt (Bits 0-17) and a special interrupt to occur. If an interrupt does not occur within this period of time after the initiation of an I/O Command, the Software Monitor Program will assume the interrupt is not going to occur and classify the condition as an error.
- W5 - Contains two binary counters for the number of special interrupts that have occurred since the counters were cleared by the Peripheral Program. The Software Monitor Program will add one to the first counter (Bits 18-35) for each special interrupt received from the PUB assigned to the Peripheral in W10. The Software Monitor Program will add one to the second counter (Bits 0-17) for each special interrupt received from the PUB assigned to the Peripheral listed in W11. It will be the responsibility of the Diagnostic Programmer to clear these counters.
- W6 - Contains the starting address of a Test Transfer Table in Bits 18-35. The Test Transfer Table is to be supplied by the Diagnostic Programmer in his program. This table consists of transfers to the beginning of each test in his program. The purpose of this table is to enable the operator to enter any test of a given program. This implies that the Tests must be 1, 2, 3, 4 ---n. Initial entry to the program will be made by a transfer to the first entry in this table.

W7 - Bits 24-35 contain the number of entries in the Test Transfer Table whose starting address is contained in W6.

W8 - W9 - These words are saved for later expansion.

W10 - Bits 0 and 1 are used to determine whether the program was written for an IOC, GIOC, or MD-32.

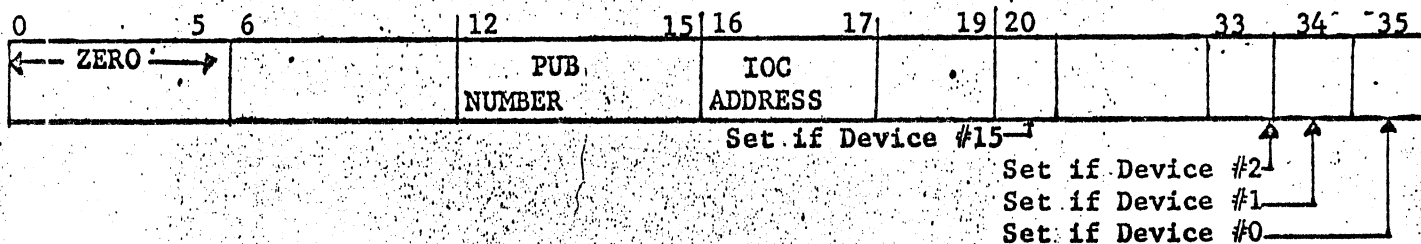
Bit 0	Bit 1	
0	0	- IOC
0	1	- MD-32
1	0	- GIOC
1	1	- Illegal

Bits 30 - 35 contain the type code of the peripheral being tested.

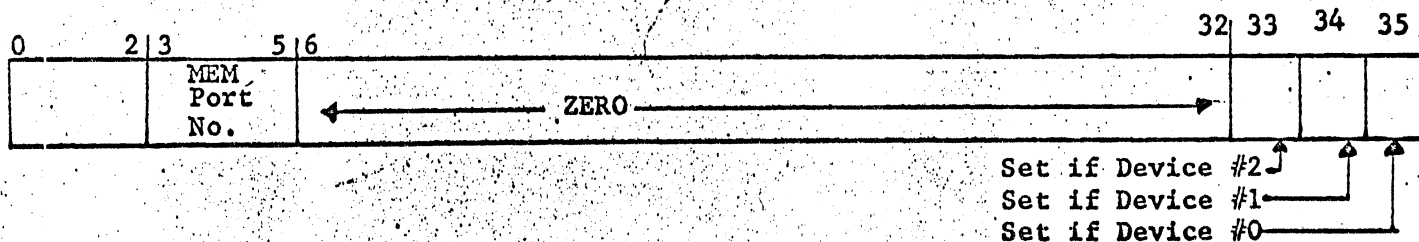
W11 - Contains the Peripheral Type Code of additional peripherals required to run this program. If this word is zero, no additional peripherals are required. If bit 29 is set, the second peripheral requirement (W11) is to be considered only if a Magnetic Tape Controller or Drum is available that is Crossbarred with the Tape Controller or Drum, respectively, required by this word. The Software Monitor Program assumes a loading device and Console or Printer so the Programmer need not list a Peripheral for standard error output routines.

NOTE: In W10 (and W11 if additional Peripheral is required) the Software Monitor Program will replace the type code with the PUB Number that the requested peripheral is connected to and the number of the devices connected to that peripheral. This replacement is made by the Software Monitor Program before it gives control to the Peripheral Program. The format of W10 and W11 after the replacement is as follows:

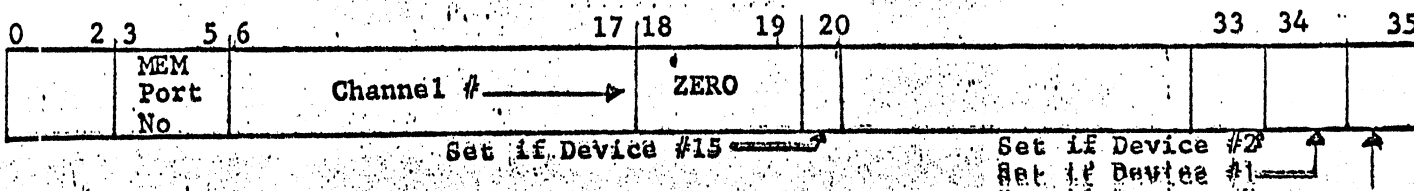
FOR IOC



FOR MD-32



FOR GIOC



III. T&D PROGRAM LOAD - (continued)

If a program has an additional peripheral requirement in W11 and such a peripheral is not available, the Software Monitor Program will output a message to the operator and will not attempt to execute the program. The exception to this case is when bit 29 is set in W11.

IV. T&D PROGRAM MASTER MODE ENTRIES - The Software Monitor must to be able to service a set of T&D Master Mode Entry routines and handle them as described below. It should be mentioned that the address fields of all MME commands need not be exactly as specified (Ex. Bit 0 set could denote T&D MME).

A. Common Peripheral Input/Output Command Initiation

Each time the writer of a Common Peripheral T&D Program wishes to issue a command to a peripheral, he must communicate with the Software Monitor Program by a Master Mode Entry with the following call sequence. The Software Monitor Program must be able to handle this call sequence when peripheral is connected to a GIØC by using the indirect DCW for IØC simulation.

0	3	6	9	12	15	18	21	24	27	30	33
← ZERO →						0 0 0 0 0 0 1	← ZERO →				
← OP-CODE →		DEVICE CODE		PUB ADDRESS	IØC ADDRESS	IØC COMMAND		0 0 0 0 0 0 0		RECORD COUNT	
← STARTING DATA ADDRESS FOR THIS DCW →						ZONE CONTROL	ACTION CODE	← NO. OF WORDS TO BE XFERRED BY THIS DCW →			
← ADDRESS OF NEXT DCW TO BE USED →						← ZERO →					
← ADDRESS OF FIRST DCW →						← ZERO →				RECORD COUNT	
Sub Ign	MAJOR STATUS EXPECTED		SUB-STATUS EXPECTED		0 0 0 0 0 0		IØC STATUS EXPECTED		0 0 0 0 0 0 0		T I S R
← ZEROS →											
← START ADDRESS OF NEXT TEST →						1 1 1 0 0 1 0 0 0		← ZERO →			
← START ADDRESS OF LOOP →						1 1 1 0 0 1 0 0 0		← ZERO →			
← NORMAL RETURN LOCATION →											

W1 - MME 10.

W2 - Primary Mailbox Word  
PUB address (Bits 12-15) is provided by programmer from information furnished by Software Monitor Program.

W3 - Secondary mailbox #1 Word.

W4 - Secondary mailbox #2 Word.  
Upper and lower address limits will be provided by Software Monitor Program.

W5 - Secondary mailbox #4 Word.  
Upon interrupt, Software Monitor Program will replace record count (Bits 30-35) with record count residual in call sequence.

W6 - Type of interrupt and status expected upon interrupt.

Bit 1 - Set if substatus is to be ignored by Software Monitor Program Error Check.

Bit 31- Set if terminate interrupt is expected.

Bit 32- Set if initiation interrupt is expected.

Bit 33- Set if special interrupt is expected.

Bit 34- Set if program wants immediate return.

If this bit is set, the Software Monitor Program must give control back to the T&D Program immediately after the connect command has been issued. This feature is used sparingly by the T&D Program and only when the program has to have control back to perform certain functions.

Bit 35- Set if program wants standard error output.

If this bit is set, the Software Monitor Program will compare the results of the interrupt against what was expected and output an error message of the following type if an error is detected.

Standard Peripheral Error Output Connected To IOC

PROGRAM AND TEST IDENTIFIER

\* MT 02 PUB-01 DEV-04 OP-46 COM-01 IOC-0  
EXPECT T READY C00 C00  
ACTUAL I REJECT 10 00

IOC MEMORY STATUS

SUBSTATUS

MAJOR STATUS

TYPE OF INTERRUPT

I = INITIATION

T = TERMINATION

S = SPECIAL



MAJOR STATUS REPRESENTATION:

00	READY
01	D BSY
02	D ATT
03	ALERT
04	EOF
05	REJCT
06	INTER
07	L TER
10	C BSY
11 - 15	ILLEGAL

If interrupt is not received in allowed time. NONE will be inserted as major status.

Standard Peripheral Error Message Connected To The GIOC

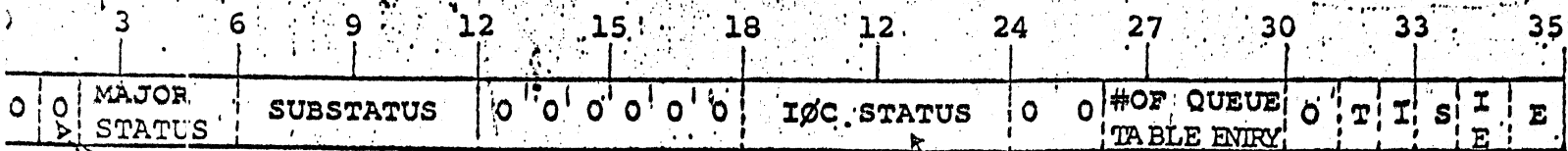
1	10	20	30	40	50
	PROGRAM AND TEST IDENTIFIER				
	CCW (XXXXXX)		CONNECT WORD (XXXXXX)		
*IOC27B	DIAG	CHAN	COMMAND	DIAG	C P
	XX	XXXX	XXXXXX	XXXXXXXXXX	X X

	WORD A							WORD B				
	TYP	TER	EXH	EXT	INT	XPL	CONT	EXTEN	ADDRESS	TALLY	S	P
LPW	X	0	X	0	X	0	X000	XX	XXXXXX	XXXX	0	0
DCW	X	X	X	X	X	X	XXXX	XX	XXXXXX	XXXX	X	X

STATUS	CH	TYPE	CAUSE	CHAN	STATUS
EXP	X	A	XX	XXXX	XXXXXX
ACT	X	A	XX	XXXX	XXXXXX
MSK					

EXP  
ACT  
MSK

W7 - Software Monitor Program Stores word with the following format after interrupt (1st interrupt if more than one expected) or interrupt error (no interrupt).



Set if power is off

Not applicable on GIOC or MSU

- Bits 26-29 - Contain the binary count of the entry in the queue table where status information was obtained.
- Bit 31 - Set if terminate interrupt occurred.
- Bit 32 - Set if initiation interrupt occurred.
- Bit 33 - Set if special interrupt occurred.
- Bit 34 - Set if an interrupt is missing or 2nd interrupt is in error.
- Bit 35 - Set if expected status is not received after first interrupt or if first interrupt was not the type expected.

NOTE: If more than one interrupt is expected, it will be the responsibility of the peripheral program to interrogate this word for the occurrence of the second one. If the peripheral program wishes to receive the status from second interrupt, it must issue a request or reset status command.

18 - TRA (address the program wishes to transfer to if the option "skip to next test is set).

NOTE: The Software Monitor Program will return control to this word if the option is set to skip to the next test. It should be noted that a test is a portion of the program that is self-contained and may be entered into without depending on any previous functions performed. A test may contain any number of sub-tests which are dependent upon previous functions performed within the particular test.



W9 - TRA (address the program wishes to transfer to if the option to "loop" is taken).

NOTE: The Software Monitor Program will return control to this word if looping is desired. Control will be returned to W9+1 if looping is not desired.

B. Input/Output Command Initiation For GIOC Testing

Each time the writer of a GIOC T&D Program wishes to issue an I/O command to the GIOC, he must communicate with the Software Monitor Program by a Master Mode Entry having the following call sequence:

	0	5	6	11	12	17	18	23	24	29	35														
W1	0 0 0 0 0 0 0 0 0 0 0 0 1 0 1 0 0 0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0 0											MME 20													
W2	MBZ except diagnostic command										D	C	C	Mem. Port.	GIOC										
W3	MBZ except diagnostic		Channel No.					Channel Command(s)					CCW												
W4	O	S	C	O	O	E	X	H	O	O	Int Sig	O	O	O	O	A	O	O	O	O	O	O	O	Address Extension	LPW(A)
W5	DCW address							Tally					O	O	O	O	O	O	LPW(B)						
W6	Expected Status List Address							O	O	O	L	C	I	M	O	O	O	O	O	O	O	O	No. of Int. Expected	Expect	
W7	Actual Status List Address							O	O	O	O	O	S	C	O	O	O	O	O	O	O	O	No. of Int. Received	Actual	
W8	Return location if Next Test option set												Control Wd.												
W9	Return location if Loop option set												Control Wd.												
W10	Normal return location												Control Wd.												

W1 - MME 20

W2 - Connect Word

This word will be moved, without alteration, to location x in the Monitor program (which is in the same memory controller as the GIOC mailboxes). A GIOC x command will be executed after appropriate tests and initializing.

W3 - Channel Command Word (CCW)

This word will be moved, without alteration, to location y. A command pointer word as described below will be stored in channel 8, 9, 6, 10 depending on the setting of Bits 31-32 in W2.

CPW Word A

0	5	6	8	9	29	30	35
Zero	001		Zero			Zero	

CPW Word B

0	17	18	29	30	35
Y			0 0 0 0 0 0 0 0 0 0 0 0 0 1		Zero

W4 - List Pointer Word (LPW Word A)

W5 - List Pointer Word (LPW Word B)

These two words may be moved to the list channel number defined in W3 and the DCW Address (bits 0-17 of W5) may be modified depending on the configuration of bits 21 and 22 of W6. (See W6, bits 21 - 22.)

W6 - Expected Operation Word

Bits 0-17 - Address of the Expected Status List which is a list of status words which are expected as a result of this I/O operation. This list does not include the interrupt caused by CCW exhaust which occurs on status channel 1.

This is checked for by the monitor but is not stored in Actual Status List. The Expected Status List is not used or accessed by the Monitor except when outputting an error message.

Bits 18-20 - Zero

Bits 21-22 - These two bits effect changes as defined below:

0 0 - No change

0 1 - (a) Add the processor base address register to bits 0-17 of W5.

(b) Store W4 and W5 in the list channel defined in W2.

(c) Store zeros in the data channel defined in W2.

(d) Add the processor base address register to bits 0-17 of Word B of each DCW in the list specified by W5 if the DCW is a data transfer type (i.e., if bits 0-2 of Word B of the DCW are 0, 1, or 2).

1 0 - (a) Store W4 and W5 in the list channel defined in W2.

(b) Store zeros in the data channel defined in W2.

1 1 - Same as 01 and in addition, reset bit 22 of W6.

Bit 23 - Immediate return bit. If this bit is zero, the slave program is roadblocked until the number of status words defined in bits 30-35 has been detected or the time currently in bits 0-17 of W4 of the slave program header has been exceeded. If this bit is 1, control is returned to the slave program immediately.

Bits 24-29 - Zero

Bits 30-35 - Number of words in the Expected Status List.

W7 - Actual Operation Word

Bits 0-17 - Address of the Actual Status List. The interrupt processing routine of the Monitor stores status words in this list as they are processed. The status words are stored in the location which is the sum of bits 0-17 + bits 18-35 + processor base address.

Bits 18-35 - These bits are zeroed when the CIOC command is executed. The Monitor stores information in them as follows:

Bit 23 - Sequence Complete bit. This bit is set to 1 when the number of interrupts received equals the number expected or when the maximum wait time has been exceeded.

Bits 30-35 - After each status word is stored in the Actual Status List this field is incremented by one.

- W3 - The  Control Program will return control to this word if "skip to next test" option is set and an error was detected.
- W9 - The  Control Program will return control to this word if the "loop" option is set.
- W10 - The  Control Program will return control to this word if options mentioned in W8 and W9 are not in effect.

### C. Input/Output Command Initiation For Md-32 Testing

Each time the writer of a MD-32 T&D Program wishes to issue an I/O command to the MD-32, he must do so by a Master Mode Entry with the following call sequence:

	0	17	18	29	30	35
W1	000 000 000 000 011 110			000 000 001 000 000 000		
W2	Zero			Command	Zero	Memory Port #
W3	Disc Address			Memory Address		
W4	Next DCW Relative Address			Command	P	Zero
W5	Current Status Box Storage Adr.			00	S C	I M
W6	Return Location if "Skip to Next Test" Option is set					
W7	Return Location if "Loop" Option is set					
W8	"Normal" Return Location					

W1 - MME (30) DSU IO

W2 - Peripheral Control Word (PCW)

This word will be moved, without alteration, to location X in the Monitor Program (which is in the same memory controller as the Status Boxes). A CIOC X command will be executed after appropriate tests and initializing.

W3 - First DCW Word A

W4 - First DCW Word B

These two words will be moved to the 17th and 18th words of the MD-32 Hardware communications block before the connect command is issued. Also, W3 and W4 will be modified before being transferred if bit 22 of W5 is set (see below).

W5 - Monitor Communications Word

Bits 0-17 - The monitor stores the contents of the current status box in this table when the interrupt from the drum is processed (and also sets bit 20 of W5 when the no. of interrupts listed in bits 30-35 are received).

Bits 18-22 - Are set to zero when the Monitor issues a CIOC.

Bit 20 is the Sequence Complete bit. It is set to 1 by the Monitor when all interrupts are received from the MD-32 or when the maximum wait time (defined in bit 0-17 of W4 in the program header) has been exceeded.

Bit 22 is the DCW modifier bit. If it is reset there is no modification done by the Monitor. If it is set, the following operations are performed:

- (a) Bit 22 is reset.
- (b) The (processor base address  $\div$  64) minus the MD-32 base address is added to the next DCW relative address field of W4 and also to each DCW in the DCW list.

Bit 23 - Immediate return bit. If this bit is zero, the slave program is roadblocked until the specified number of interrupts have occurred from the MD-32 or the maximum wait time has been exceeded. If this bit is 1, control is returned to the slave program immediately.

Bits 30-35 - Number of interrupts expected - This field defines the number of interrupts the T&D Program expects from this I/O command. Control may be returned to the MD-32 T&D Program when this number of interrupts has occurred.

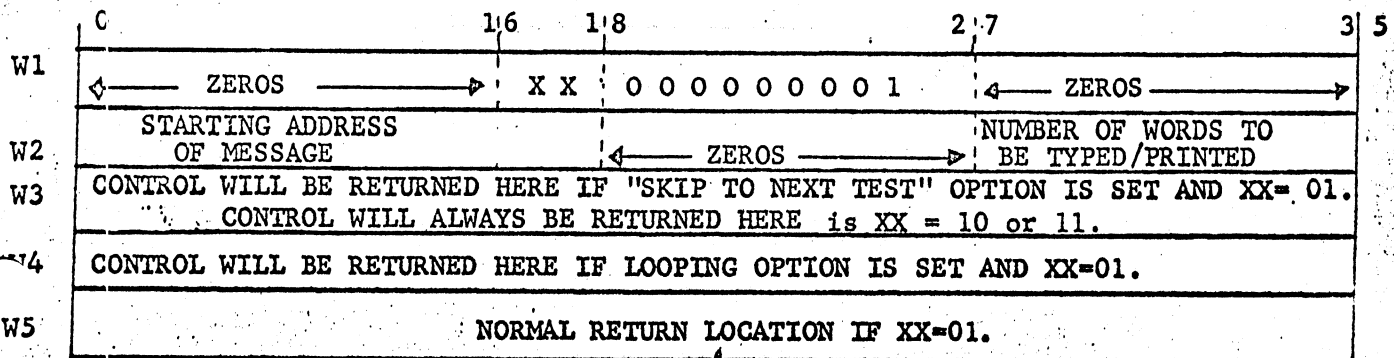
W6 - Return location if Next Test option set.

W7 - Return location if Loop Option set.

W8 - Normal Return location.

D. Print and/or Type Routine -

The person writing T&D programs will want to perform much of his own error detection and output error messages. This routine will allow the programmer to output an error message via the Maintenance Console or printer (determined by operator option), output information messages to the Maintenance Console, or read information via the Maintenance Console. Communication with the Software Monitor Program requires a Master Mode Entry with the following call sequence:



W1 - MME TYPR (XX=01) or TYPEW (XX=10) or TYPER (XX=11). 12

NOTE: MME TYPR - The message will be typed or printed according to the type or print option. When this routine is entered, all of the error options are tested by the Software Monitor Program (looped, Skip, Bypass error timeout, Halt after error, etc.). The programmer has the responsibility of the message format to be typed or printed. The control program will assume the message is for the typewriter. If the print option is in effect, the control program will interrogate the number of successive carriage returns and slew that number of lines after printing.

MME TYPEW - This entry will output a message on the Maintenance Console only. None of the error options are interrogated and control will always be returned to W3.

MME TYPER - This entry is provided to enable a program to issue a Maintenance Console read command. Control is returned to Slave Program after Console Termination with status to A-register.

W2 - Bits 0-17 contain the starting address of the message to be typed or the input area to be typed into. The message or area cannot be "scattered" in memory as only one DCW will be used for the type connect command.

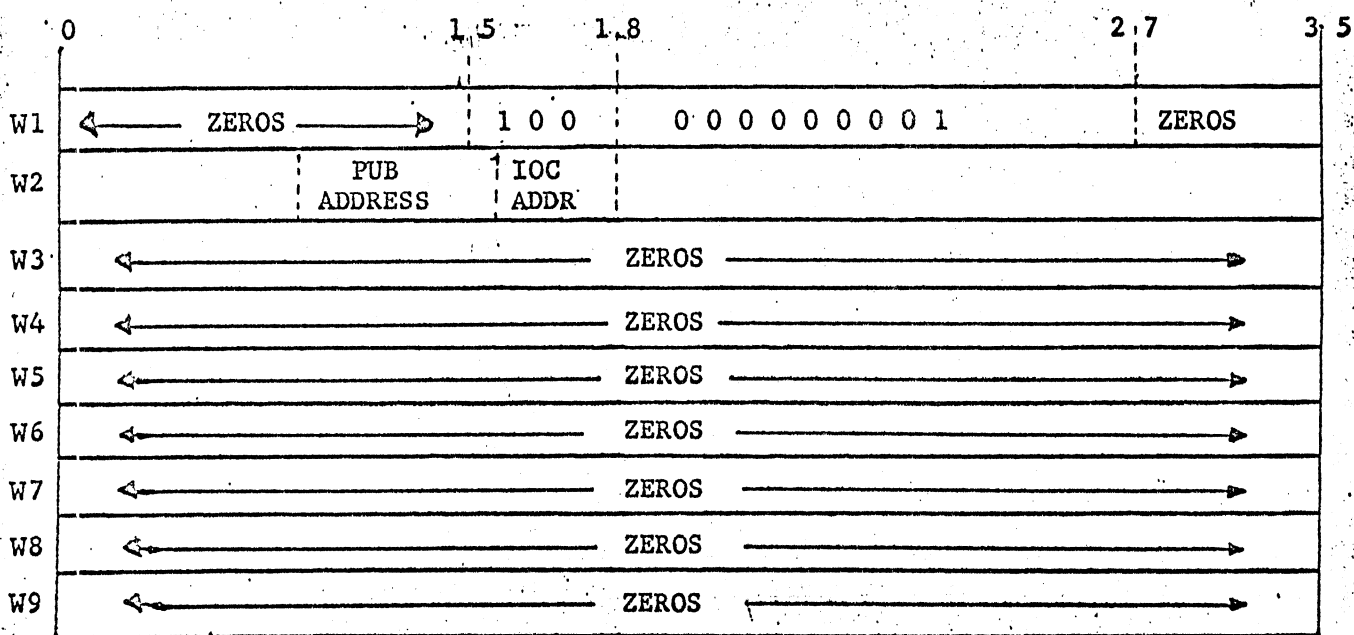
Bits 27-35 contain the binary count of the number of words to be typed out or typed into. The maximum number of words is 777 octal.

W3 - Control will always be returned to this word in the case of an MME TYPEW or MME TYPER. If the entry is a MME TYPER, control will be returned to this word if the "skip to next test" option is set.

W4 - Control will be returned to this word if the entry is a MME TYPR and the "loop" option is set.

E. READ QUEUE COUNTERS AND SECONDARY MAILBOXES ROUTINES

The purpose of this routine is to allow the IOC T&D Program to read the secondary mailboxes, interrupt queue counters, and duplicate interrupt queue counters. Communication with the Software Monitor Program requires a Master Mode Entry with the following call sequence.





W1 - MME RMAIL

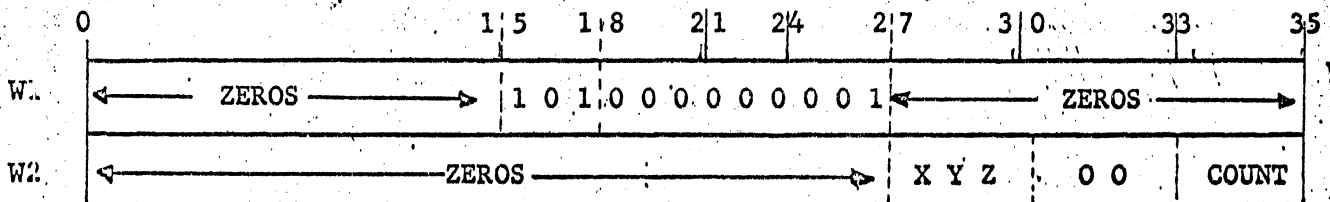
W2 - Contains the PUB number (Bits 12-15) and IOC number (Bits 16-17) of the queue counters and mailboxes to be read.

W3-W9 - Contain zero upon entry. Upon exit, the T&D Control routine will place the following information in these words.

W3	← ZEROS →	INITIATION QUEUE CNTR	← ZEROS →	DUPLICATE INITIATION QUEUE CNTR
W4	← ZEROS →	TERMINATION QUEUE CNTR	← Zeros →	DUPLICATE TERMINATION QUEUE CNTR
W5	← ZEROS →	SPECIAL QUEUE CNTR	← ZEROS →	DUPLICATE SPECIAL QUEUE CNTR
W6	← CONTENTS OF SECONDARY MAILBOX #1 →			
W7	← CONTENTS OF SECONDARY MAILBOX #2 →			
W8	← CONTENTS OF SECONDARY MAILBOX #3 →			
W9	← CONTENTS OF SECONDARY MAILBOX #4 →			

F. SET QUEUE COUNTER ROUTINE

The purpose of this routine is to allow the IOC T&D Program to store the count he wishes in particular queue counter and its duplicate. It should be noted that the count given by the program will be placed in both the queue counter and its duplicate. Communication with the Software Monitor Program requires a Master Mode Entry with the following call sequence.



W1 - MME QCTRS

W2 - Contains the type of interrupt counter desired and the value to set the counter.

Bits 27-29 - Type of interrupt counter to store value into.

Bit 27 - Initiation

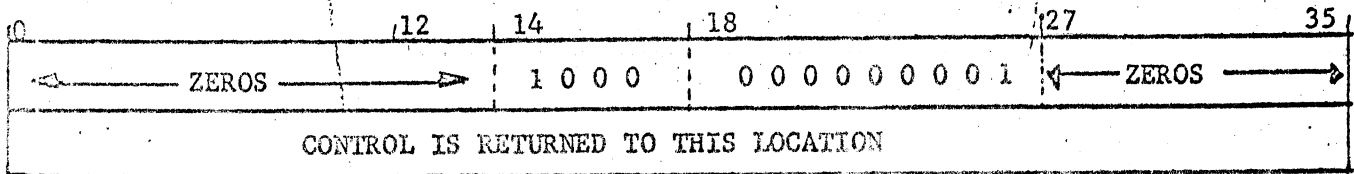
Bit 28 - Termination

Bit 29 - Special

Bits 32-35 - This value will be placed into the queue counter desired and its duplicate.

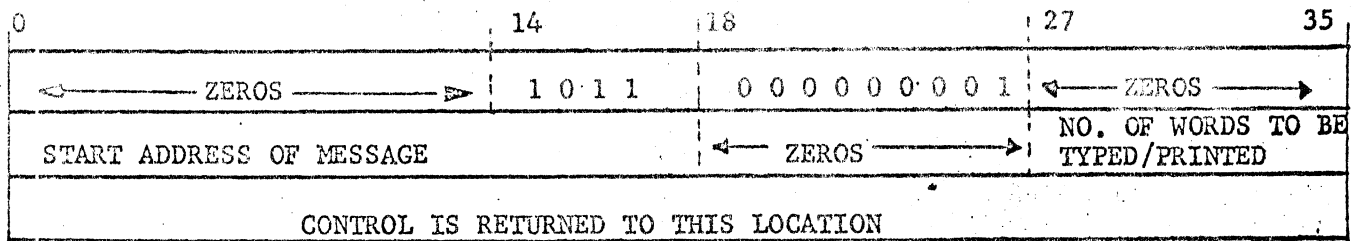
F. OUTPUT LAST STATUS

This routine will type or print (according to option setting) the STATUS and ERROR HEADING of the last I/O operation performed by the Peripheral T&D Program. The format of the message is the same as that mentioned IV-A. The Software Monitor does not interrogate any of the options except the TYPE/PRINT when the routine is executed. Communication with the Software Monitor Program requires the below call sequence:



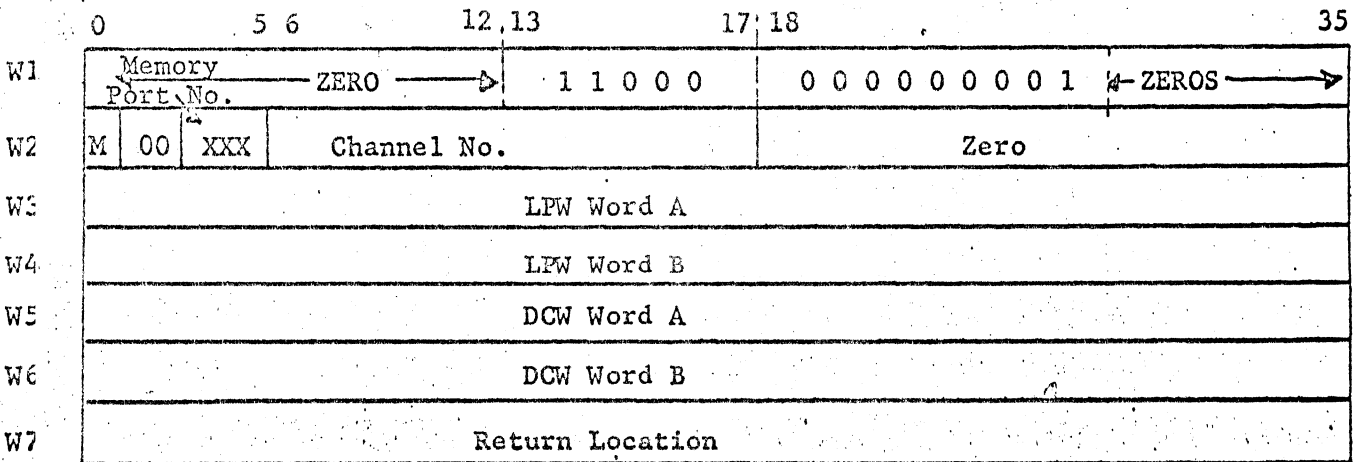
G. PRINT/TYPER WITHOUT OPTIONS

The routine functions as the TYPER routine (IV-D) except that the HALT AFTER ERROR, LOOP, AND SKIP options are ignored by the Software Monitor Program. The call sequence for this routine is a Master Mode Entry as follows:



H. READ GIOC LIST AND DATA CHANNEL WORDS

This routine is to allow the GIOC T&D Program to read the List and Data channel words for a consecutive pair of channels. The Software Monitor must be able to handle this routine by recognizing the following MME call sequence:



Bit 0 of word 2 is the Modification control bit. If bit 0 is zero, the words are transferred from the channel mailbox locations to W3, 4, 5, and 6 without modification.

If bit 0 is one, the processor base register is subtracted from LPW Word B before it is stored and also from DCW Word B if the DCW is a data transfer type. The words in the channel locations remain unchanged.

The Software Monitor will mask off bit 17 of the channel number in W2 to ascertain that a List Pointer pair will always be placed in W3 and W4.

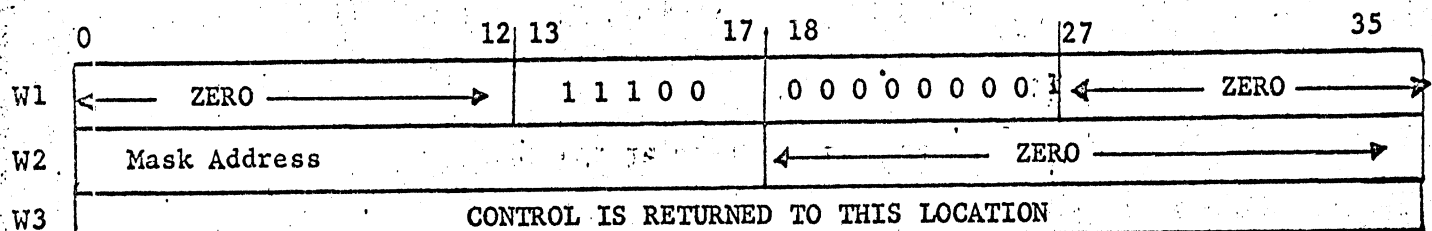
**I. SET GIOC LIST AND DATA CHANNEL WORDS**

This MME is similar to the one to read the channel words except that data is transferred from W3, W4, W5, and W6 to the channel mailbox locations. The address portion of the MME word is 25<sub>10</sub>.

If bit 0 of W2 is one, the processor base address register is added to the address fields by the Software Monitor before the words are stored. The words in the call sequence remain unchanged.

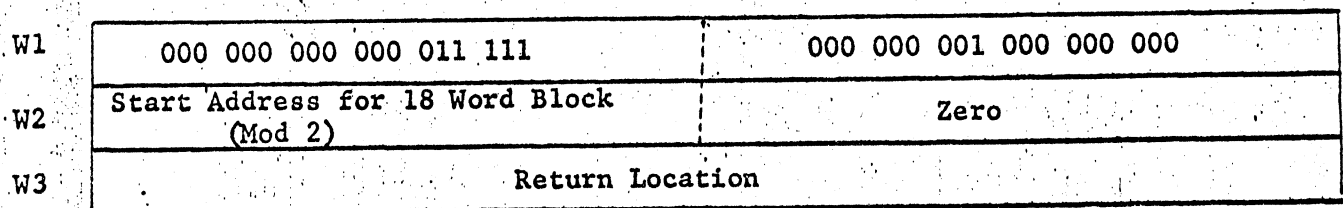
**J. OUTPUT LAST GIOC STATUS**

This routine will type or print (according to option setting) the STATUS and ERROR HEADING of the last I/O operation performed by the GIOC T&D Program. The format of this message is the same as the GIOC error message mentioned in IV - A. The Software Monitor does not interrogate any of the options except the Type/Print when this routine is executed. Communication with the Software Monitor Program requires the following call sequence:



**K. READ MD-32 STATUS BOXES**

Each time the writer of a MD-32 T&D Program wishes to read the 18 status Boxes (16 status boxes and 1st DCW pair), he must do so by a Master Mode Entry with the following call sequence.



W1 - MME (31) RBLOK.

W2 - Bits 0-17 contain the starting location in the slave program where the 18 word block is to be stored into. This starting address must be even. The block will be stored by the Software Monitor as shown on the following page.

W1	Current DCW Address	Status	Pointer
W2	Abnormal DCW Address	Status	
...	...	...	...
W17	Drum Address	Memory Address	
W18	Next DCW Address	Command	P Zero

W1 - Bits 0-17 contain the current DCW address in the slave program (actual address = absolute address + MD-32 Base Address - Base Address Reg.)

- Bits 18-31 contain status information.

- Bits 32-35 contain a four bit code identifying the last abnormal status box into which an entry was made.

W2-W16 - Bits 0-17 contain the address of the DCW pair which was being used when an abnormal condition was detected (actual address = absolute address + MD-32 Base Address - Base Address Register). Bits 18-31 contain status information.

W17 - Bits 0-17 contain the starting MD-32 address where data is to be read from or written into. Bits 18-35 contain the memory address that data is to be written into or read from (actual address = absolute address - Base Address Register).

W18 - Bits 0-17 contain the address of the next DCW pair to be used (actual address = absolute address + MD-32 Base - Base Address Register).

Bits 18-22 contain the DCW Command.

Bit 23 - set defines block size to be 64 words.

- reset defines block size to be 1024 words.

NOTE: All addresses returned to the slave program by the Software Monitor Program will be addresses which are relative to the slave program (ex: current address returned in first word = 104<sub>8</sub> means the current DCW pair was located at 104<sub>8</sub> in the slave program). The Software Monitor Program will not calculate slave address for any absolute address which is Zero or all ones.

L. SET MD-32 STATUS BLOCK

Each time the writer of a MD-32 T&D Program wishes to set the 16 status boxes from data in memory, he must issue a Master Mode Entry having the following call sequence.

W1	000 000 000 000 100 000	18	000 000 0001	27	000 000 000
W2	Start address of 16 word block		Zero		
W3	Return Location				

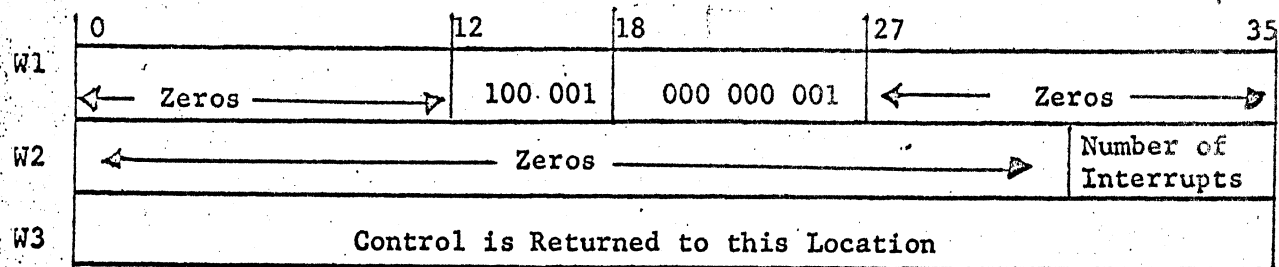
W1 - MME (32) SBLOK

W2 - Bits 0-17 contain the starting address of a 16 word block to be stored into the 16 status boxes. Address must be even.

NOTE: The address portions of the status block (bits 0-17) is set to zero or all ones if the programmer wishes to determine the entries placed in the status block by the MD-32. The Software Monitor Program converts all address in the block to slave address when it receives a MME RBLOK if the addresses are not zero or all ones.

M. RELINQUISH CONTROL FOR MD-32 T&D PROGRAM

This routine is used by the MD-32 T&D Programs to give control back to the Software Monitor until a certain number of interrupts has occurred. The call sequence for this routine is as follows:



When this routine is executed, the Software Monitor Program will not return control to the MD-32 T&D Program until the number of interrupts received is equal to or greater than the number in bits 32 - 35 of W2 or until the maximum wait time for the interrupts (determined by bits 0 - 17 of W4 of the PROGRAM HEADER) has elapsed.



V. SYSTEM CONFIGURATION CHANGES - The T&D Program operating under control of the Software Monitor Program will have to have complete control of the Peripheral, IOC, GIOC, or MD-32 it is testing. The Software Monitor Program will have to delete a peripheral from its system configuration when an on-line Peripheral T&D Program is called into memory. If the T&D Program is an IOC or a GIOC T&D Program, the Software Monitor must delete the entire IOC or GIOC from its system configuration.

The Product Service man should have the capability to delete and add to the Software Monitor's system configuration through the maintenance console.

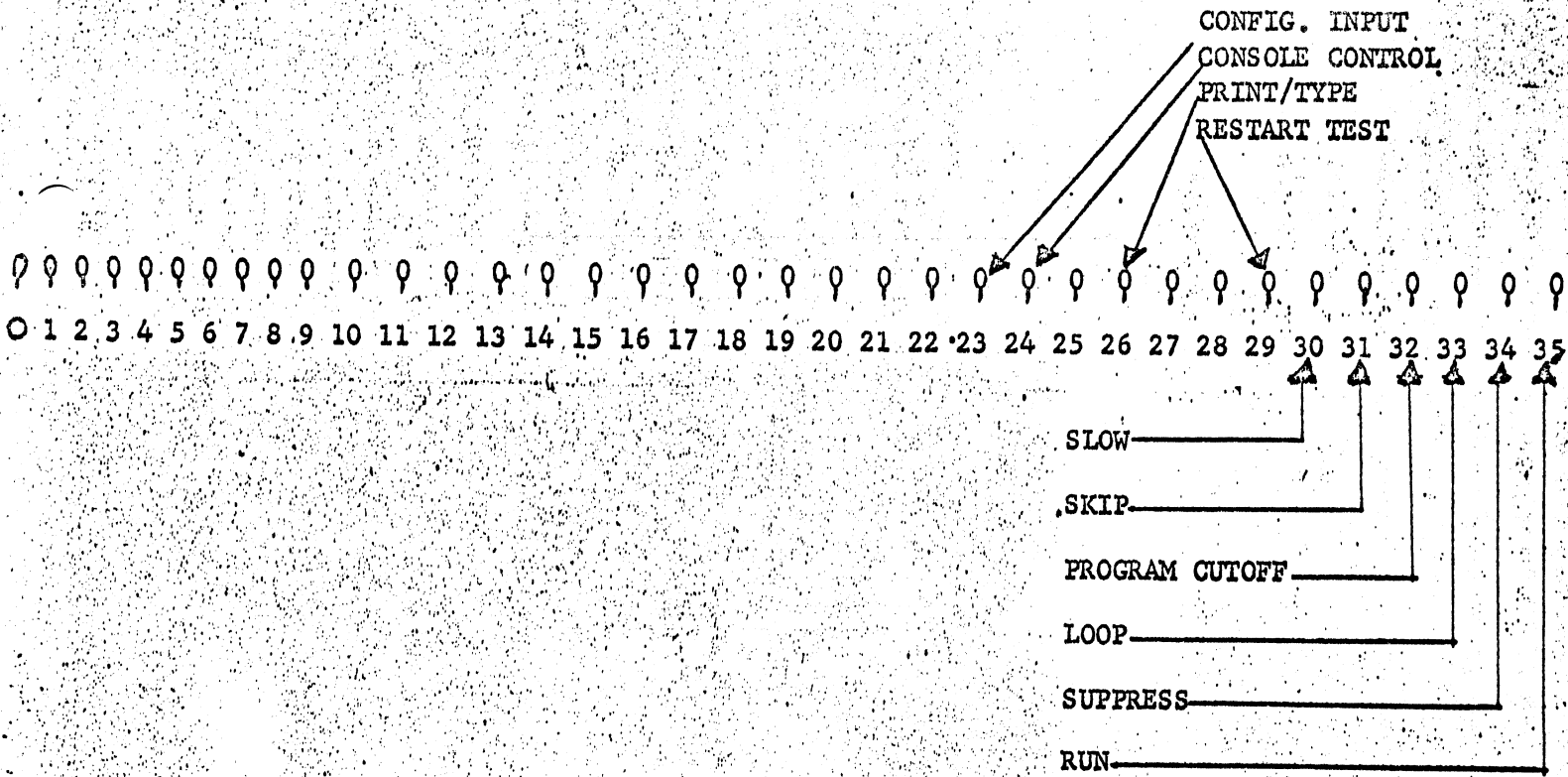
VI. RETURN TO T&D PROGRAM AFTER I/O REQUEST - The Software Monitor will return control to a T&D Program in the following manner after the T&D Program has issued a MME I/O:

- A. IMMEDIATE RETURN - The T&D Program may set a bit in a MME I/O which means it wants returns to the program immediately after the Software Monitor has issued the CIOC command. This feature will be used sparingly by the T&D Programs and only when it is necessary to test certain functions.
- B. NUMBER OF EXPECTED INTERRUPTS IS RECEIVED - Each I/O command will contain the number of interrupts that is expected from the execution of that I/O command. The Software Monitor may return control to the T&D Program when the number of interrupts received is equal to or greater than the number expected.
- C. MAXIMUM WAIT TIME FOR INTERRUPT HAS ELAPSED - The Software Monitor Program may return control to the T&D Program if the expected interrupts have not occurred, but the maximum wait time has elapsed. This condition implies that an interrupt is "missing", and the Software Monitor should output a message to the Product Service man for this condition.

VII. OPERATOR OPTIONS - Switch Control - Primary option control is maintained by using the 36 toggle switches on the processor maintenance panel. Control of certain options may be transferred to the maintenance console by setting switch 24 true (up). (See section 8 for console option).

- A. ERROR OUTPUTS - Error messages may be typed on the maintenance console printed on a high-speed printer, or they may be suppressed. Switch 34 true causes output suppression; switch 34 false allows output as specified by switch 26. For console typeout switch 26 must be false; for printed output switch 26 must be true. (Console control words - TYPE/PRINT/ BYPASS).
- B. HALT/RUN AFTER ERRORS - When an error typeout occurs, it may be desirable to halt further I/O operations from the T&D Program to allow operator action before subsequent tests. This option is provided by use of switch 35. A halt after typeout will occur if switch 35 is false; no stop will occur if true. To proceed and halt at the next error, toggle switch 35 true then false. To run without halts, set switch 35 true. (Console control words - HALT/RUN/GO).

- C. SLOW RATE - A delay between I/O operations may be useful. If switch 30 is true, the Software Monitor Program will not return control to a T&D Program until at least .2 seconds after it normally would have after an I/O request. (Console control words - FAST/SLOW.)
- D. SKIP TO NEXT TEST - If a particular sequence of operations cannot be completed because of failure of a previous function, a skip to the next complete test may be effected by setting switch 31 true. This option is effective only following a typeout. (Console control words - SKIP/NOSKIP.)
- E. RESTART - An error message may be such that a restart is necessary or desirable. It is possible to restart the T&D Program by setting switch 29 true. The restart option is effective only after a halt after typeout. (Console control words - START (RESTART); TEST - PUB-).
- F. T&D PROGRAM CUTOFF - If switch 32 is true (set), the software monitor will not return control to the T&D Program until the switch is reset.



PANEL SWITCH SUMMARY

VIII. MAINTENANCE CONSOLE CONTROL

Certain functions, normally under panel switch control, may be transferred to the operators console by setting switch 24 true. If such is the case, the following vocabulary will be active when a console request is received.

- ABORT - causes an abort with a memory dump.
- BYPASS - suppresses error outputs.
- FAST - negates SLOW option.
- GO - used to continue after an error timeout, but stop after the next error.
- HALT - causes stop after error timeout.
- LOOP - causes current test to be repeated until NOLOOP entered.
- NOLOOP - negates LOOP option.
- NOSKIP - negates SKIP option.
- PRINT - causes error outputs to go that printer on lower numbered PUB.
- PUB - Sets entry points for PUB testing.
- RESET - clears all console options to normal.
- RESTART\* - restarts T&D Program.
- RUN - eliminates halt after error timeout.
- SKIP - causes skip to next test following error timeout.
- SLOW - sets a 200 millisecond delay after every I/O command issued.
- START\* - synonymous with RESTART
- TEST - used with PUB (above) to start at a particular test on that PUB. e.g. TEST 2, PUB 1.
- TYPE - causes error messages to be sent to the Maintenance Console.

\*Effective only during halt after error timeout.

IX. INTERRUPTS

The Software Monitor must handle interrupts caused by a T&D Program differently than those caused by a regular slave program. The differences that come to mind at the present time are as follows:

- A. The Software Monitor will not try error recovery on status errors caused by a T&D Program.
- B. Status information will be sent to the T&D Program and the Software Monitor must output error messages to the Product Service man as previously defined.
- C. The Software Monitor must be able to keep track of time and if an interrupt does not occur within the limit set in the T&D Program Header, output a message to the Product Service man telling him of a missing interrupt.

X. RESERVED AREAS ON DISC AND DRUM DEVICES

It becomes necessary for T&D Programs to have reserved blocks on devices where the recording media is <sup>non</sup>removeable. The purpose of these reserved blocks is so that the T&D Programs can "write" on the storage media without destroying any customer data. The reserved blocks, that Software must not use, for the different types of devices are as follows:

X. RESERVED AREAS ON DISC AND DRUM DEVICES (continued)

- A. DS-20 - First four blocks (000000-000003) and the last block (64 word blocks).
- B. DS-30 - First and last block (64 word blocks).
- C. MD-32 - First block and last two blocks (64 word blocks).