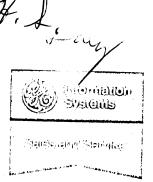
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SA-B601 2/3/69 Page 1 of 18

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SPA-355 STORED PROGRAM ADAPTER

The SPA-355 is a stored program adapter which functions as a high performance, expandable communications subsystem. Now your customers can implement the total communications information system using the 3-D concept without having to expand past system capability. The SPA-355 can support a wide variety of terminals in use today, or planned for announcement shortly; and can support large numbers of these terminals, without degrading the performance of the mainframe system.

The SPA-355 is an extremely *flexible* subsystem. It can be configured to handle terminals or lines operating at from 5 bits per second (almost dc signal) to 50,000 bits per second. Its line adapters have been designed to operate all the most used communications frequencies. And different line frequencies can be operated from one SPA-355 line adapter. This means that the SPA-355 can be accommodated to a customer's communications systems requirements and volume requirements with a more economical configuration than has been true with presently available communications subsystems.

Your customer/prospect benefits from the built-in *reliability* of the SPA-355. Integrated circuits have been used throughout the SPA-355. This technology results in substantially fewer connections and a greater compactness in packaging.

The SPA-355 is being introduced as a communications processor, but its capabilities and growth potential are much greater. In the near future, it will be used as the peripheral control processor on the GE-600. It also provides high-volume terminal capacity, which enables your customer to expand his communications system significantly within one SPA-355.

When compared to other communications processors running large systems, the SPA-355 comes out on top in a *cost-performance* comparison. Its compact packaging scheme and flexibility enable a responsive system to be configured for less money.

TARGETED MARKETS – INITIALLY

- 1) Use the SPA-355 to upgrade your installed GE-600 user to full, 3-D capability. Many of our users have been postponing sizeable communications applications because of the limitations of the DATANET-30 in larger systems. Now that limitation has been overcome.
- 2) Bid the SPA-355 in instances where more than one DATANET-30 would be required to do the job. Price-performance studies have shown that the SPA-355 becomes the price-performance leader at about the point where a second DATANET-30 is indicated.
- 3) Bid the SPA-355 in instances where the ultimate configuration will require more than one DATANET-30, even if the initial system does not, unless a "low-ball" effort is indicated.
- 4) Later this year additional capabilities associated with the SPA-355 will be announced. These capabilities will "fill out" loopholes in the present product posture and will be thoroughly documented to you at that time. In the meantime, start thinking SPA-355.

for Conovel Electric Francis

1.0 PRODUCT DESCRIPTION

The SPA-355 is an advanced subsystem which was designed to become a systems module of the GE-600 3-Dimensional System. It was designed to:

- Provide the GE-600 System with a highly adaptable multi-function systems module which is capable of supporting the large volumes of input and output required in a 3-Dimensional System.
- Provide maximum flexibility of input/output processing including special real-time devices.
- To perform these functions at a very high degree of reliability.

It is planned that the SPA-355 Subsystem will be integrated into the GE-600 System in several carefully planned phases. Phase A will include primarily those communications functions which are currently handled by the DN-30. A major change will occur, however, in the method of connecting the communications processor to the 600. The SPA-355 will not connect through the IOC as is the case with the DATANET*-30, but rather will connect to the 600 Memory. This will permit the 355 to assume a much larger role in the total system as the later software phases develop.

Phase B will include the transfer of all unit record equipment from the 600 main frame to the SPA-355. This will reduce the memory and processor load on the 600 main frame. More importantly, however, it will make all unit record equipment, whether it is local or remote, look alike to the GECOS System.

Phase C will be directed primarily towards the movement of selected data management functions from the 600 processor to the SPA-355.

Other developments which will occur concurrent with this phased development will be:

- Special real-time subsystems, i.e., MICR Reader/Sorters, etc.
- Transfer functions associated with remote terminals from GE-600 to SPA-355.

The description which follows is directed primarily towards the Phase A problem. The descriptions of the hardware, however, will provide a base of information which is required in all phases of development.

- 1.1 The SPA-355 Subsystem is comprised of:
 - SPA-355 Processor
 - Processor Options
 - Adaptors
 - Adaptor Options

The SPA-355 Processor includes the 355 Memory Controller, with 16K of memory, 355 Central Processor Unit, and 355 Input/Output Multiplexer (IOM). The processor options are, an additional 16K of memory and an extended arithmetic package.

^{*}DATANET - Registered Trade-mark of the General Electric Company.

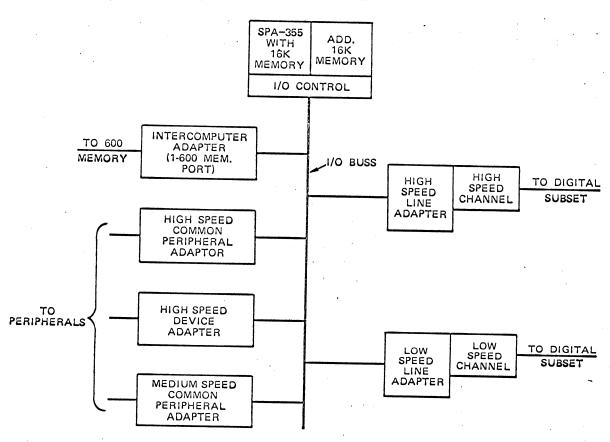
The adapters available for the SPA-355 Subsystem are:

- High speed common peripheral adapters
- Medium speed common peripheral adapter
- High speed device adapter
- Intercomputer adapter (ICA)
- High speed line adapter (HSLA)
- Low speed line adapter (LSLA)

The adapter options are:

- ICA ports
- HSLA high speed channels
- LSLA low speed channels

SPA-355 SUBSYSTEM



MAXIMUM CONFIGURATION:

- 16 CONNECTIONS TO THE I/O BUSS
- 32 K MEMORY
- 3 HIGH SPEED LINE ADAPTERS
 16 HIGH SPEED CHANNELS PER ADAPTER
- 8 LOW SPEED LINE ADAPTERS
 48 LOW SPEED CHANNELS PER ADAPTER
 1 INTERCOMPUTER ADAPTER
- 4 INTERCOMPUTER PORTS

1.1.1 Processor Specifications

• Instruction word size 18 bits

• Data word size 6, 9, 18 or 36 bits

• Instruction Repertoire 96 instructions

Memory speed One microsecond

• Priority interrupt 256 (16 physical levels by 16

functions)

• Memory size 16,384 18-bit words, expandable

to 32,768

Data transfer rate Up to 1,000,000 words per second at up to 36 bits per word.

1.1.2 Processor Description

The 355 Processor is a general-purpose, stored-program, digital computer of microelectronic construction. It is a parallel binary, fixed-point computer that utilizes a random-access, coincident-current core store with a cycle time of one microsecond. The 355 can operate 16 channels of input/output concurrently. The 355 accommodates data of variable word lengths -6, 9, 18 or 36 bits (binary, 2's complement). Data words of these various lengths may be freely intermixed and fully packed in memory. All data word lengths are individually addressable to allow highly efficient processing of tabular data.

The system organization of the 355 follows the pattern of the GE-600 Series Systems. The 355 is a storage-oriented computer with independent store, processor, and input/output modules. These three basic modules are independently timed, and they operate asynchronously of each other. The processor and the input/output multiplexer (which are active units) process data at their own rates and request cycles from the storage module (a passive unit) as the need arises. The only knowledge one active unit has of another is that a storage cycle request may be delayed while the store is responding to the other active unit. Only when the processor executes certain input/output instructions must the processor and the input/output multiplexer communicate with each other.

This type of organization has three main benefits -

- The input/output can operate concurrently with the processor on a "cycle stealing" basis.
- Since neither active unit depends on the store to operate at any fixed speed, various speed stores can be used and intermixed in the same system.
- The modularity of input/output, processor, and storage allows orderly system growth.

The 355 instructions are a subset of the GE-635 instructions and provide characteristics functionally identical to the most commonly used GE-635 instructions.

The 96 machine instructions of the 355 Processor provide operations normally found only in large-scale processors. Instructions include arithmetic and Boolean operations, shifting, comparisons, data movement, and peripheral equipment control operations.

Similarity between SPA-355 and GE-635 instructions encompasses operation code symbolic names and arithmetic algorithms. Programmers familiar with the GE-635 instruction repertoire will be able to make the transition to the SPA-355 with an absolute minimum of retraining due to the similarity between the two systems.

The 96 instructions are in an 18-bit format with one single-address instruction per word. Three index registers and multi-level indirect addressing with indexing at all levels give an addressable storage capability of up to 32,768 18-bit words.

Fault traps (internal interrupts) are included in the processor to provide for program intervention when certain system errors occur. When specific faults occur, program control is automatically transferred to fixed memory locations similar to the GE-635 fault trap technique.

The input/output is designed to facilitate efficient real-time concurrent servicing of multiple peripherals and external devices. Up to 16 channels are provided to accommodate a total data transfer rate of up to one million words per second (with 6, 9, 18 or 36 bits per word) independently of processor operations. Sixteen levels of priority interrupt, with 16 sublevels per level and with corresponding interrupt masks, are provided.

The 355 IOM can control all common peripheral devices currently available with the GE-625, and GE-635 computers. The complement includes devices which are currently undergoing test or subsystem design, but not yet available in the field.

1.1.3 Processor Options

There are two options available for the SPA-355 Processor. These options are:

- Additional 16K memory
- Extended arithmetic

1.1.3.1 Additional Memory

The SPA-355 Processor will contain 16K of memory with electronics and module space for an additional unit of memory. The processor is designed such that the additional memory module can be added in the field with minimal effort.

1.1.3.2 Extended Arithmetic

The SPA-355 Processor includes the capability to perform fixed point arithmetic functions using 36 bit arguments. This includes multiplication and division. The extended precision package will increase this capability to 72 bit fixed point multiplication and division.

There are four instructions which are added with this package:

- Double precision divide (DDUF)
- Double precision Multiply (DMPF)
- Double length left shift (DLLS)
- Double length right shift (DLRS)

1.1.4 Adapters

As can be seen in Figure 1, all adapters connect to the SPA-355 I/O bus. The function of the adapters is to interface peripherals to the SPA-355 Subsystem. A peripheral may be anything from a teletype to a drum as long as the proper adapter is used. The initial adapters are:

- Intercomputer Adapter (ICA)
- High Speed Line Adapter (HSLA)
- Low Speed Line Adapter (LSLA)
- High Speed Common Peripheral Adapter

HPC-

- Medium Speed Common Peripheral Adapter
- High Speed Device Adapter

1.1.4.1 Intercomputer Adapter (ICA)

The 355 (ICA) provides a link between the input/output bus of the 355 IOM and up to four memory controller ports of the GE-600 System.

The ICA transfers data and control information between the two memories. In normal data transfer activities, the ICA acts as an agent of the 355 which controls all detailed transactions.

The GE-600 Series exercises command control over the ICA and can initiate a bootload into the 355 or program interrupt the 355.

The capability to respond to GE-600 System interrupts (thereby becoming the control processor of the system) is included as a standard feature of the ICA, permitting the 355 to assume IOP functions if desired.

1.1.4.2 High Speed Line Adapter (HSLA)

The HSLA is a multi-line communication controller using the associated 355 computer to connect up to 16 low-medium-and high-speed data communication lines. It services a variety of communications terminals and subsystems intended for remote operation at speeds from 5 bps to 50 thousand bits per second.

Each communication line can be used in either simplex, half-duplex or full-duplex transmission mode in two-wire or four-wire operation. Individual HSLA subchannels will normally service any terminal that can transmit and/or receive character-oriented bit-synchronous messages with information codes that do not exceed nine bits in length.

Input data is collected from the communications lines and assembled into characters in subchannel character buffers. The subchannel then requests service and the character is stored in the appropriate subchannel message buffer. Each input character is checked against a character control table taken from word memory. The data character will be compared to the table word to determine if a control character has been received, a special condition has been met or if code conversion required.

A match of a control character or special condition indication dictates the storing of status and a program interrupt. A terminate match, as an Conust older

example, means stop all activity until further commands are received from the program. If no control is required, the character will be stored in the appropriate input buffer with no processor interruption.

1.1.4.3 Low Speed Line Adapter (LSLA)

A LSLA provides the primary facility for connecting low speed terminals to the 355. Up to 48 low speed terminals operating at speeds up to 300 bps can be connected to a single LSLA.

The LSLA operates with low speed terminals in either full or half-duplex for asynchronous data transfer.

The message frame containing a composite of sync, data, and control characters, is the format used for transmitting data between the LSLA to the SPA-355. The frame is composed of a number of 8-bit characters called time slots, each time slot containing one complete character. A 10 cps terminal uses one time slot per frame, a 15 cps terminal uses two time slots per frame, and a 30 cps will use three time slots per frame. Several time slots are allocated to overhead functions; e.g., sync characters, STX, ETX, block check character, and T&D time slot.

The message format requires the presence of a character in each time slot at all times. The LSLA will insert a fill character when no character has been received from the terminal for that time period, and detect and discard any fill characters received in frames from the 355. Consequently, frames may often contain all fill characters in data time slots. The ASCII character DEL (with odd parity) is used as the fill character.

Keyboard terminal modems will be controlled by transmitting a two-character sequence in consecutive time slots dedicated to that particular terminal. Status conditions from the modem will be returned to the 355 as a two-character sequence generated by the LSLA.

Terminals with different communications speeds and code sets can be mixed at the LSLA, with 10, 15, and 30 characters per second expected to be the most commonly used speeds.

1.1.4.4 High Speed Common Peripheral Adapter

The high speed common peripheral adapter allows the high speed common peripherals such as the magnetic tape and disc to connect to the SPA-355 Subsystem.

The maximum character rate is 500 KC (83.3 KC word rate).

The adapter meets the response time of the peripheral it is serving during command sequences, on status service and data services as outlined in the common peripheral specification.

Each adapter is capable of buffering two 36 bit words on read operations and two 36 bit words on write operations.

1.1.4.5 Medium Speed Common Peripheral Adapter

The medium speed common peripheral adapter allows character type common peripheral devices such as the line printer, card reader, and console to connect to a SPA-355 Subsystem.

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The maximum character rate is 150 KC.

The adapter meets the response time of the peripheral it is serving during command sequences, on status service and data services as outlined in the common peripheral specification.

Each adapter is capable of buffering one 6-bit character on read operations and one 6-bit character on write operation.

1.1.4.6 High Speed Device Adapter

The high speed device adapter allows any standard 605 high speed peripheral such as magnetic tape or disc to connect to a SPA-355 Subsystem.

The adapter is capable of operating directly at 500 KC or indirectly at 250 KC peak I/O access interrupt rates.

The adapter is capable of buffering one data word on output. No buffering is required on input data.

1.2 Software

1.2.1 GEneral Remote Terminal Supervisor-255(GERTS/355)

The GERTS/355 is a remote terminal supervisor for operation in the GE-635/355 environment under the GEneral Comprehensive Operating Supervisor III (GECOS III). The 355 and remote terminal resident portions of GERTS will operate with minimum change in the 655 System. GERTS/355 performs the following functions:

- Utilizes a real-time communications subsystem which receives and processes information from remote terminals for direct input to the GE-635 computer system. After data has been processed by GECOS III within the GE-635, the 355 may (under user control) transmit all or part of the output resulting from the processing to a remote terminal over communication lines.
- Allows any type of job to be submitted from a remote site and the output (all or part) to be directed back to the originating terminal, another terminal, or to have it printed and/or punched at the central site.
- Allows for a mixture of communication lines between the 355 and the remote terminals: (1) wideband (10K-50K bps); (2) voice grade (300-10K bps); (3) low speed (100-300 bps).
- Allows a slave (user's) program to communicate directly with a terminal.
- Allows the remote terminal operator to communicate with the system through a control card language to request specific actions from the operating system.
- Safeguards access to the central site by requiring a password from the terminal at the time the communication connection is established.
- Will allow the terminal operator to break the connection with the central site after the programs and data have been transmitted and reestablish it later to request the output.

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1.2.2 Assembler

The 355 Assembler is a program that executes on any GE-600 Series computer. It operates under the standard operating supervisor (GECOS III) and uses the generalized input/output services of the GEneral File and Record Control (GEFRC).

The Assembler accepts as input symbolic 355 machine language instructions and produces relocatable or absolute binary card images on the program output device. A list of the symbolic program and its assembled equivalent is produced on the list output unit.

1.2.3 Simulator

The 355 Simulator is a program that executes on any GE-600 Series computer. The program operates under GECOS III, and uses the generalized input/output services of GEFRC.

The simulator simulates all instructions of the 355 except those which pertain to input/output. A set of special input/output instructions are provided that allows simulation of these functions.

1.2.4 Utility Package

The Utility Package for the 355 is a set of routines and subroutines consisting of a monitor, input/output subroutines, a loader, and a dump routine.

2.0 RECOMMENDED PRICE

DEVICE	MONTHLY RENTAL	SALE PRICE	MONTHLY MAINT.
355 Processor			
Includes 16K Memory, I/O Control	\$2,400	\$110,000	\$200
Additional 16K Memory	900	41,850	63
Extended Arithmetic Package	150	7,350	13
Intercomputer Adapter (Includes 1 Port)	295	13,500	25
Additional ICA Port	120	5,500	10
High Speed Common Peripheral Adapter	350	16,000	30
High Speed Device Adapter	275	12,600	23
Medium Speed Common Peripheral Adapter	250	12,250	20
High Speed Line Adapter	800	34,450	111
High Speed Channel	85	3,550	14
High Speed Channel with Automatic Call Unit	95	3,950	16
Low Speed Line Adapter	650	28,550	79
Low Speed Channel	25	1,050	4 ·

35 5	2,400		HSLA	800	
Memry	900		16-HSC	1360	•
ICA	295				
3 ports	360			2160/m	
2-LSLA	1300 3	reggins 4 LILA	us 95 / 10 pm	w TTY'S ON 1	34 hand 2741's
96 - LSC	2400		•		
	7,655/ms				
	13001				•
	8,955	40		•	
•	,	25			
quation:	Cons = 3,9	55 + 37 * Ni	+ 135 X	NZ	
0				•	
		N1 = #	1 TTY		
•			ARDS		•

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3.0 COMPETITIVE COMPARISONS

Competition was based upon communication capability as the IOP capability is not well defined at this time.

The DATANET-30 is not considered part of the competition and is included as a reference base only.

The competitive comparisons were made for several communications configurations ranging from present day time sharing to future RESOURCE requirements:

- 1. 50 Teletype only for time sharing
- 2. 45 Teletype

5 Low Speed Lines

Present Commercial

8 Voice Grade Lines

1 TELPAK

3. 45 Teletype

35 Low Speed Lines

Future Commercial

15 Voice Grade Lines

2 TELPAK

- 4. 10 Voice Grade for present ISD
- 5. 20 Voice Grade for future ISD

6. 32 Teletype

Present RESOURCE

16 Voice Grade

7. 64 Teletype

Future #1 RESOURCE

32 Voice Grade

8. 64 Teletype

Future #2 RESOURCE

16 Voice Grade

These configurations are considered to be representative for GE-600 Systems requirements with no effort made to configure in favor of the 355 or any of the candidates.

The GERTS rules were applied to the DATANET-30, requiring that up to five DATANET-30's are required for two of the configurations. Also, the processors felt to roughly equal the DATANET-30 were multiple for various configurations. The more powerful processors were considered to be capable of handling all configurations with a single processor.

The candidates price and rental were calculated and are shown in graphic form in Figures 3 and 4 and tabular form in Figure 2.

The 355 is compared to competition in two ways:

- 1. As a communications processor.
- As communications gear only (without processor or memory) to compare fairly with the multi-line controllers.

For further confidence, the IBM 2700 series with added memory cost at (200 words/low speed line, 600 words/high speed line, and 8K supervisor) x (\$2,800 sale or \$55/Mo.) per 1K words and 20% of all this was added to allow for processor usage.

The candidates are:

- 1. Univac 418 II
- Honeywell 416
- 3. Honeywell 516
- 4. Digital Equipment Corporation PDP-9
- 5. Univac CTMC
- 6. Burroughs DCP
- 7. IBM 2700 Series

3.1 Univac 418 II

The Univac 418 Systems are primarily intended for real time and communication applications.

The Univac 418 II processor is an expensive but very capable unit. It uses a 2 microsecond core storage expandable from 4 to 64 K of 18-bit words. It is used in several communications systems, either alone or interfaced to a 1108. It can handle a full range of peripherals including drums (FH330 or FH880) and mass storage (FASTRAND II).

The 418 II has six primary registers which includes 3 - 18-bit arithmetic registers. All index registers (8) are in core storage.

The 418 II has 14 discrete internal interrupt levels and 96 additional levels for I/O channels.

The 418 II can accommodate several varieties of transmission line adapters:

- 1. Low speed (up to 300 bps)
- 2. Medium speed (up to 1600 bps)
- 3. Parallel input (up to 75 characters/sec)
- 4. Parallel output (up to 75 characters/sec)
- 5. High speed (600 50,000 bps)
- 6. Dial

Consequently, the 418 II is a very flexible and powerful communications processor, however, it is too expensive to be very popular.

3.2 Honeywell 416

The Honeywell DDP-416 is the junior member of a three-computer family consisting of the DDP-116, DDP-416, and the DDP-516. The DDP-416 is a desk size, word-oriented computer intended primarily for process control and small-scale scientific applications. Its computational capabilities are limited; e.g., only one working register, no index registers, and no floating-point capability. Its instruction repertoire is geared primarily to the requirements of its input/output environment, which can be quite extensive. However, these apparent limitations in computational ability are partially compensated for by an extremely rapid (0.96 microsecond) memory cycle time. Many relatively complicated

computational operations can be processed with comparative rapidity. The onus, of course, falls on the programmer, who is denied the more sophisticated tools of larger, and more expensive computers.

The 416 handles communications by the use of multi-line and single line controllers. There are three varieties of multi-line controllers:

- 1. Low Capacity
- 2. High Capacity
- 3. Programmed

The low capacity version has a low entry price but expensive per line charge. The high capacity version has a high entry price and low per line charge. The programmed version has low entry and low per line cost but requires virtually all the processor to operate.

In the configuration analysis, the direct memory access (DMA) price was used as a computer interface price. This price is very close to quotes that ISD received from Honeywell for a memory interface to a GE-600.

The 416 has approximately the overall capability of the DATANET-30 and was considered to need multiple processors in some of the configurations.

Though the 416 can handle communications lines, the system lacks flexibility and performance. It is a small inexpensive machine and cannot be expected to perform well in a GE-600 System environment.

3.3 Honeywell 516

The Honeywell DDP-516 is the senior member of a three-computer family consisting of the DDP-116, DDP-416 and DDP-516. It is a desk-size, word-oriented computer intended primarily for control applications with moderate provisions for small-scale scientific data processing. It has two accumulators, one index register, and indirect addressing. Its instruction repertoire is geared primarily to the requirements of an extensive input/output environment, but a large arithmetic subroutine library and an extremely rapid core memory cycle time (0.96 microsecond) augment the programming of computation tasks.

All the communications capability available to the 416 is available to the 516. Flexibility and overall system performance of the 516 are also deficient for a GE-600 System.

A comparison of the 416 and 516 is shown below:

Characteristics	DDP-416	DDP-516	
Number of Instructions	30	72	
Working Registers	1	2	
Index Registers	0	1	
Indirect Addressing	Yes	Yes	
Maximum Memory Size (16-bit words)	16,384	32,768	
Arithmetic Operations -			
Fixed Point —			
Single-precision	Add and subtract by instruction; multiply and divide by subroutine	Add and subtract by instruction; multiply and divide by subroutine or by optional instructions.	
Double-precision	Add, subtract, multiply, and divide by subroutine.	Add, subtract, multiply, and divide by subroutine. Add and subtract optionally by instruction.	
Floating Point —			
Single-precision	No provision. By subroutine.		
Double-precision	No provision.	By subroutine.	
Overflow Indication	Indirect; checked by testing for a sign change in the high-order bit position.	Direct; sets testable indicator.	
Addressable Memory (no indexing or indirect addressing)	1024 word locations (one of two 512-word sectors)	1024 word locations (one of two 512-word sectors)	
Memory Parity Checking	Optional.	Optional.	

3.4 Digital Equipment Corporation PDP-9

The PDP-9 is the fourth in a series of computers with a word length of 18 bits produced by the Digital Equipment Corporation. The line consists of the PDP-1, PDP-4, PDP-7, and PDP-9. Only the PDP-9 is currently marketed, although DEC still installs peripheral devices on all PDP systems in the field.

The PDP-9 is a direct descendent of the PDP-7 and PDP-4 with an identical instruction repertoire but with expanded capabilities. The PDP-9 Basic Software is a direct copy of the PDP-7 Basic Software, and, in most installations, programs written in the PDP-9 Basic Assembly language can be run on the PDP-7. The PDP-9 Advanced Software is being retrofitted to run on the PDP-7.

The PDP-9 is a highly modular, small scale computer that can perform a variety of functions in many different environments. The marketing emphasis has been in the scientific, control, and data communications field.

DEC offers various facilities for data communications input/output with the PDP-9.

The Type LT09A option provides control for up to five teletype stations; Teletype Models 33 or 35 ASR and 33 or 35 KSR can be used. Each line station requires an LT09B interface for each line unit and an LT09C EIA Line Adapter. The LT09A interfaces to the PDP-9 I/O bus and to the program interrupt facility.

The Type DP09A Data Communications System provides a single full-duplex synchronous channel between the PDP-9 I/O bus and a data set with an EIA RS-232 B interface at speeds of 2000, 2400, or 40,800 bits per second.

The DP09A contains the computer interface, the EIA interface, input and output control logic, input and output buffers, and input and output shift registers. Data is transferred one character at a time between the PDP-9 accumulator and the DP09A input or output buffer. The DP09A has the control logic for assembling one character in the input shift register when receiving data and for disassembling one character from the output shift register when transmitting data. This double buffering allows the PDP-9 a full character time for emptying the input buffer or replenishing the output buffer.

Control of the communications terminal is through Input/Output Transfer instructions. The DP09A uses six input/output device codes.

The 680 Data Communications System, which uses a PDP-8 computer to control the data communications facilities, can interface to the PDP-9 I/O bus via the DB98A Interprocessor Buffer.

The 680 System, which uses a PDP-8, is the only reasonable answer to the configurations. Even though two processors, PDP-8 and PDP-9, are required, the prices are competitive. The PDP's are not for lease, however, which lessens their position.

3.5 Burrough Data Communication Processors (DCP)

The DCP handles the interfacing between the B6500/7500 systems and remote devices. Each I/O multiplexer can accommodate up to four data communications processors, and each DCP can control up to 256 communications lines. Thus, a B6500/7500 system can connect up to 2048 lines. The DCP is a special purpose computer that contains the logic and memory required to perform the basic functions associated with sending and receiving data over communications lines. No message buffering is in DCP which qualifies it as a multi-line controller in the definitions used in the analysis.

3.6 IBM 2700 Series — Multi-line Controllers

The IBM 2700 series multi-line controllers provide the 360 series with a communications interface. Three models of the series are available operating under the following configurations.

2701

Connects to 360 models 20, 40, 44, 50, 65, 67 and 75 via a selector or multiplexer channel.

Terminates up to:

4 HDX, Asynch., 600 bps max. or

2 HDX, Synch., 230, 400 bps max.

Note: 4 HDX, Synch., 230, 400 bps max. lines may be connected but only 2 may be active at any given time.

2702

Connects to 360 models 30, 40, 44, 50, 65, 67 and 75 via a multiplexer channel.

Terminates up to:

31 HDX, Asynch., 200 bps max. or

15 HDX, Asynch., 600 bps max.

2703

Connects to 360 models 30, 40, 44, 50, 65, 67 and 75 via a multiplexer channel.

Terminates up to:

176 H, Asynch., 180 bps max. or

72 HDX, Asynch., 600 bps max. or

48 HDX, Synch., 1200, 2000, 2400 bps max.

In the teletype only configurations the 2700 series prices are quite competitive. The introduction of voice grade and broadband lines, however, produces a decided upward swing in price.

A point of interest in discussing the 2700 series is that all transmission above 600 bps is done in the synchronous mode using the Binary Synchronous Communication — BSC—line discipline. All competitive equipment runs asynchronously up to 1800 bps.

The use of broadband lines with the 2701 is limited to a maximum of four lines per 2701, only two of which can be active at any given time.

The IBM 2700 series is considered to be the prime competition, so it was analyzed in more detail. The 355 is compared to the 2700 series in two ways:

- 1. The 355 communications only (no CPU or memory) vs. the 2700.
- 2. The 355 system vs. the 2700 with costs allowed for equivalent memory and processor.

The graphs (Figures 3 and 4) show that the 355 is competitive with the 2700 series on both counts.

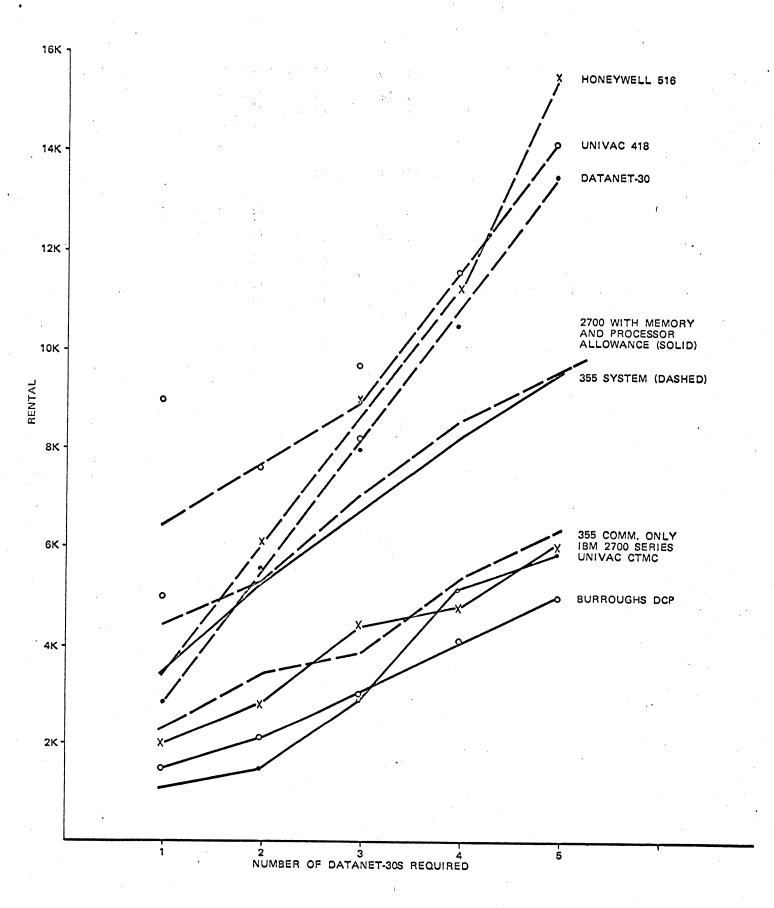


FIGURE 3

for Annual Minustry To at wrong and

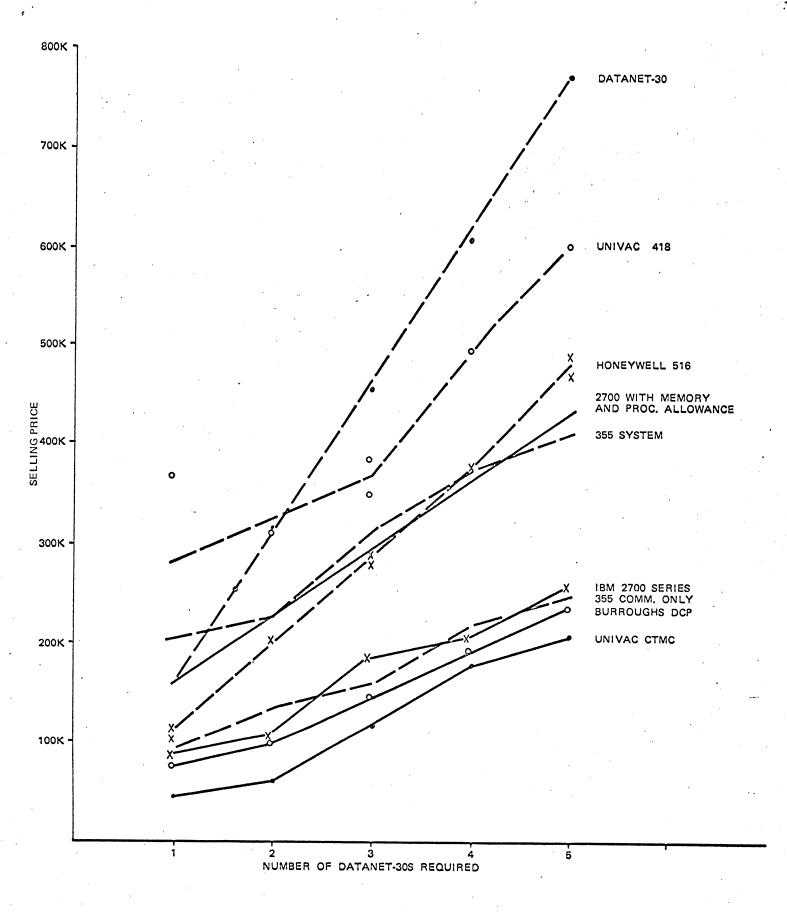


FIGURE 4

for Great Storing Theory and Anti-

