~~6 75~~ ~~Alone~~ Next Multics machine.

645 changes

no access control on PTW's,

Ring hardware

SCU / 635 compatibility

4 box system → 8 ?

600 ~~#~~ # of ports

amount of memory

355 Configuration restriction formulae

Direct I/O channel for 655 to allow high speed devices.

List control channels

What are IOC plans? Can 355 replace it?

650 clock or 8040 & ½ mike memory.

Bulk core + large memory plans.

DS-120, Datacell, etc.

10^{12} bit memory.

What is the approach to better reliability for the 655

GE/Phoenix

1/9/70 Discussion topics

600-line/655 Technology:

Most RAR instr. use 2 cycles now - So 2 cpu opsys needs work.

- What port count, memory size, active unit # restrictions are on 655? ✓

- What is clock in new controller doing? Can it be adapted to look like a 645 clock, or can an 8040 controller be built? 33 bit clock. No problem.

- Is there a collection of more detailed specs - EPS or whatever for 655 memory and processor.

- Why is ~~that~~ 1st delivery so far away in time?

- What is the measured throughput improvement for GECOS III ~~III~~ outside on the 655? Not yet known - a complete 655 is not yet in operation.

- ~~Does~~ GECOS III TSS still use dedicated core. Never did.

- What is the plan for GECOS IV? Evolution is all that has been planned.
  Convert operand ~~words~~ to larger word mode

- 655 privileged instruction set - anything new or changed? How does Mem Controller communicate. (Need read-alter-rewrite arrangement for channel masks.) How interrupts ~~struct~~ are changed? 4 mask/~~per~~ system controller

(RAR gone. Can install STAC again) (possible)

Margin: [illegible] carried across the interface. 72 bit integer.

A.M. R. Stevens , Church, Saul

Plans:

Will merge RESOURCE of GCOS III

GCOS is basically complete now; small extensions will come

Nothing in ~~[illegible]~~ higher language work; hopeful

DS160 - not to be offered DS[illegible] instead

RAR is great for efficiency — new hardware instr { lda + clear storage / ldq + clear / SZN + clear }

P.M. Jim Dahl, Bill Shelley

Lee Wilkinson

Gordon Williams

Robert [illegible]

Dick [illegible]

John [illegible]

30% of hardware in 655 cpu is maintenance oriented

Cond organization 1 word / [illegible] 4[illegible] words in 655

16 registers [illegible]

System Controller has a 2 way interleave for 64 K x 2 modules

~~645~~ for 655 has 4 ports like 635, but can have 8 if [illegible]

Datanet 355 -

- Need more information on configuration restrictions

- What language is DN 355 programmed in. On GE-MAP
  what computer does the translation operate? 635/655 CPU

- What DN 355 Control programs are delivered with it? DN 30 rewrite plan to upgrade

- What is the view on how to handle 200-300 or
  more Terminals. (What about advanced Technology,
  discuss copy of GIOC? What is feeling about willingness.)

- Any plans for less control demand capability? ✓

- Any plan for "Direct" I/O channel for HS devices?

- What is the follow on to the 355.

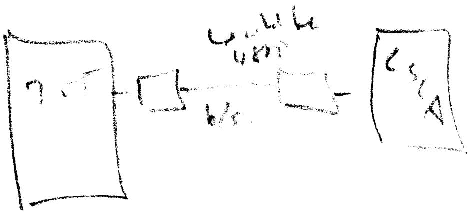
- What are the plans for upgrade of the IOC? IOM?
  4 port dev.

18 bit 256K address fields everywhere

IOM looks like 610C but for HPC class things. Uses 64 multiplexed channels.
allows 6, 9, 18, 36 or 72 bit channels
(big difference with I200)
PRT 300 is a 9 bit ASCII printer. No
code conversion anything.
Chain computer store is loadable by program.

355 Multiplexer ← 100 ms →
LSLA [illegible] 53 slots

1 slot / Terminal for ≤ 10 ch/sec
2 slots / 20 – 30 ch/sec
3 slots for TN 300



Can put 6 LSLA's

355 is a 4-port device [illegible] via IOC

355 has 12 slots, 1 – 1024 2 – [illegible]
9 bays

General –

- Bulk core (addressable or swappable) ✓

- DS-120 (when?) Mid year delivery — how many channels
  DS-175 (DN355) 4 X # of shipments will be heard on IBM 1971

- DS-170 follow-on, 270 follow-on?
  3 – 270 Solution, etc. ~~[illegible]~~ DSU270 X4

- Anything like MSU 302 for 655? **no**

- Datacell or other large memory plan — $8 \times 10^9 \times 6 = 1.2 \times 10^{10}$
  MSS-860 | 750 X 10^6 ch/box | X 4 or 8 boxes = 16 X a full 2314. Del. in Nov — CDC 9720 Big Big Disk
- 10^{12} bit memory, laser addressable. laser stuff, etc.

- What is being done to upgrade reliability record of 600 line ease of trouble shooting, etc. ✓
  (esp. memory core, etc.)

- Who is supplying the new, faster core memories? { Local design / purchase / memory designed plane.

- Storable, wired serial numbers in all hardware units?

- Partitioned 645 has a crosstalk/noise problem. How solved?

Would like to add book case, but Marketing is dragging feet.
An order would be well received by engineering dept.

Potential changes to 645 in a redo:

1. No access control on Page Table Words

2. Ring protect in hardware. (This is a big order.)

3. 8 base registers, permanently coupled { register number / Base number }

4. IT, XED, RPD, etc; remove and replace with a compatability fault. Eliminates need for SCU.

5. Store interrupt number and skip fault

6. Effective absolute address computation instruction ✓
(gives address of SDW or PTW or word, as desired)

7. Ability to store CPU tag in slow mode (10 or 18 bit tag must be better.)

8. Store data, wired serial numbers in all units

1. Ability to read directly, as many configuration switch settings as possible.

10 ASCII-interface printer PRT-300 + all other peripheral
type to equal ... [illegible] years

11. GIOC - only needs 1 status channel and 1 connect channel. ✓

12. GIOC should be able to use ~~[illegible]~~ appending hardware when appropriate. ✓

13. Reconfiguration set channel via I/O path. ✓

14. Upgrade drum controller? ✓

15. ~~Don't~~ run Memory command (SMIC, CIOC, etc.) ✓
address these appending hardware.

16. Support for GECOS/635 program would be easier with ✓
a ~~slave mode~~ master mode loadable base register which
acts like 635 BAR -; would ease stealing of
Basic, for example.

17 No SDW's in Associative Memory.

18. Could eliminate 2 page sizes
Single page size would help.

19 Absolute mode not needed.