Meeting with HIS / IPC   9/20/77   Large Memory System

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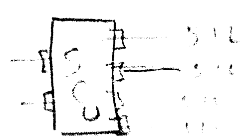
1st phase   40 bits EDAC   1k chips   #INT to DA   inside CPU.
2nd phase   40 bits EDAC ; 4k chips   1 - 1.2 μsec.   double word

Hardware changes
17 boards to 4 plus SCU   11 new boards,   2 new, 6 modified
18 bit micro to 24 address line.



2 active ports.

Can be done on site | CPU / IOM   18 → 21 address bits.
~ 2 boards   10 wire changes each, some backwiring
1. "second" carry speed also, to keep speed constant.
(2x6 bit adders → 4x6 bit adders)

4k chips are not yet in production; only 1 vendor planning to build
HMOS
Backup plan is to go to 2k chips designed for IPC.

1 box
M.
1k → 128k
2k → 256k
4k → 512k
} can fit in easily

Access of chip   350 ns ; cycle ~1 μs
Access of CPU   ~1 μs ;

Reliability : 1 chip / day will fail ; with EDAC ~ 168 hr / failure
(8M word memory)   (some model was used ; will try to get details)

Interested in exercisor models.

(No plans for a spare module;

80 chip stations / board : spares at the board level & chip level.

Cache

4-level set associative 2k words 512K/level
128 column
4 words / block

Wired in per column, modified round robin, used in 6070.

Speed not specified ~100 ns

What would speed of 6180 be if 100% hit ratio.

(Side topic)

On 645 all stores of control unit were buffered; on 6180 they are not.

(on 6000 they are not; trouble in Multics was SCU's ... the cases.)

(Has no estimate on difficulty of retrofitting a buffer)

Hit ratio: have no estimate at all.

2 issues:

1. 6180 mix is different than 6080 mix.
2. Shared writable segments — change mix.

Another question: what would speed be at 0% hit ratio, 1.2μ memory.

Does know what AMO means? Paul Adair ...