INTERDEPARTMENTAL

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from the office of

To: Ed Fredkin

From: J. H. Saltzer

Date: November 28, 1973

Bob Scott has received a new large memory proposal from HISI. Technically, the proposal appears identical to the earlier proposals, but the entry price has been significantly reduced. I have been puzzling how to describe the proposal succinctly because individual aspects are bundled and hard to sort out, but the following seems like a fair description:

1. Today's 6180, with 2 cpus, one IOM, 384k of 0.5 μsec memory, and 2M words of bulk store, has a purchase price of $4.8M. (There are also disks, tapes, printers, and communication equipment worth about $1.5M).

2. HISI's current proposal would replace the bulk store and 384k memory with a 2M word 1.2 μsec primary (MOS) memory, add a cache to each cpu, and increase the $4.8M price to $5.6M.

3. After that replacement, HISI offers to provide additional 1.2 μsec MOS memory in 2-million word increments at 1.6¢/bit, or $1.1M per 2M words. Thus, a 4M-word system would cost about $6.7M, and an 8M-word system about $8.9M. (Not counting $1.5M in peripherals.)

I have described all the prices in terms of purchase, for simplicity; HISI is prepared to rent or sell, as desired. IPC has set its current prices and budgets around the price and performance of the $4.8M system. Either an IPC price increase on the order of 20% or a 20% increase in billable usage (about $30k/month) would be needed to pay for such a system.

As for system performance, there are two effects: the 2M word memory would eliminate about 85% of the paging activity, producing a 20-30% performance improvement. The combination of cache and 1.2 μsec memory produces a complex effect, depending on the hit ratio of the cache. As shown by the accompanying memo, any hit ratio higher than .54 would probably not degrade performance; a hit ratio in the range near 0.80 — 0.8% would probably increase performance by about 30%. Thus the proposal described in point two would probably produce a system with a better price/performance ratio, but perhaps with more capacity than sellable at current IPC rates.

This apparently increased price/performance ratio is actually the result of a comparison with a system which is operating well below its expected performance. The 6180 was anticipated to be a 0.95 mips processor, rather than a 0.65 mips one, and the bulk store was expected to be about twice as fast, so that paging delays are swallowing up about 10% more of the system time than expected.

To summarize,

	CPU speed	Useful time after paging	Computation available to users
expected	.95 mips	70%	.66 mips/cpu
available	.65 mips	60%	.39 mips/cpu

Thus, the computation available to the user, on which price/performance should be judged, is about .39/.66 = .59 of that expected. Given these observations, the proposal to add a cache and replace the bulk store with directly addressable 1.2 μsec memory would bring the system performance back up to the range originally anticipated. To add a third line to the above chart, we might assume a 0.8 hit ratio:

	CPU speed	Useful time after paging	Computation available to users
with cache hitting 0.8	.85 mips	90%	.76 mips/cpu

Recommendations

1. Since the actual hit ratio to be expected by a cache is uncertain, and since even the most optimistic assumptions merely bring system performance near to that originally anticipated, I suggest that we recommend to IPC that they insist that HISI perform the first part of the large memory upgrade without additional charge. (That is, install a cache in each cpu and replace the bulk store and 384k core with MOS memory). This should leave IPC prices and utilization unchanged, but return the system to a position where its first-shift load is 60% of its capacity rather than 100%.

2. For each $25k/month ($300k/yr) in additional revenue which Project MAC can provide or locate, an additional 2M word memory box could be attached. This price is quite reasonable, and some arrangement along these lines should be pursued. This path requires the minimum effort in system engineering to a large memory system.

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To: 6180 Performance File

From: J. H. Saltzer

Date: November 28, 1973

Subject: Cache hit ratios required for 6180 performance

I. CPU model

The measured speed of the 6180 running Multics is 0.65 mips, or 1500 ns/inst. That speed is with a 650 ns. memory access time as viewed inside the 6180 cpu. If we assume (from instruction timings with maximum overlap) that the speed with a zero-access time memory is 1.25 mips, or 800 ns/instructions, we conclude that the 650 ns. memory produces about 700 ns. of delay per instruction, or 1.1 memory delays per instruction. We thus crudely estimate that the time per instruction, t_i, is

$$t_i = 800 + 1.1t_m \text{ nanoseconds}$$

where t_m is the average memory access time and we have grossly simplified lookahead and overlap details.

II. Cache model

Assume a 100 ns. cache and a 1200 ns. main memory. Assume that access to main memory is serial with cache access, so that the time for access when the cache fails to hold the desired item is (100 + 1200) ns. If the hit ratio (success rate) is r, the average access time is then:

$$t_m = r \cdot 100 + (1-r) \cdot 1300 \text{ ns.}$$

III. Hit ratios required for particular performance levels

We now calculate values for some particular possible performance levels.

for this hit ratio		the average access time would be	and the cpu would run at	giving a performance relative to the 6180 of
	0	1300 ns.	0.45 mips	.69
minimum hit ratio required not to retrogress	.5	700 ns.	.63 mips	.97
	.54	650 ns.	.65 mips	1.0
	.6	580 ns.	.70 mips	1.07
	.7	460 ns.	.77 mips	1.18
	.8	340 ns.	.85 mips	1.30
	.9	220 ns.	.96 mips	1.47
	1.0	100 ns.	1.1 mips	1.69

Note that these performance predictions are very sensitive to some untested assumptions, particularly

1. cache speed, assumed to be 100 ns.
2. primary memory speed, assumed to be 1200 ns.
3. cpu speed with zero-access time memory, assumed to be 1.25 mips.