HONEYWELL INTEROFFICE CORRESPONDENCE

PHOENIX OPERATIONS – HONEYWELL INFORMATION SYSTEMS

file - Long Memory proj

Rec'd 10/23/73 RSH

DATE 16 October 1973 PHONE 993-5370 MAIL ZONE B126 COPIES: CT Clingen

TO R. E. Hoffman

FROM R. F. Montee

COMPONENT Programs

SUBJECT CONFIRMATION OF TELECON DATED 12 OCTOBER 1973

Confirming our telecon of Friday, 12 October, 1973, the Upper/Lower bound simulation of Multics performance with Cache and MOS memory is being run. The anticipated completion date is 22 October, assuming that all computer simulation runs are completed by 15 October and allowing a minimum of 1 week for analysis of the simulation results.

A check with the reliability analysis unit regarding the maintenance strategy modeled in the HMOS memory simulation indicated that no explicit maintenance model was employed but the implicit assumption in the model was that all chips were functioning at the beginning of each day's run, i.e., the failed chip(s) of the previous day had been replaced. No probability factors were assigned that the failure was the second failure within the same word-pair.

I am enclosing an interesting article from Electronic News on 4K RAM chips. As you can tell from the tone of this article, it is still quite early in the development cycle of this technology.

R. F. Montee

R. F. Montee

/si
Enclosure