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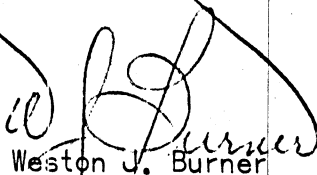
CC: E. Glaser
    R. Daley
    A. Dean
    L. Mikus

October 25, 1967

Professor F. J. Corbató
Project MAC
Massachusetts Institute of Technology
545 Technology Square
Cambridge, Mass.

As per our telephone conversation of today I am attaching hereto the
current Phase B swap out plan for the GE645 equipment at Project MAC.

Our headquarters operation is now working to this plan so if there are
any serious objections please let me know as soon as possible.

In any case it is imperative that we commit ourselves to some accept-
able schedule and proceed to that end. Can I please have your approval
and comments by November 8.

Weston J. Burner
Account Manager

WJB/ak

Attachment

MIT MOD B SITE CHANGE-OUT PLAN

REVISION C
OCTOBER 10, 1967

L. E. MIKUS, MANAGER
645 SYSTEM INTEGRATION UNIT

NOTE:

* Indicates paragraphs added, deleted, or changed from Revision B

Intent

This document attempts to define the tasks, sequence of events, and other actions that are necessary to smoothly replace the dual Mod A 645 computer system at MIT with a dual Mod B system. Revision B of this document was prepared after inputs from MIT were received. Revision B differs significantly from Revision A and no attempt is made to correlate the two revisions.

This is a working document. Further revisions are expected as change out plans solidify.

This document does not attempt to plan all hardware changes taking place at the MIT 645 site. Not covered are the following:

* Installation and site check-out of both DDA's and the Data Products Disc subsystem. This plan assumes both DDA's have been installed in the Mod A GIOC's some time before Mod B equipments reach the site. If one of the DDA's is delayed, then it will be installed along with the first Mod B GIOC.

* Addition and check out of the RACE subsystem.

* Removal of peripherals once they are no longer needed (such as common Peripheral drum) unless they affect the retrofit program.

Goals

The change-out proposal keeps in mind the following objectives during change-out.

* Leave a usable 256K single system (usable for either MULTICS or GECOS) up at all times.

* Install only one major piece of hardware at a time (CPU or GIOC) and build confidence in the new hardware before another major piece is installed.

* To minimize the time both Mod A and Mod B software is running on the system, the two GIOC's will be installed successively.

* Non-major boxes (EMM controller, SCC, clocks, MM8040's, MM8030 updates) will be installed to minimize impact upon the usability of the remaining equipment.

1

Retrofit Task Summary

The following tasks must be performed to implement the retrofit program:

* Replace both Mod A CPU's with Mod B CPU's.

* Replace both Mod A GIOC Controllers with Mod B Controllers

* Remove: 2-HPC's

   Replace: 6-HPC's
   6-TTA's
   2-CAA's
   2-CSA's
   1-DDA
   1-IPA
   2-CAB 600's (including ribbon cables)

   Update: 1-IPA
   2-DGA's
   1-DDA

* Replace existing extended memory file and controller with new extended memory file and updated controller.

* Add SCC (plus cables).

* Replace Mod A dual system clock and cabinet with a Mod B dual system clock and new CAB601 cabinet.

* Update two system controllers for remote reconfiguration.

* Replace two MM8030 system controllers with two MM8040 system controllers.

* Remove the manual switch console.

The equipment will be turned over to the customer in several parts - effectively after each major piece of hardware is installed and checked out.

Customer turn-over for each part will occur after an on-site acceptance test is completed where all applicable T & D plus a GECOS II supplement for the Mod B system will be successfully demonstrated.

GECOS II Supplement Terminology

To describe new 645 GECOS supplements, the following definitions have been coined:

K3GECOS: GECOS supplement that runs with a Mod A 645 system, common peripherals, and DSC11F/DSU10F.

K4GECOS: GECOS supplement that runs with a Mod B 645 system, common peripherals, and DSC11F/DSU10F.

Change-Out Phases

Site change-out of the GE645 system can be divided into nine distinct phases.

Phase I

The hardware is essentially all Mod A. Some updates and changes that can be added without affecting the customer's use of the dual Mod A system will be completed.

Phase II (Est. two weeks)

One Mod B CPU is installed and checked out. The customer has use of only a single Mod A system.

Phase III (Est. two weeks)

The customer has use of two systems (One Mod A and one with a Mod A GIOC and a Mod B CPU). Since the Mod B CPU is fully program compatible with the Mod A CPU, the mixed Mod A/Mod B system should operate effectively. This period of time is used to build confidence in the new Mod B CPU.

Phase IV (Est. two weeks)

One Mod B GIOC and associated adapters is installed and checked out. Either the Mod A CPU or the Mod B CPU can be used for GIOC check out. The customer has use of a single system with a Mod A GIOC and either a Mod A or Mod B CPU.

Phase V (Est. four to six weeks)

The customer has use of one Mod A CPU, one Mod B CPU, one Mod A GIOC and one Mod B GIOC. Both MULTICS and the customer's use of GECOS must be converted to the Mod B GIOC before the next phase can begin. This period of time is used to debug the Mod B GIM and to build confidence in the new Mod B GIOC.

Phase VI (Est. two weeks)

The second Mod B GIOC and associated adapters is installed and checked out. Again, either the Mod A CPU or Mod B CPU can be used for GIOC check out. The customer has use of a single system with a Mod B GIOC and either a Mod A or Mod B CPU.

Phase VII (Est. one week)

The customer has use of two Mod B GIOC's, one Mod A CPU and one Mod B CPU. This period of time is used to build confidence in the new GIOC.

Phase VIII (Est. two weeks)

The second Mod B CPU is installed and checked out. The customer has use of a single Mod B system.

Phase IX

The customer has full use of the dual Mod B system.

The above time estimates are given for planning purposes. Actual times may vary from these figures. The time estimates assume:

- Systems test in Syracuse will be extended approximately one month to check out Mod B CPU hardware by running debugged programs developed by MIT that exercise the paging/segmentation hardware under a GECOS environment.

- Debug of the GIM for the Mod B GIOC will occur in Cambridge after the first Mod B GIOC is turned over to the customer.

Check-out System Requirements

The minimum additional check-out memory and peripheral equipment that must be provided full time during Phase II, Phase IV, Phase VI, and Phase VIII is:

- System Controller with 64K memory

- One channel mag tape with two handlers

- One Operator Console

- One Printer

In addition, the following peripheral equipment must be available part time:

- Mod 33, 35, or 37 TTY on dial up plus one 103E and one associated 801 ACU with EIA option (for DGA check out and acceptance tests). (Estimate: 8 hours each Phase IV and Phase VI)

- Additional peripherals to run K4GECOS (for acceptance tests):

  2 more tape handlers
  1 card reader
  1 card punch
  1 DSC11F/DSU10F or DSU200
  (Estimate: 32 hours each towards the end of Phase II, Phase IV, Phase VI, and Phase VIII)

It is not possible to share the same standard common peripheral dual magnetic tape controller between the customer's system in use and the Mod B system being brought up. Special interrupts resulting from a rewind or rewind/unload command are transferred on the channel that issued the command. However, special interrupts resulting from handlers reverting to the ready status from standby or Tape Handler Unit Check status are always transferred through only one channel. Thus it would be impossible for one system to receive all necessary special interrupts and for the other system to sort out extraneous interrupts.

To overcome this difficulty, SIPD (with MIT FEO's concurrence) will put a temporary design change in the magnetic tape controller such that a manual switch can direct the ambiguous special interrupts occuring to a selected channel. This would require checking the switch every time a manual operation on a tape handler is initiated.

In addition, the handler with device code 04 will be made to respond to device code 00 from one channel only (the channel allocated to bringing up the new equipments). In effect, there will be two quasi-independent tape subsystems each with a tape handler responding to device 00 and each with three other handlers (01, 02, and 03 for one channel and 05, 06, and 07 for the other channel).

The proper GECOS control cards must be employed and T & D test 157 and test 357 must be modified to utilize only handlers with device codes 00, 05, and higher.

Minimum Customer System

After discussion with MIT, the following __minimum__ equipment must remain available to them full time:

```
192K of core (256K desirable)
1          CPU
1          GIOC and associated adapters
1          Channel magnetic tape with two handlers
1          Printer
1          Card Punch
1          Card Reader
1          Operator console
1          DSC11F with two files
1          EMM
1          System Clock
1          Manual Switch Box
Peripheral switches
```

With the addition of a temporary design change in the magnetic tape controller, it is possible to meet the minimum equipment requirements of both the customer and for new equipment check out by utilizing the equipment now on site.

Memory and Systems Clock Requirements

A back-up auxiliary memory (64K) is now on site. Since MULTICS requires 256K and an additional 64K is required to bring up each simplex Mod B system, a 64K back-up memory must remain on site at least until the retrofit program is completed. Also, while two of the four MM8030 system controllers are being updated for remote reconfiguration (one at a time), the back-up memory is necessary to retain 256K working core for MULTICS.

The 64K back-up memory must always be connected into the customer system (since it is an auxiliary memory and not a system controller). The implication that interlace is not possible at these times should have no detrimental impact upon the customer system.

The Mod A System Clock is housed in a basic cabinet without the ability to add core memory to the cabinet. Connections are made via six cables (3 to each CPU).

The Mod B System Clock is housed in a CAB601. The CAB601 has a new snowplow to accommodate the clock option. Up to 64K of core memory can also be added to the CAB601. Connections are made via 12 cables (6 each to two MM8040 system controllers).

The Mod B clock must connect to a MM8040 and cannot connect to a MM8030 (635 system controller). Also, the clock cannot be mounted in a 635 type auxiliary memory cabinet, but must mount in a CAB601.

To satisfy the space requirements on site, the existing 64K back up core and vendor logic will be moved to the CAB601 with the Mod B clocks. This should be accomplished during Phase I. The Mod B clocks can be used in a system only if the associated MM3040's are available.

Cable Changes

Except for deviations noted in this section, existing Mod A cabling will be used in the Mod B system.

When the first Mod B GIOC is installed, it will come complete with GIOC to CAB600 cables and CAB600 ribbon cables. The second GIOC, however, will use the GIOC to CAB600 cables and CAB600 ribbon cables from the Mod A GIOC subsystem being removed from site.

The Mod A dual system clock connects to the system by three cables to each of the two CPU's. The Mod B dual clock connects to the system by six cables to each of two MM3040 system controllers. Therefore, six additional cables are required. These six cables are presently on site (as spares) and no new clock cables need to be ordered.

Normally each Mod B system clock attaches to the auxiliary memory inter-faces of a system controller with short (8 or 15 foot) cables. However, it is acceptable to extend the length of these cables up to a total length of fifty feet. However, if core is included in the clock cabinet, the cycle time of the core in the clock cabinet only may be increased due to longer signal delays between the system controller and the auxiliary cabinet. During the equipment change out phases, 50 foot cables will be employed.

Installation of the SCC will require the following additional cables:

TO SCC	PERIPHERAL TYPE CABLES	COMMUNICATION TYPE CABLES
GIOC (2)	4 x 2 = 4	2
EMM (1)	2 x 1 = 2	
CPU (2)	4 x 2 = 4	
Syst. Contr. (4)	4 x 1 = 4	
	14	2

The peripheral type cables are 4JC13G655 GXXXXX. The communication type cables are 4JC13G63GC1. One communication type cable is used for the card Number Verification Channel and the other is used to connect a teletypewriter to the system (either via 103 dataset or directly to a TTA600 if within 50 cable feet). The current plan is to employ a 103 dataset for the teletypewriter.

Cable lengths for the peripheral type cables must be less than 150 feet and will be determined by the site layout.

When peripherals are added or removed (such as DSC11F) the addition or removal of cables will be considered as part of the peripheral installation and not as part of the Mod B retrofit program.

If the floor layout for Mod B equipments deviates from that of the Mod A, then all affected cables must be examined to determine if they can be used with the Mod B equipments.

EMM Subsystem

An interim EMM subsystem is on site today. This subsystem will be replaced by an updated controller and a new file. The updated controller has the capability to interface with the SCC (provides for remote reconfiguration).

Either the interim EMM subsystem or the replacement EMM subsystem can run with either Mod A or Mod B equipments. However, reconfiguration via SCC cannot be accomplished until the replacement EMM subsystem is installed.

Significant Events During the Change Out Phases

Phase I (Before removing Mod A equipments)

1) One at a time, update two of the MM8030 system controllers for remote reconfiguration.

2) Lay all new cables required.

3) Modify the dual Mag Tape controller to properly direct operator initiated Special Interrupts.

4) Ship the Mod B clocks and the associated CAB601 to the site and transfer the 64K core and vendor logic from the existing auxiliary memory to the CAB601. (If possible, 64K of core will be shipped in the CAB601 instead of effecting a site swap out but current schedules do not show core availability.)

NOTE: It would be desirable to do the following items during Phase I, but it is possible to do them during later phases.

* Replace two MM8030's with two MM8040's.

* Install new EMM controller.

* Install the SCC (For space reasons, the customer has requested this to occur during one of the later phases.)

Phase II

1) Remove 1 Mod A CPU

2) Install 1 Mod B CPU

Phase IV

1) On one GIOC subsystem:

   Remove: 1 HPC

   Replace: 3 HPC
                3 TTA
                1 CAA
                1 CSA
                1 IPA
                2 CAB600 (including cables)
                1 DDA

   Update: 1 DGA

* ## Phase VI

1) On the second GIOC subsystem

   Remove: 1 HPC

   Replace: 3 HPC
                3 TTA
                1 CAA
                1 CSA

   Update: 1 IPA
               1 DGA
               1 DDA

* ## Phase VIII

1) Remove second Mod A CPU

2) Install second Mod B CPU

3. Complete the installation and check out of any remaining
   Mod B equipments required to complete the equipment change out.

Site Installation Teams

Four site installation teams will be formed. Each team will consist of at least one expert on the major piece of hardware being installed. If necessary, additional personnel will be dispatched from Syracuse if specialized problems develop.

Preliminary manpower assignments are as follows (actual personnel subject to change):

Phase II:	J. Ammons*	CPU/SI
	D. Baird	CPU
Phase IV:	H. Nilsen*	GIOC/SI
	D. Lacy	GIOC
Phase VI:	D. Hansen*	GIOC
	L. Chenevert	GIOC
Phase VIII:	J. Ammons*	CPU/SI
	D. Bissel	SI

* Installation team leader

Each site installation team will be responsible for checking out the new equipment on site. Each team will arrive approximately at the same time as the hardware and will remain until checkout (including the acceptance test) has been completed.

APPENDIX II

MAGNITUDE OF WIRING TO BE

ADDED ON SITE

Change	Est. Wires Per Unit	Units Phase I	Units Phase IV	Units Phase VIII
Add SCC interface to MM8030	688	2		
DDA update	5			1
IPA update	120			1
DGA update	100		1	1

REV B

FW 1968

| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 |

PHASE I

PHASE II
2/24

PHASE III
3/9

PHASE IV
3/23

PHASE V
4/6

PHASE VI
5/11

PHASE VII
5/25

PHASE VIII
6/1

PHASE IX
6/15

MIT MOD-B CHANGE OUT SCHEDULE ESTIMATES

Nov. 3, 19 67

Memo to _Phase Blder_ .... Room .... Ext. ....

— Aux. memory prevents interlace — symmetry
— Timing problem
— aux. mem into clock cabinet ! (is it part of 256K memory)
— moving guts of aux. mem. into another cabinet
— more than 192K ?

from .... Room .... Ext. ....