TO:

M. M. Jones

FROM:

R. C. Daley

DATE:

February 14, 1969

SUBJECT: Configuration of the Multics Development Machine

## Introduction

This document proposes a series of changes in the configuration of the Multics development machine in an attempt to minimize the cost to Project MAC and maximize the usefulness of the machine. These changes are described in terms of the four steps outlined below.

> Step 1 - The development GIOC is immediately stripped down ARPA votwark to development status by removing a number of specialized communication line adapters leaving only two typewriter adapters of 16 channels each. This will give us enough capability for development work and provide a limited form of backup for the other GIOC. As a result the development GIOC cannot support ARDS terminals or remote computers and displays (e. g., (IMP) PDP-8 display monitor etc.) and will only be able to handle 2 classes of typewriters (e. g., (133) and 150 baud).

Step 2 - As soon as possible the development machine is augmented with an additional memory controller and 64K of memory for the duration of the file system performance improvement effort which is expected to be terminated before June 1. This augmentation assures that all development work may continue on the development machine while the larger Multics machine is being used to replace CTSS as the primary service machine for the Multics effort. Due to the reduced core requirement of the new file system, the additional core may be released as soon as the new file system is installed without impairing development work significantly.

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Step 3 - Once the system maintenance and MST generation activities have been successfully moved from CTSS/GECOS to Multics, the lower speed Univac drum (and its associated channel) can be released. Since this drum is only useful to improve the performance of GECOS (Multics has no use for it), it should be released by April 1. In addition, the high speed tape drives should be replaced by lower speed drives at this time.

Step 4 - Once the new file system is operational (before June 1), the additional memory controller and 64K of memory can be released.

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## Hardware to be Released on June 1

1	MM8030 - Memory Controller (w. 32K)	6760
5	OPT802 - Active Unit Ports (2 included)	252
1	OPT815 - Interrupt Cell Groups (1 included)	NC
1	AMM600 - Added Memory (32K)	4475

Total Saved 11487

## Hardware Rental

Step	Price	- Discount	= Subtotal	+ Use*	= Rent
0 (Now)	68512	13702	54810	2741	57551
1 (Feb.)	63689	12736	50953	2548	53501
2 (March)	75176	15034	60142	3007	63149
3 (April)	69941	13988	55953	3798	58751
4 (June)	58454	11690	46764	2338	49102

\*Second shift maintenance charge.

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