

Processor Interval Times

1. Always counts (downward) once per memory access greater than CPU.
2. ~~May generate an interrupt via SXC~~
When it passes zero, it may generate an SXC^{command} which is switchable to any memory controller and memory cell.
3. Generation of SXC can be generated^{by program}, although counter continues.
4. Can be loaded or reset at any time by program.