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March 9, 1966

MR. JAY ROBERTSON
General Electric Computer Department
Phoenix, Arizona

Dear Mr. Robertson:

We have reviewed the technical proposal for "System Clocks for GE 645 Prototype System" as revised on February 4, 1966, and find it generally satisfactory. Enclosed for your information is a list of comments on the proposal prepared by Mr. Chester Jones. We would be pleased to have answers in due course to the questions he raises; his other comments might well be considered in designing the system clocks for the production version of the 645, although we do not see any need for changes in the proposal for the prototype system.

We would appreciate receiving from GE, when it becomes available, model designations, prices and other such information, so that we may revise our orders to include these clocks.

Sincerely,

ORIGINAL SIGNED BY

T. H. CROWLEY
Director
Computing Science Research

MH-1373-VAV-MBT

Enc.

Copy to
Messrs. F. J. Corbato
C. Jones
V. A. Vyssotsky

Comments on 4 February System Clock Proposal

The proposed clock design is much cleaner and therefore more appealing than the 21 January version. Most of the inadequacies of the earlier proposal have been corrected. There are still several questions I would like answered concerning the current proposal.

1. Is the Comparator disabled during the loading of the Alarm Clock? If not, the Alarm Clock will be difficult to load. Consider the following case:

	2^{51}	2^{36}	2^{35}	2^{0}
CAL. CLOCK REGISTER	1	(any non-zero value)		
DESIRED ALARM VALUE	1	1111 ⟶ 1		

Now, since the Load Alarm Clock instruction sends a double precision word to the Alarm Clock Register, if the Comparator performs a compare after the first half of the desired alarm value is received but before the second half has been received, an interrupt will be sent to the memory controller.

2. On page 9, line 3, does "Command Fault Trap" mean "Illegal Procedure Fault Trap", GE 645 privileged instruction in slave mode or "Illegal Memory Command"?

3. In the event that a system includes two or more clocks, how is the calendar clock whose output is to be sent to the Comparator selected? In the earlier proposal, this was done by the RCCL instruction. I would prefer to have the LACL instruction do this.

4. For what is bit Y17 used in the RCCL instruction?

Comments

1. I like the finer resolution with which the calendar clock may be set manually.

2. I would like to be able to mask the interrupts sent from the Alarm by using other than bit 28. However, we can live with it as is.

3. The interlacing of memories is somewhat awkward.

CHESTER JONES