J. Saltzer

I made a few notes — mostly questions —

TECHNICAL PROPOSAL

SYSTEM CLOCKS

for

GE 645 PROTOTYPE SYSTEM

January 21, 1966

Accuracy Clock module — 100-115 cards

Clock Controller — 50-75 cards
85 cards — 100

Need more details. status on rate control + on increment. Δ in increment.

Can 2 clocks be synchronized in value or in rate

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GENERAL:

This proposal is a formal reply to specific requests from MIT and BTL regarding system clocks for their 645 Prototype Systems.

The system clocks are composed of three types:

1. Calendar Clock
2. Alarm Clock
3. Processor Interval Timer

The Calendar Clock is required to serve as a fine increment clock as well as a calendar clock. The minimum increment provided shall be 1.0 microsecond and the maximum capacity shall be greater than 100 years. The clock time base is to be January 1, ~~1900~~ 1901 (Universal Time). This clock shall be read as a binary number.

The Alarm Clock is required to generate a program interrupt at a preset time. The minimum increment shall be 64 microseconds. This clock shall be set as a binary number representing Universal Time.

The Processor Interval Timer shall be the timer register currently implemented in the 645 Prototype Processor (GE Spec. M50EB00107). It shall count memory cycles associated with instruction execution, but does not count memory cycles required by the segmentation and paging hardware. This timer shall be set and read as a binary count.

we must have this information. How? By putting it back in.

The Calendar Clock and Alarm Clock shall be designed to be rapidly accessible by any processor. From a programmer's viewpoint, both clocks shall be addressed directly by command as if they are contained within a memory controller.

Reliability and redundancy shall be provided within the design to enable operation for at least one year with 50% or greater probability of mission success with no maintenance and continuous power on.

Emphasis shall be given to the clock design with the consideration in mind that the clock is essential in the operation of MULTICS. Without it, the system is effectively down.

Reliability and Maintainability

The design goal for the system clocks (calendar clock and alarm clock) shall be 50% probability of mission success for 10,000 hours continuous operation, as defined by the fundamental equation.

$$P = e^{-t/m}$$

where

t = 10,000 hours

m = mtbf hours,

Redundancy

The Calendar Clock shall be redundant within the Clock module to provide greater probability of success.

Two sources of frequency standard inputs shall be provided. Both may be internal or one may be external.

* Are these statements perfectly, unambiguous? I think not, but I am not familiar with "reliability" jargon.

Two sources of DC power inputs shall be provided. One source shall be derived from a self contained AC/DC regulated power supply. The second source shall be a raw DC source provided external to the clock system.

System down time shall be minimized due to a failure of a redundant element by the following functions:

1. Either Calendar Clock Counter shall be switch or program selectable
2. Either of two oscillator sources provided may be selected by manual switch.
3. When a second source of unregulated DC power is supplied, circuitry shall be supplied to enable the highest source voltage to power the clocks, thus providing uninterrupted operation.

On-Line Operation

On-line operation shall require the following hardware functions:

- Detection of DC power dropping below a threshold value shall cause:
  - a) An interrupt condition.
  - b) A light to be turned on.
  - c) All clock outputs to be read as zeros.
  - d) Manual operation (test panel) required to reset conditions (a-c).
- Indicators on test panel shall identify:
  - a) Calendar Clock selected by program.
  - b) Power supply source voltage present.
- Ability to remove, replace, and debug at least 75% of the functions associated with each Calendar Clock Counter independent of other Calendar Clock Counter.

* A complete puzzle, except for 3.

On-Line Operation implies ~~to~~ the following software functions for error detection.

- Periodic verification of calendar clock and alarm clock operation.
- Notification to operator of detected clock failure (i.e. - typed message)
- Programmed selection of secondary calendar clock when detected failure of primary clock encountered.

MAINTENANCE PANEL

A maintenance panel shall be provided to indicate current status and to isolate and initiate functions within the Calendar Clock and Alarm Clock.

Features of the panel shall enable the Field Engineer to isolate 75% of all hardware failures within the clock system (excluding Interval Timer within the processor), with a 90% assurance.

Prime emphasis shall be given to function of testing one malfunctioning Calendar Clock while the alternate Calendar Clock is currently on-line with the system.

The test panel shall contain the following:

Display	-	Calendar Clock
		Alarm Clock
Indicators	-	Power Sources
		Selected Calendar Clock Counter
Switches	-	Set Calendar Clock - Upper 26 bit
		Select Oscillator Source
		Select Control Processor
		Select Calendar Clock Counter - 0, 1. On-Line (Program)
		Start clock - local/remote

Pushbuttons	-	Stop (Calendar Clock Not Selected) Start (Calendar Clock Not Selected)
External Connectors (BNC)		Strobe out (count 0 mod. 2^{26} of Calendar Clock counter Selected) Strobe in (external start) External Oscillator

MTBF

For purpose of calculating MTBF a failure shall be defined as an equipment malfunction resulting in need for unscheduled maintenance. An equipment malfunction is defined within GE drawing 43A145284.

The Accounting Clock module shall be designed and constructed so the MTBF shall be equal to or greater than 2×10^4 hours at a 50% confidence level.

Each Calendar Clock Counter shall be designed and constructed so that the MTBF shall be equal to or greater than 3×10^4 hours at a 50% confidence level.

MTTR

For purposes of this document the MTTR shall be defined totally by GE drawing 43A145285 and is summarized here as including:

- Diagnostic time - time to isolate the problem.
- Repair time - time to remove and replace the failed part.
- Checkout time - time to determine if repair is effective.

The clock module shall be designed and constructed so that the MTTR shall be equal to or less than 1.0 hour at a 70% confidence level for all failures. This shall be the time that the clock module is unavailable to the system. The Calendar Clock function shall be designed and constructed so that the MTTR, while its alternate Calendar Clock Counter is operating on-line, shall be equal to or less than 2.0 hours at a 70% confidence level.

FUNCTIONAL DESCRIPTION

The Accounting Clock is organized to provide two distinct functions under general control of a Clock Controller.

Calendar Clock

Purpose

The Calendar Clock provides to the system a source of real time information with sufficient time span and resolution to allow use for such varied functions as user job accounting, source of time of day to user and executive programs, and time coordination with other computer sites. It shall be designed to be set manually and run continuously with high reliability. Read-only capability shall be provided to active modules through the Clock Controller.

Implementation

The Calendar Clock shall consist of two 52 bit flip-flop counters, running independently for reliability. They shall be fed by two independent frequency sources. Only one counter is accessible at a time -- the choice being made either under program control or by a control panel switch. Counters may be stopped by control panel switches or by test signals from an external source. One of the counters may be set up to generate a start pulse to the other under appropriate maintenance conditions.

Frequency Source

Two internal sources of one megacycle pulses - shall be supplied, one for each counter. These sources are crystal controlled to a long term stability of $\pm$ 5 parts per million. This represents a drift of less than $\pm$ 3 seconds per week. One of the two sources may be switched out and replaced by an externally supplied source if desired. Panel controls are provided for this purpose. The crystal controlled oscillators shall be adjustable to compensate for frequency drift.

Counters

The two 52 bit counters shall be identical. Resolution of each is 1 microsecond. They shall be designed to minimize settling time by using appropriate look-ahead logic on the various counter segments. Settling time shall be designed to be less than half of a read cycle time. Logic shall be included to assure that no counts are lost which may occur when a read cycle is initiated. The most significant half of a counter may be set by panel switches while the counter is stopped. Output of the selected counter shall be serially multiplexed onto a 36 bit buss as two words and sent to the Clock Controller. A test pulse shall be generated every 16.8 sec. (2^{26} μ sec.) to start the other clock counter or an external clock.

Alarm Clock

Purpose

The Alarm Clock shall be designed to supply wake-up interrupts to MULTICS at desired times. The Any processor may calculate a desired calendar time, load it into the Alarm Clock and shall be sent an interrupt at that time with 64 μs. resolution.

Implementation

The Alarm Clock shall consist of a 46 bit holding register and a 46 bit equal-or-less comparator.

Register

The Alarm Clock Register shall be loaded in two halves from a 36 bit data bus from the Clock Controller. Its output is connected permanently to the comparator and shall be displayed on the Maintenance panel.

Comparator

The 46 bit comparator shall look at A - the Alarm Clock Register and B - the Calendar Clock Counter presently selected as active. A comparison of $A \leq B$ is made and the true compare is sent to an interrupt cell in the Clock Controller. Thus as a program check an interrupt will be generated immediately if a time smaller than the present time is loaded.

after the interrupt does the compare bit go down?

Clock Controller

Purpose

The Clock Controller shall allow a processor to access the Calendar Clock and Alarm Clock as if they were special registers in a memory controller. Ports shall be provided for multiple processor connections. Interface specifications are identical to those contained within the 645 Prototype System Specification M50EB00105 (Section 3. - , Appendix A), except as follows:

a) Only two ports are provided. One is switch selected as "control" and the processor on this port shall receive all Alarm Clock and Fault execute interrupts. This port shall also have highest priority in case simultaneous interrupts arrive at both ports.

Maximum of 2 processors?

Who is sending interrupts to the ports?

b) Only three Memory Commands shall be recognized.

1) XEC - Execute. A code specifying the highest priority execute interrupt present shall be placed on the data lines and that execute interrupt cell will be reset. Legal only for the control port.

2) SAC - Set Alarm Clock. Generated as a result of execution of the LACL (Load Alarm Clock) instruction. Places the double precision word sent by the control processor into the 46 bit Alarm Clock Register.

3) RCC - Read Calendar Clock. Generated as a result of execution of the RCCL (Read Calendar Clock) instruction. The contents of the 52 bit Calendar Clock counter specified by the least significant bit of the address shall be sent as a double precision word to the requesting processor. If a power-failure alarm has occurred and has not been reset, all zeros shall be returned for this command.

c) Only the least significant bit of the 18 bit address is recognized. This shall be used to select either Calendar Clock counter 0 or 1 as the active counter for time references and Alarm Clock comparisons.

d) Only three Illegal Action codes are possible.

1) $\overline{\text{Control}}$ (for XEC if not control)
2) Non-Existent Address (for any but the 3 legal commands)
3) No Illegal Action

e) Cycle time for the XEC command is less than 800 ns.

f) Cycle time for the SAC command is less 1.7 μs.

g) Cycle time for the RCC command may vary from 500 ns to 1500 ns depending on whether or not Calendar Clock is in process of incrementing. However, average cycle time shall be 1 us or less.

What if another processor or GPIC is reading it?

h) Execute interrupt cells shall be provided for Wake-Up interrupt, Power Failure interrupt, and one spare. Cells may not be masked or set by a processor.

Tilt

i) the ~~$~~ CON is not provided.

j) Zone lines are not provided.

This must be fixed.

Is there a control processor for the controller

Instructions

The programming instructions associated with the accounting clock shall be as follows:

- LACL - Load Alarm Clock
- RCCL - Read Calendar Clock

RCCL allow access NC.

Both instructions shall be executed in master mode only. The functions of each are described below:

MNEMONIC	NAME	OP CODE (OCTAL)
LACL	Load Alarm Clock	453

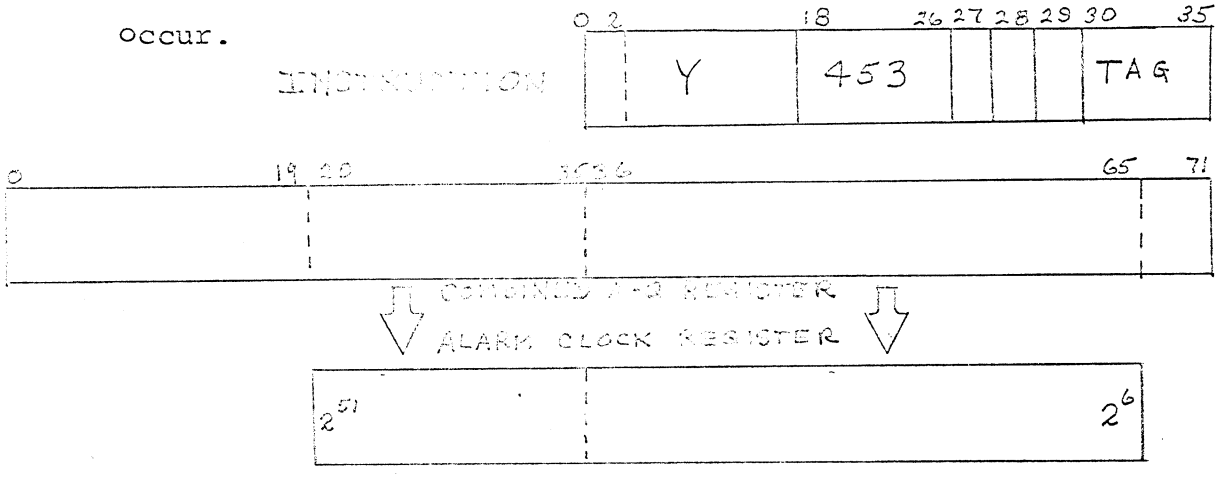
Summary: C (AQ) ⇛ C (Alarm Clock Register) located in clock module & connected CPU port specified by Y0-2

Modifications: All except DU, DL, CI, SC

Indicators: None affected

NOTES: 1. The effective address Y is used in selecting a Memory (clock) module as with a normal memory access request. However, the selected module does not store the data received in a memory location, but in its Alarm Clock Register.

2. This instruction can be used only in the Master Mode by any either Processor. If the use of this instruction is attempted by a Processor that is in the Slave Mode a Command Fault Trap will occur.



MNEMONIC	NAME OF INSTRUCTION	Op Code (Octal)
RCCL	Read Calendar Clock	633

Summary: C (Calendar Clock) ⇒ C (AQ)

Calendar Clock located in clock module connected to CPU port specified by Y0-2 and Y17

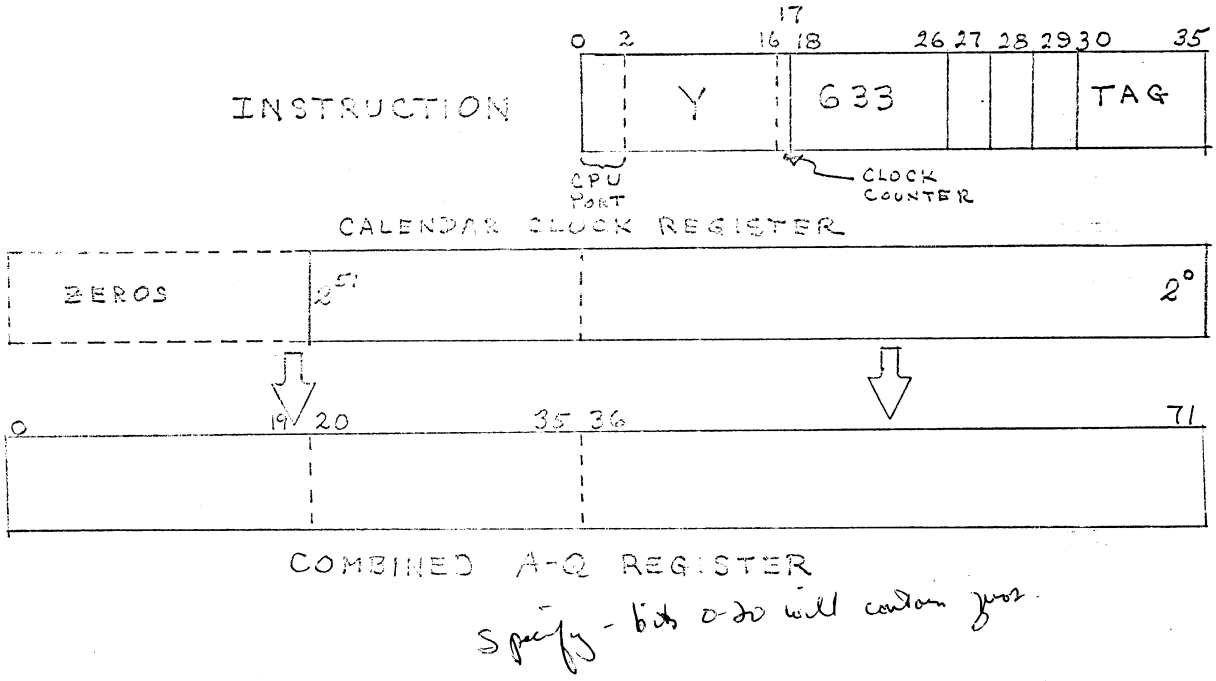
Modifications: All except DU, DL, C1, SC

Indicators:

INDICATORS: (Indicators not listed are not affected)

Zero	If C(AQ) = 0, then ON; otherwise OFF

NOTES: 1. The effective address Y is used in selecting a Memory (clock) module as with a normal memory access request. However, the selected module does not transmit the contents of an addressed memory location [except as specified by,] but the contents of its Calendar Clock.



Specify - bits 0-20 will contain ZEROS

2. This instruction can be used only in the Master Mode by either ? Processor. If the use of this instruction is attempted by a Processor that is in the Slave Mode a Command Fault Trap will occur.

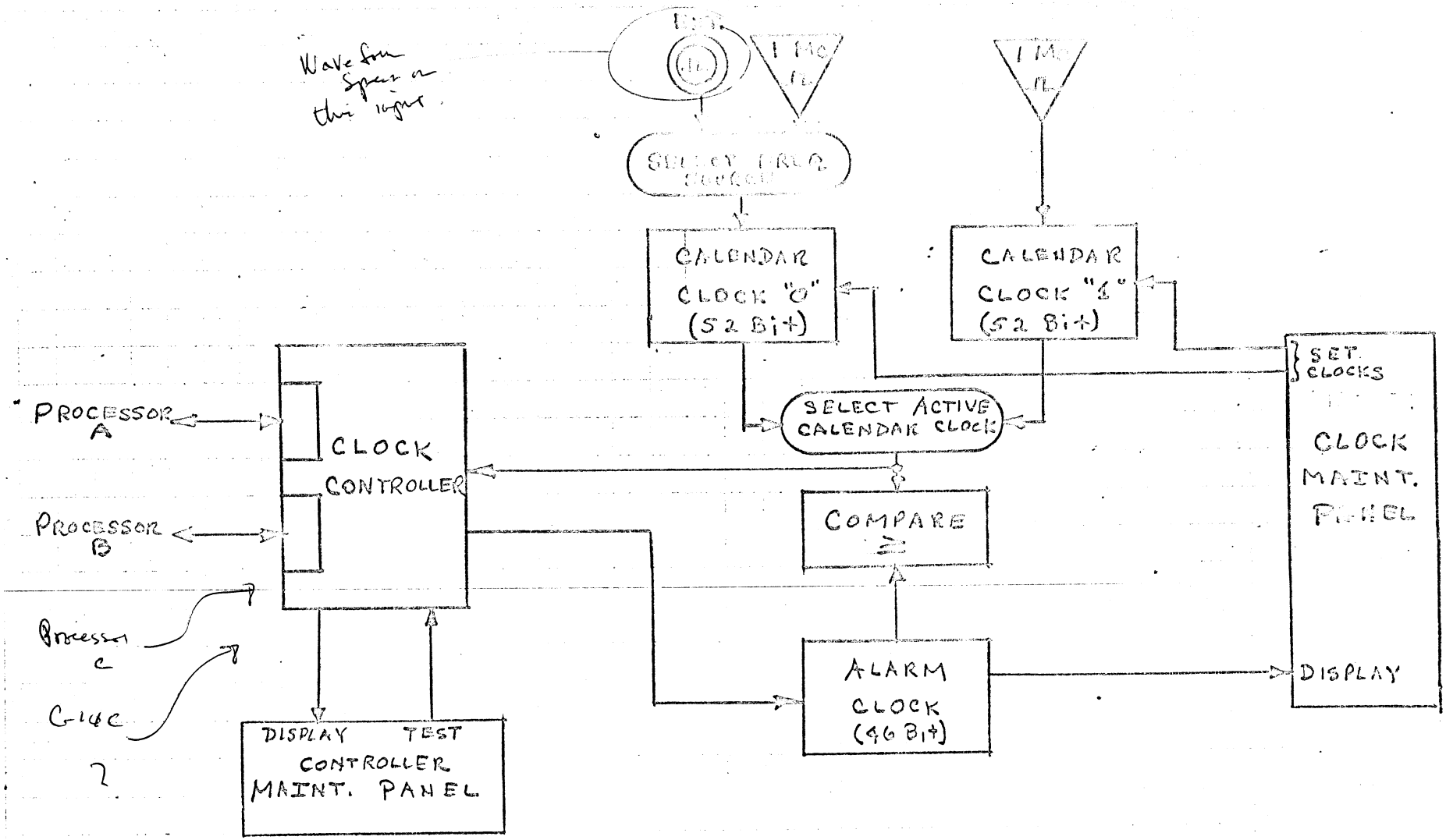
slave slave occurs.

3. Bit 17 of the operand addres (Y) shall designate which of the two Calendar Clock counters available in the clock module shall be read.

4. The Alarm Clock shall be compared against the Calendar Clock counter last selected by this command, or by manual switch.

use manual switch if slave access allowed.

We could make this
1. inoperative in Slave Mode
or
2. operate only on the LACL inst.



G45 SYSTEM
ACCOUNTING
CLOCK

D N Lueders
1/20/66