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Identification

System Clock operation
J. H. Saltzer

Purpose

The system clock is a hardware device which can be read by
the operating system or by any user program; its contents
can be used to determine both the date and the time of day.
Its use is essential to the operation of the Multics supervisor.
It is used to generate unique identifiers to label files
of the file system and events happening within the system;
most of the system accounting and administration procedures
are based on this clock. If an operating system clock is
not available, the Multics supervisor cannot be run.
This section describes the method of setting the clock, and the only
other routine operations procedure performed by the operation
staff on this device.

Discussion

It may, upon occasion be necessary to reset the system
clock. It should, for example, be reset whenever it is

observed that times printed by the system are more than

one minute in error. (If maintaining the clock to this tolerance

requires resetting it as often as once a week, an internal

adjustment should be made by the field engineer; an appropriate

trouble report should be initiated.)

The system clock
should be reset at a time when Multics is not operating,
since a sudden clock change requires a large number of
accounting adjustments. Although the operating system is
capable of discovering the clock resetting has occurred and
taking appropriate action, the action may be quite costly
to undertake. (Note: the initial version of the Multics
will stop if it discovers that the operator has reset the
clock.)

In a system with only one clock, that clock may only be reset at ~~øx~~ a time when Multics is not operating. In a system with two or more clocks, an incorrectly set clock should first be reconfigured ~~øff/øinf~~ off-line, after which it may be reset. A further reconfiguration will then bring the newly-set clock back on-line. In this way, the ~~øyø~~ operating system can chhose when it wishes to begin using the ~~nøv/~~clock ~~/øynøøy,~~ reset ~~r~~ather than having a reset clock thrust upon it at an awkward time.

In a system with two or more clocks, all clocks should normally be left on-line. Although only one of these clocks will be used as the primary time reference, the others will then be instantly available in case of trouble with the primary ... the clocks have extensive ... and trouble ... reporting ... into them, and ... system ... of these troubles ... or

The Clock itself.

~~y~~ A System Clock is a 52-bit binary register which counts up once every microsecond under control of an internal (precisely controlled) oscillator. The upper 36 bits of this register are displayed on a set of/octal readout lights, twelve and may be set by means of twelve octal dial switches. Setting is accomplished by placing the desired value in the twelve octal dial switches, and ~~xhøn~~ when the time corresponding to this value arrives, depressing the <u>set clock</u> button. ~~Thø/føxxøyin/ø øxøøø/ørøøxø/bø/føxxøyøø//~~ The clock setting procedures ~~is~~ are summarized in the next section.

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...automatically performed ... recently ... the clock a ... would take.

For Multics operation, the ~~øxøøx~~ system clock is set to contain the number of microseconds since 0000 ~~GMT~~, January 1, 1901; a *Greenwich Mean Time (GMT)* table of octal switch settings ~~Whxøh/øxyø~~ in terms of local date and time is used to avoid hand calculations each time the clock is to be set. ~~Since~~ This table ~~xø~~ only gives values

                                but
at one-hour intervals,/values for other times can be obtained
                     clockval
by executing the ~~clock value~~ command described in section
CX.3.01.   (Only if Multics is running, of course.)

Note that since the clock value is based on GMT and a standard
date, the clock does not need to be ~~is~~ reset when daylight
savings time switches in and out of operation. The switch
to and from daylight savings time is taken care of automatically
by programs which read the clock and ~~print~~ compute dates and
times from its value/ for printing.

                                                in
Note also that two ~~system~~ system clocks ~~in~~ different   time
zones contains the same clock value. Again, the correction
for time zone is taken care of automatically by any program
which reads the clock and computes dates and times from its
value.

⇈ #

In a system ~~with~~ with two or more system clocks and in which
                satisfactory
one has a/~~correct~~/value and the second needs to be reset, it
is possible to synchronize the second clock to contain ~~the~~/exactly the
same value as the first one. This is done by setting the
                                contain the
dials of the second clock to ~~contain a~~/value of a synchronizing
point which the first clock will soon pass. (Synchronizing
                              16
points occur about every ~~20~~ seconds.) Shortly before the
synchronizing time occurs, the **arm synchronization** button is
depressed. When the synchronizing time occurs, a pulse will
be sent from the first clock, the octal readout lights will
display the new value, and the clocks are synchronized.

~~Since~~ synchronizing points occur ~~when the~~ whenever the bit 26 of the clock change value. Since
these times are hard to compute or even tabulate, the ~~clockval~~ command should be used to
obtain a list of nearby synchronization points.

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on page 2

Clock setting procedure.

1 2. Reconfigure the system so that the clock in question is
off-line. In a single clock system, this step can only
be accomplished by taking Multics down.

2. Establish a value to be set into the clock dial switches
which corresponds to
~~for~~ some time in the near future. This value may be
obtained either by running the ~~clock-set/~~ clock-value
command as described in CX.3.01, or by looking up a value
in the published table of clock values.

3. Set ~~this~~ value the obtained in 1. into the clock dial switches.

4. When the time corresponding to the value set in the dial
switches/ occurs, depress the set clock button located
near the dial switches. The octal readout lights should
immediately display the new value and begin counting up.
~~from it.~~

Clock Synchronizing Procedure.

(This procedure is only applicable to systems with more
than one system clock.)

1 2. Reconfigure the system so that the clock to be set is
off-line.

2 1. Establish a value to be set into the clock dial switches
for some time in the near future that corresponds to a
synchronizing point of the clock to which synchronization
will be made. This value may be obtained ~~by the~~ by using the clockval command.

3. Set ~~this~~ value the obtained in 1. into the clock dial switches.

4. At any time within ~~20~~ 16 seconds ~~previous/~~ before the time
set in the switches depress/the ~~arm~~ once and hold arm synchronization
button located near the dial switches. When the clock begins counting, release the button. ~~When the synchronizing
time occurs, a pulse will be sent from the other clock,~~

Standard switch settings.

When a system clock is on-line, panel switches on the
clock itself should be set as follows:

Display: ccu

Operating Mode: on-line

Power up/down sequence.

~~The~~ A system clock is powered ~~indep~~ independently of the
main ~~frame of the~~ 645 computer system, and does not take
part in main frame ~~048~~ power up or power down sequences.
In general, even when ~~pole~~ power is taken down on the main
computer, for motor-generator-set maintenance or for vacation
periods, power should be left on in the system clock so
that it will not need to be reset and so that its temperature stability
will not be disturbed.