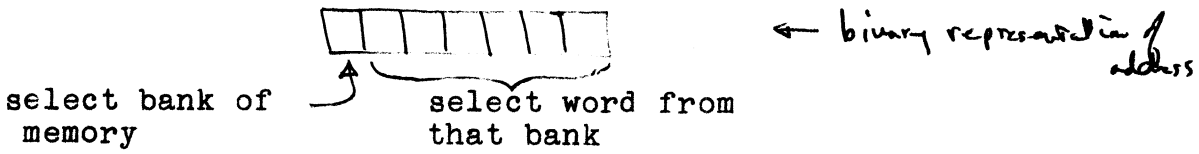
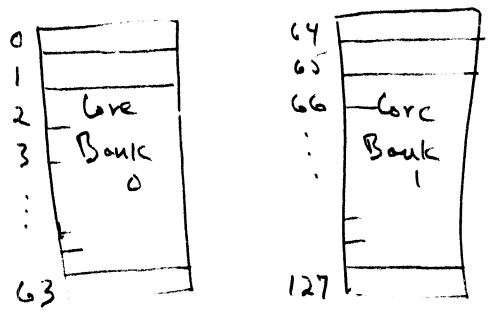
Corby,

On interlace:

Consider 128 words of memory in 2 banks of 64 words each. With no ~~Ø~~ interlace, the seven bit address is broken up as follows:



and addresses would be assigned as follows:

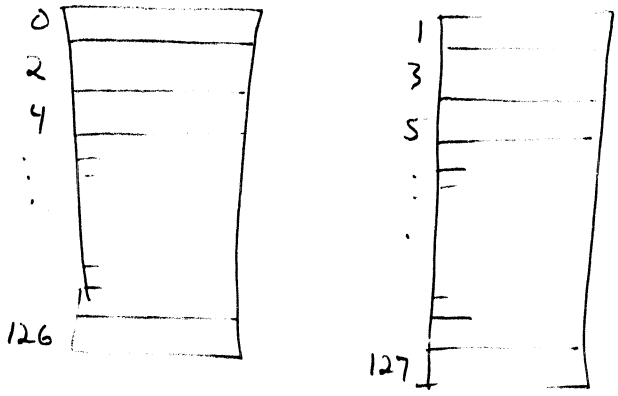


No Interlace ←

The simplest, most straightforward interlace scheme is done by reinterpreting the seven bit address, as per:

with the result that all even-numbered addresses fall in the bank numbered zero, and odd-numbered addresses fall in bank one.

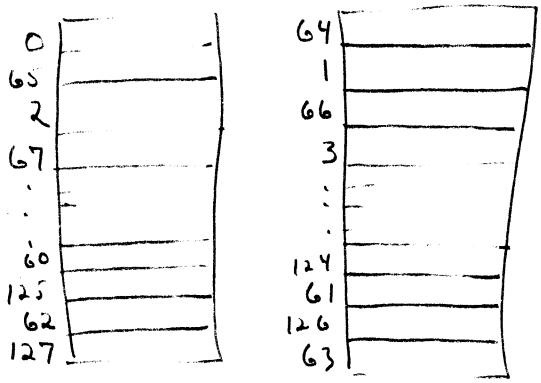
and addresses are assigned as follows:



Simple Interlace

This scheme has the difficulty that all addresses which are multiples of 2 (and therefore 8, and 64) fall in the same bank of memory. All pages would begin ~~%~~ in the same bank, and all GIOC mailbox addresses would fall in the same bank. (Since GIOC/s set mailboxes to the nearest 0mod64 address.) And all GIOC interrupts would be directed to the same bank of memory, and thus to the same CPU.

The GE interlace scheme results in the following address assignment:



GE 600-line Interlace

Note that with this scheme, the first 64-word page is based in bank zero, while the second page is based in bank one.
Exercise: deduce hardware logic with above result.

Jerry